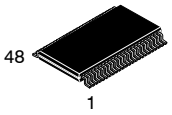
Low-Voltage CMOS 16-Bit D-Type Flip-Flop

With 5 V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

MC74LCX16374



TSSOP-48
DT SUFFIX
CASE 1201

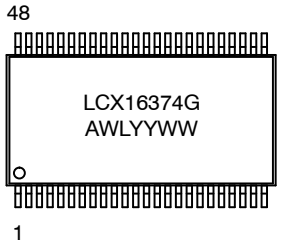
The MC74LCX16374 is a high performance, non-inverting 16-bit D-type flip-flop operating from a 1.65 V to 5.5 V supply. The device is byte controlled. Each byte has separate Output Enable and Clock Pulse inputs. These control pins can be tied together for full 16-bit operation. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5 V allows MC74LCX16374 inputs to be safely driven from 5.0 V devices.

The MC74LCX16374 consists of 16 edge-triggered flip-flops with individual D-type inputs and 5.0 V-tolerant 3-state true outputs. The buffered clocks (CPn) and buffered Output Enables ($\overline{OEn}$) are common to all flip-flops within the respective byte. The flip-flops will store the state of individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the $\overline{OE}$ LOW, the contents of the flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. The $\overline{OE}$ input level does not affect the operation of the flip-flops.

Features

- Designed for 1.65 to 5.5 V V_{CC} Operation
- 6.2 ns Maximum t_{pd}
- 5.0 V Tolerant – Interface Capability With 5.0 V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When V_{CC} = 0 V
- LVTTL Compatible
- LVCMOS Compatible
- 24 mA Balanced Output Sink and Source Capability at V_{CC} = 3 V
- Near Zero Static Supply Current in All Three Logic States (20 μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 100 mA
- ESD Performance:
  - ♦ Human Body Model >2000 V
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MARKING DIAGRAM



A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

© Semiconductor Components Industries, LLC, 2012

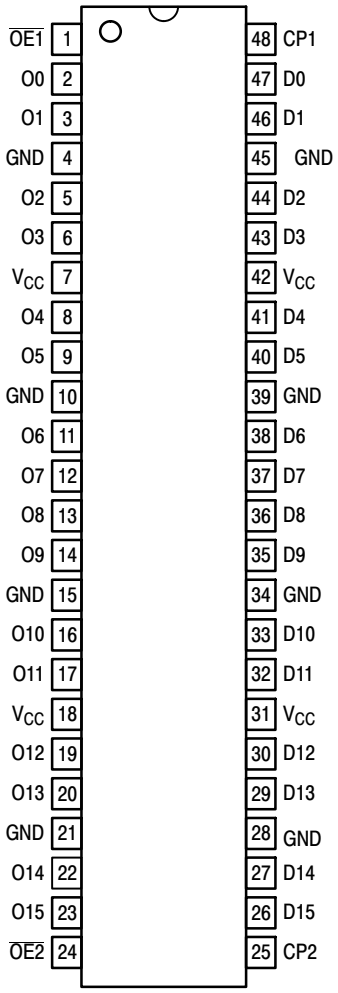


Figure 1. Pinout: 48-Lead
(Top View)

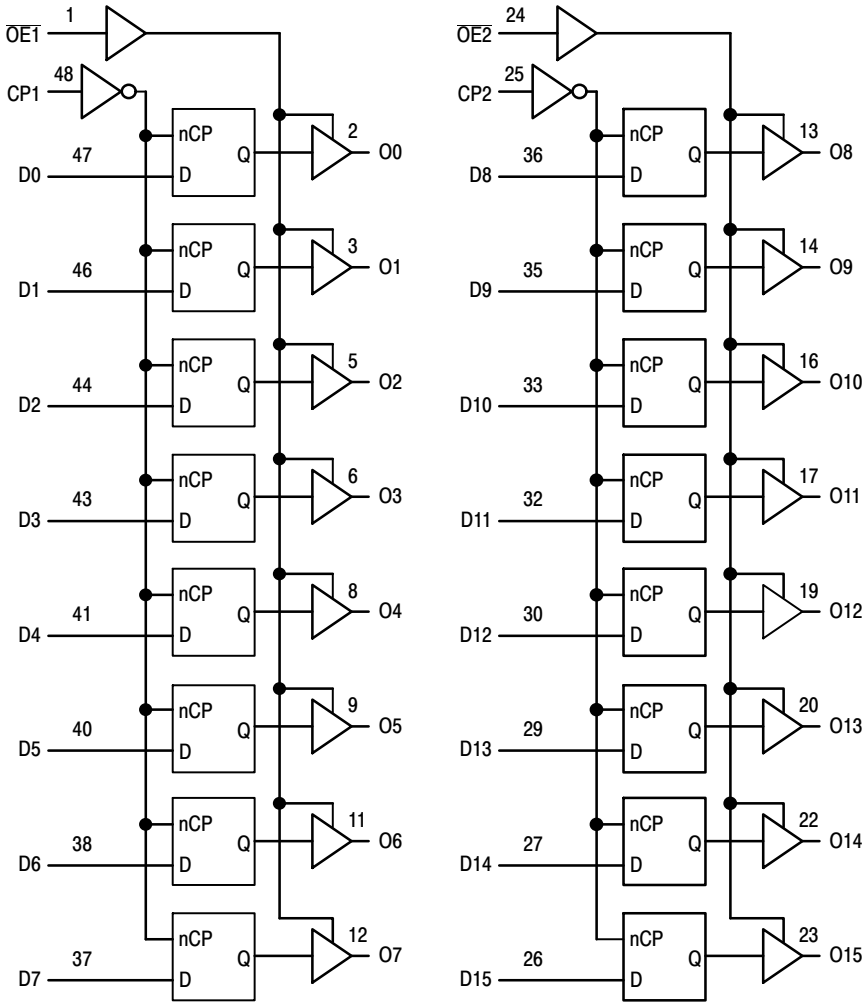


Figure 2. Logic Diagram

Table 1. PIN NAMES

Pins	Function
$\overline{OEn}$	Output Enable Inputs
CPn	Clock Pulse Inputs
D0–D15	Inputs
O0–O15	Outputs

TRUTH TABLE

Inputs			Outputs	Inputs			Outputs
CP1	$\overline{OE1}$	D0:7	O0:7	CP2	$\overline{OE2}$	D8:15	O8:15
↑	L	H	H	↑	L	H	H
↑	L	L	L	↑	L	L	L
L	L	X	O0	L	L	X	O0
X	H	X	Z	X	H	X	Z

H = High Voltage Level
L = Low Voltage Level
Z = High Impedance State
↑ = Low-to-High Transition
X = High or Low Voltage Level and Transitions Are Acceptable; for I_{CC} reasons, DO NOT FLOAT Inputs

Share Feedback
Your Opinion Matters

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		–0.5 to +6.5	V
V_{IN}	DC Input Voltage (Note 1)		–0.5 to +6.5	V
V_{OUT}	DC Output Voltage (Note 1) Active-Mode (High or Low State) Tri-State Mode Power-Down Mode (V_{CC} = 0 V)		 –0.5 to V_{CC} + 0.5 –0.5 to +6.5 –0.5 to +6.5	V
I_{IK}	DC Input Diode Current	V_{IN} < GND	–50	mA
I_{OK}	DC Output Diode Current	V_{OUT} < GND	–50	mA
I_O	DC Output Source/Sink Current		±50	mA
I_{CC}	DC Supply Current per Supply Pin		±100	mA
I_{GND}	DC Supply Current per Ground Pin		±100	mA
T_{STG}	Storage Temperature Range		–65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 secs		260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 2)		71	°C/W
P_D	Power Dissipation in Still Air		1765	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage (Note 3) Human Body Model Charged Device Model		 >2000 N/A	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I_O absolute maximum rating must be observed.
2. Measured with minimum pad spacing on an FR4 board, using 76 mm-by-114 mm, 2-ounce copper trace no air flow per JESD51-7.
3. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage Operating Data Retention Only	 1.65 1.5	 2.5, 3.3 2.5, 3.3	 5.5 5.5	V
V_{IN}	Digital Input Voltage (Note 4)	0		5.5	V
V_{OUT}	Output Voltage (Note 4) Active Mode (High or Low State) Tri-State Mode Power Down Mode (V_{CC} = 0 V)	 0 0 0		 V_{CC} 5.5 5.5	V
T_A	Operating Free-Air Temperature	–55		+125	°C
t_r, t_f	Input Rise or Fall Rate V_{CC} = 1.65 V to 1.95 V V_{CC} = 2.3 V to 2.7 V V_{IN} from 0.8 V to 2.0 V, V_{CC} = 3.0 V V_{CC} = 4.5 V to 5.5 V	 0 0 0 0		 20 20 10 5	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

Share Feedback
Your Opinion Matters

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40 °C to +85 °C		T_A = −55 °C to +125 °C		Unit
				Min	Max	Min	Max	
V_{IH}	High-Level Input Voltage		1.65 to 1.95	0.65 x V_{CC}		0.65 x V_{CC}		V
			2.3 to 2.7	1.7		1.7		
			2.7 to 3.6	2.0		2.0		
			4.5 to 5.5	0.7 x V_{CC}		0.7 x V_{CC}		
V_{IL}	Low-Level Input Voltage		1.65 to 1.95		0.35 x V_{CC}		0.35 x V_{CC}	V
			2.3 to 2.7		0.7		0.7	
			2.7 to 3.6		0.8		0.8	
			4.5 to 5.5		0.3 x V_{CC}		0.3 x V_{CC}	
V_{OH}	High-Level Output Voltage	V_I = V_{IH} or V_{IL} I_{OH} = −100 μA I_{OH} = −4 mA I_{OH} = −8 mA I_{OH} = −12 mA I_{OH} = −16 mA I_{OH} = −24 mA I_{OH} = −32 mA	 1.65 to 5.5 1.65 2.3 2.7 3.0 3.0 4.5	 V_{CC} − 0.1 1.2 1.8 2.2 2.4 2.2 3.8		 V_{CC} − 0.1 1.2 1.8 2.2 2.4 2.2 3.8		V
V_{OL}	Low-Level Output Voltage	V_I = V_{IH} or V_{IL} I_{OH} = −100 μA I_{OH} = −4 mA I_{OH} = −8 mA I_{OH} = −12 mA I_{OH} = −16 mA I_{OH} = −24 mA I_{OH} = −32 mA	 1.65 to 5.5 1.65 2.3 2.7 3.0 3.0 4.5		 0.1 0.45 0.6 0.4 0.4 0.55 0.6		 0.1 0.45 0.6 0.4 0.4 0.55 0.6	V
I_I	Input Leakage Current	V_I = 0 to 5.5 V	3.6		±5.0		±5.0	μA
I_{OZ}	3-State Output Leakage Current	V_I = V_{IH} or V_{IL}, V_O = 0 V to 5.5 V	3.6		±5.0		±5.0	μA
I_{OFF}	Power Off Leakage Current	V_I = 5.5 V or V_O = 5.5 V	0		10		10	μA
I_{CC}	Quiescent Supply Current	V_I = 5.5 V or GND	3.6		10		10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} − 0.6 V	2.3 to 3.6		500		500	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Share Feedback
Your Opinion Matters

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	V_{CC} (V)	T_A = −40 °C to +85 °C		T_A = −55 °C to +125 °C		Unit
				Min	Max	Min	Max	
f_{max}	Clock Pulse Frequency	See Figures 3 and 4 Waveform 1	1.65 to 1.95					MHz
			2.3 to 2.7					
			2.7					
			3.0 to 3.6	170		170		
			4.5 to 5.5					
t_{PLH}, t_{PHL}	Propagation Delay, CP_n to O_n	See Figures 3 and 4, Waveform 1	1.65 to 1.95		12.4		12.4	ns
			2.3 to 2.7		7.4		7.4	
			2.7		6.5		6.5	
			3.0 to 3.6		6.2		6.2	
			4.5 to 5.5		6.2		6.2	
t_{PZH}, t_{PZL}	Output Enable Time, $\overline{OE}_n$ to O_n	See Figures 3 and 4, Waveform 2	1.65 to 1.95		12.4		12.4	ns
			2.3 to 2.7		7.9		7.9	
			2.7		6.3		6.3	
			3.0 to 3.6		6.1		6.1	
			4.5 to 5.5		6.1		6.1	
t_{PHZ}, t_{PLZ}	Output Disable Time, $\overline{OE}_n$ to O_n	See Figures 3 and 4, Waveform 2	1.65 to 1.95		9.1		9.1	ns
			2.3 to 2.7		7.2		7.2	
			2.7		6.2		6.2	
			3.0 to 3.6		6.0		6.0	
			4.5 to 5.5		6.0		6.0	
t_s	Setup Time, High or Low D_n to CP_n	See Figures 3 and 4, Waveform 1	1.65 to 1.95	3.0		3.0		ns
			2.3 to 2.7	3.0		3.0		
			2.7	2.5		2.5		
			3.0 to 3.6	2.5		2.5		
			4.5 to 5.5	2.5		2.5		
t_h	Hold Time, High or Low D_n to CP_n	See Figures 3 and 4, Waveform 1	1.65 to 1.95	2.5		2.5		ns
			2.3 to 2.7	2.0		2.0		
			2.7	1.5		1.5		
			3.0 to 3.6	1.5		1.5		
			4.5 to 5.5	1.5		1.5		
t_w	CP_n Pulse Width, High	See Figures 3 and 4, Waveform 3	1.65 to 1.95	5.0		5.0		ns
			2.3 to 2.7	3.5		3.5		
			2.7	3.0		3.0		
			3.0 to 3.6	3.0		3.0		
			4.5 to 5.5	3.0		3.0		
t_{OSHL}, t_{OSLH}	Output to Output Skew (Note 5)		1.65 to 1.95					ns
			2.3 to 2.7					
			2.7					
			3.0 to 3.6		1.0		1.0	
			4.5 to 5.5					

5. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

Share Feedback
Your Opinion Matters

DYNAMIC SWITCHING CHARACTERISTICS

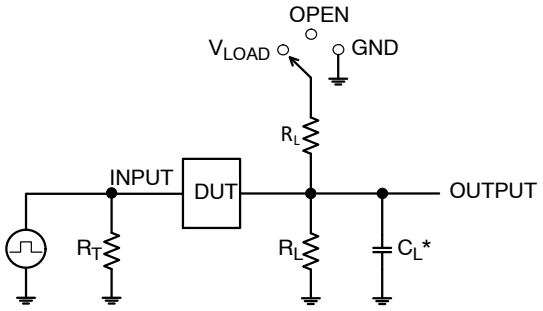
Symbol	Characteristic	Condition	T_A = +25 °C			Units
			Min	Typ	Max	
V_{OLP}	Dynamic LOW Peak Voltage (Note 6)	V_{CC} = 3.3 V, C_L = 50 pF, V_{IH} = 3.3 V, V_{IL} = 0 V V_{CC} = 2.5 V, C_L = 30 pF, V_{IH} = 2.5 V, V_{IL} = 0 V		0.8 0.6		V
V_{OLV}	Dynamic LOW Valley Voltage (Note 6)	V_{CC} = 3.3 V, C_L = 50 pF, V_{IH} = 3.3 V, V_{IL} = 0 V V_{CC} = 2.5 V, C_L = 30 pF, V_{IH} = 2.5 V, V_{IL} = 0 V		−0.8 −0.6		V

6. Number of outputs defined as “n”. Measured with “n−1” outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = 3.3 V, V_I = 0 V or V_{CC}	7	pF
C_{OUT}	Output Capacitance	V_{CC} = 3.3 V, V_I = 0 V or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	10 MHz, V_{CC} = 3.3 V, V_I = 0 V or V_{CC}	20	pF

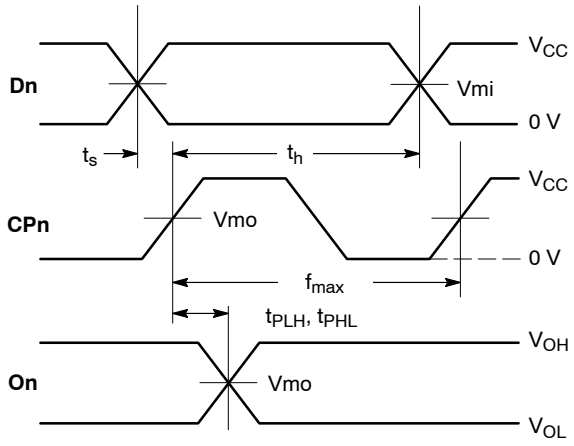
Share Feedback
Your Opinion Matters



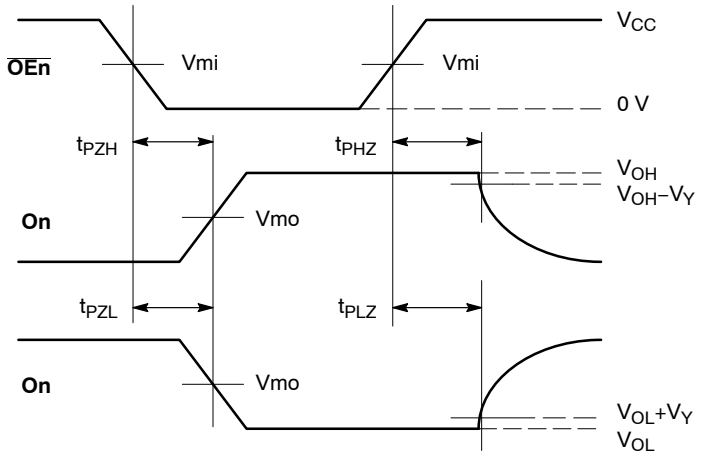
Test	Switch Position
t_{PLH} / t_{PHL}	Open
t_{PLZ} / t_{PZL}	V_{LOAD}
t_{PHZ} / t_{PZH}	GND

C_L includes probe and jig capacitance
R_T is Z_{OUT} of pulse generator (typically 50 Ω)
f = 1 MHz

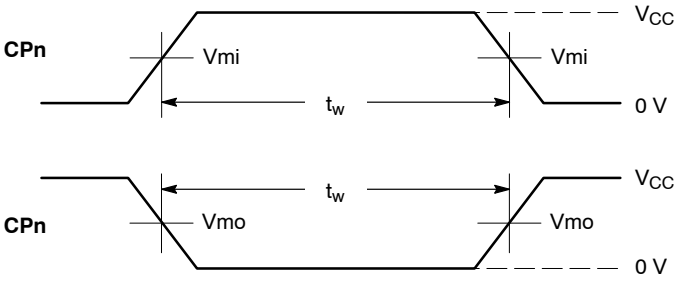
Figure 3. Test Circuit



WAVEFORM 1 – PROPAGATION DELAYS, SETUP AND HOLD TIMES
$t_R = t_F$ = 2.5 ns, 10% to 90%; f = 1 MHz; t_W = 500 ns



WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES
$t_R = t_F$ = 2.5 ns, 10% to 90%; f = 1 MHz; t_W = 500 ns



WAVEFORM 3 – PULSE WIDTH
$t_R = t_F$ = 2.5 ns (or fast as required) from 10% to 90%;
Output requirements: $V_{OL} \le 0.8$ V, $V_{OH} \ge 2.0$ V

Figure 4. AC Waveforms

V_{CC}, V	R_L, Ω	C_L, pF	V_{LOAD}	V_{mi}, V	V_{mo}, V	V_Y, V
1.65 to 1.95	500	30	2 x V_{CC}	V_{CC}/2	V_{CC}/2	0.15
2.3 to 2.7	500	30	2 x V_{CC}	V_{CC}/2	V_{CC}/2	0.15
2.7	500	50	6 V	1.5	1.5	0.3
3.0 to 3.6	500	50	6 V	1.5	1.5	0.3
4.5 to 5.5	500	50	2 x V_{CC}	V_{CC}/2	V_{CC}/2	0.3

Share Feedback
Your Opinion Matters

ORDERING INFORMATION

Device	Package	Shipping†
MC74LCX16374DTR2G	TSSOP-48 (Pb-Free)	2500 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Share Feedback
Your Opinion Matters

REVISION HISTORY

Revision	Description of Changes	Date
13	Revision to add Note 4 at the end of VIN and VOUT on Recommended operating conditions table + Updating AC ELECTRICAL CHARACTERISTICS Table	3/10/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

Share Feedback
Your Opinion Matters

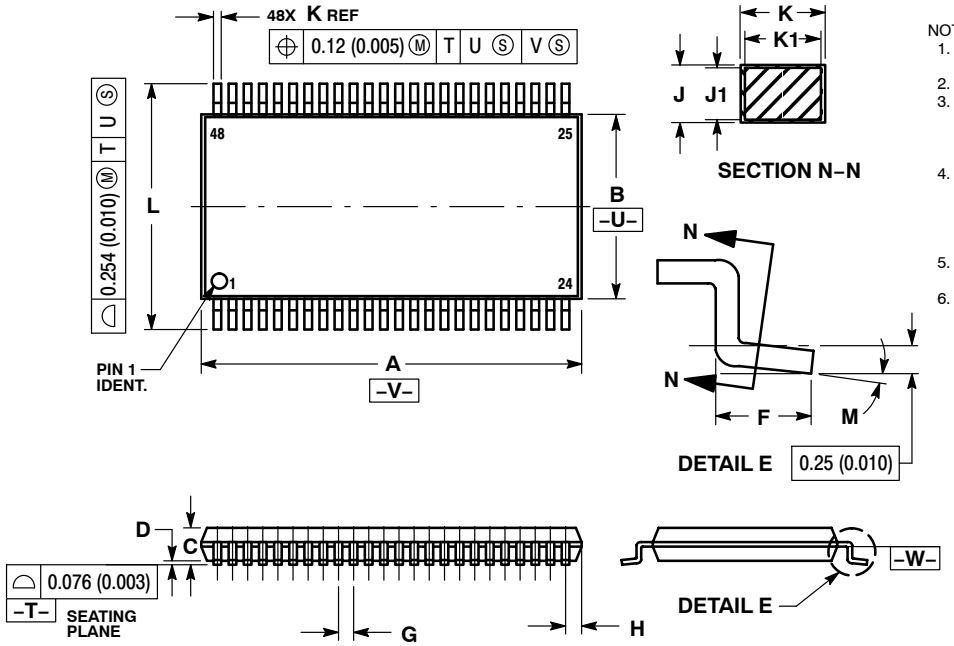


1

SCALE 1:1

TSSOP−48
CASE 1201
ISSUE B

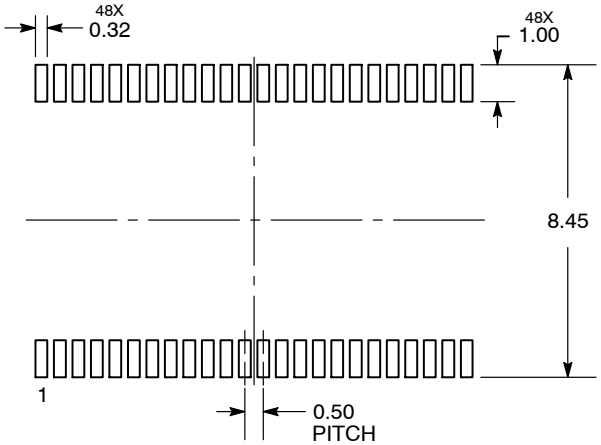
DATE 06 JUL 2010



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.40	12.60	0.488	0.496
B	6.00	6.20	0.236	0.244
C	−−−	1.10	−−−	0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.50 BSC		0.0197 BSC	
H	0.37	−−−	0.015	−−−
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.17	0.27	0.007	0.011
K1	0.17	0.23	0.007	0.009
L	7.95	8.25	0.313	0.325
M	0 °	8 °	0 °	8 °

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98ASH70297A**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**TSSOP−48**	**PAGE 1 OF 1**

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

onsemi, , and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as−is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales