MOSFET - Power, P-Channel, ChipFET

-20 V, 6.7 A

NTHS4101P

$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
−20 V	21 mΩ @ −4.5 V	−6.7 A
	30 mΩ @ −2.5 V	
	42 mΩ @ −1.8 V	

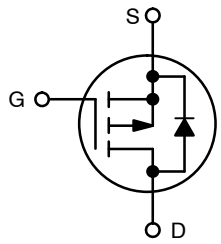
Features

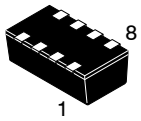
- Offers an Ultra Low $R_{DS(on)}$ Solution in the ChipFET Package
- Miniature ChipFET Package 40% Smaller Footprint than TSOP-6 making it an Ideal Device for Applications where Board Space is at a Premium
- Low Profile (<1.1 mm) Allows it to Fit Easily into Extremely Thin Environments such as Portable Electronics
- Designed to Provide Low $R_{DS(on)}$ at Gate Voltage as Low as 1.8 V, the Operating Voltage used in many Logic ICs in Portable Electronics
- Simplifies Circuit Design since Additional Boost Circuits for Gate Voltages are not Required
- Operated at Standard Logic Level Gate Drive, Facilitating Future Migration to Lower Levels using the same Basic Topology
- Pb-Free Package is Available

Applications

- Optimized for Battery and Load Management Applications in Portable Equipment such as MP3 Players, Cell Phones, Digital Cameras, Personal Digital Assistant and other Portable Applications
- Charge Control in Battery Chargers
- Buck and Boost Converters

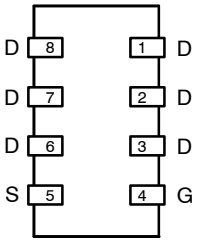
P−Channel MOSFET



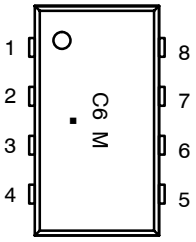


ChipFET
CASE 1206A
STYLE 1

PIN CONNECTIONS



MARKING DIAGRAM



C6 = Specific Device Code
M = Month Code
▪ = Pb-Free Package

MAXIMUM RATINGS (T_J = 25 °C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	−20	V_{dc}
Gate-to-Source Voltage − Continuous	V_{GS}	±8.0	V_{dc}
Drain Current − Continuous − 5 seconds	I_D I_D	−4.8 −6.7	A
Total Power Dissipation Continuous @ T_A = 25 °C (5 sec) @ T_A = 25 °C Continuous @ 85 °C (5 sec) @ 85 °C	P_D	 1.3 2.5 0.7 1.3	W
Pulsed Drain Current − t_p = 10 μs	I_{DM}	−190	A
Operating Junction and Storage Temperature Range	T_J, T_{STG}	−55 to +150	°C
Continuous Source Current	Is	−4.8	A
Thermal Resistance (Note 1) Junction-to-Ambient, 5 sec Junction-to-Ambient, Continuous	 $R_{\theta JA}$ $R_{\theta JA}$	 50 95	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.27 in sq [1 oz] including traces).

ORDERING INFORMATION

Device	Package	Shipping†
NTHS4101PT1	ChipFET	3000 / Tape & Reel
NTHS4101PT1G	ChipFET (Pb-Free)	3000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage (Note 2) Temperature Coefficient (Positive)	$V_{(Br)DSS}$	V_{GS} = 0 V_{dc}, I_D = −250 μA_{dc}	−20			V_{dc}
Gate-Body Leakage Current Zero	I_{GSS}	V_{DS} = 0 V_{dc}, V_{GS} = ±8.0 V_{dc}			±100	nA_{dc}
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −16 V_{dc}, V_{GS} = 0 V_{dc} V_{DS} = −16 V_{dc}, V_{GS} = 0 V_{dc}, T_J = 85 °C			−1.0 −5.0	μA_{dc}
ON CHARACTERISTICS (Note 2)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −250 μA_{dc}	−0.45		−1.5	V_{dc}
Static Drain-to-Source On-Resistance	$R_{DS(on)}$	V_{GS} = −4.5 V_{dc}, I_D = −4.8 A_{dc} V_{GS} = −2.5 V_{dc}, I_D = −4.2 A_{dc} V_{GS} = −1.8 V_{dc}, I_D = −1.0 A_{dc}		21 30 42	34 40 52	mΩ
Forward Transconductance	g_{FS}	V_{DS} = −5.0 V_{dc}, I_D = −4.8 A_{dc}		15		S
Diode Forward Voltage	V_{SD}	I_S = −4.8 A_{dc}, V_{GS} = 0 V_{dc}		−0.8	−1.2	V
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{iss}	V_{DS} = −16 V_{dc} V_{GS} = 0 V f = 1.0 MHz		2100		pF
Output Capacitance	C_{oss}			290		
Transfer Capacitance	C_{rss}			200		
SWITCHING CHARACTERISTICS (Note 3)						
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = −16 V_{dc} V_{GS} = −4.5 V_{dc} I_D = −4.5 A_{dc} R_G = 2.5 Ω		8.0		ns
Rise Time	t_r			28		
Turn-Off Delay Time	$t_{d(off)}$			75		
Fall Time	t_f			60		
Gate Charge	Q_g	V_{GS} = −4.5 V_{dc} I_D = −4.5 A_{dc} V_{DS} = −16 V_{dc} (Note 3)		25	35	nC
	Q_{gs}			4.0		
	Q_{gd}			7.0		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: Pulse Width = 250 μs, Duty Cycle = 2%.
3. Switching characteristics are independent of operating junction temperatures.

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TYPICAL PERFORMANCE CURVES (T_J = 25 °C unless otherwise noted)

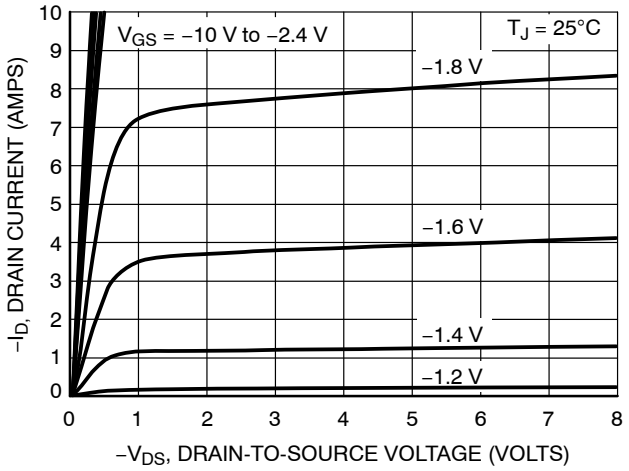


Figure 1. On-Region Characteristics

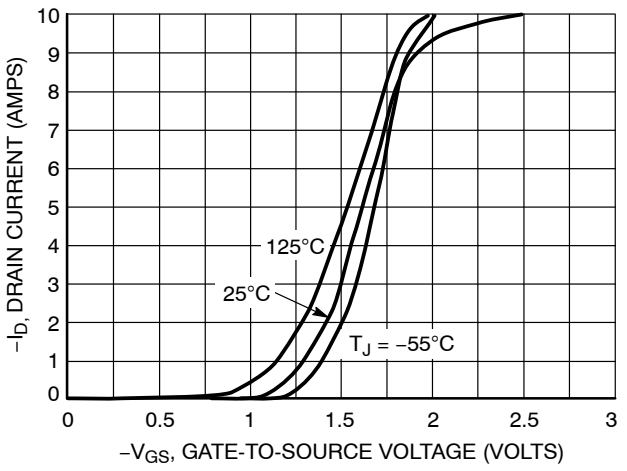


Figure 2. Transfer Characteristics

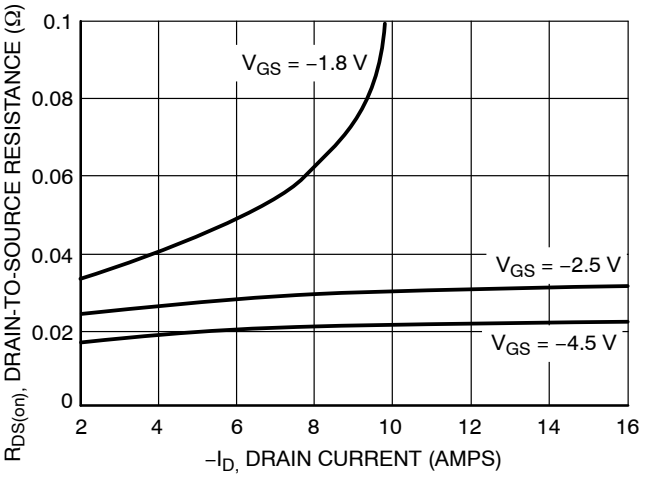


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

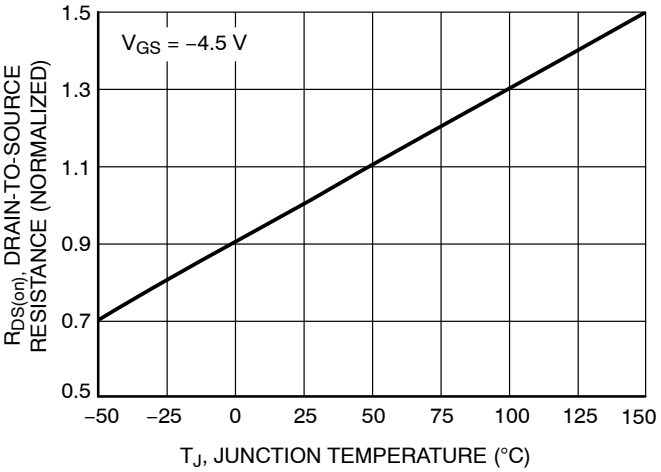


Figure 4. On-Resistance Variation with Temperature

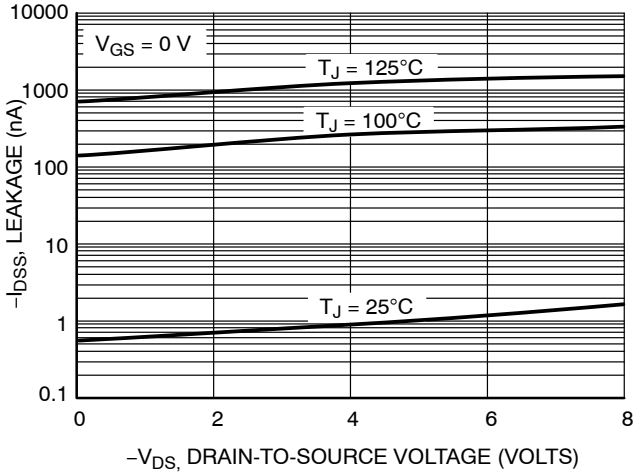


Figure 5. Drain-to-Source Leakage Current vs. Voltage

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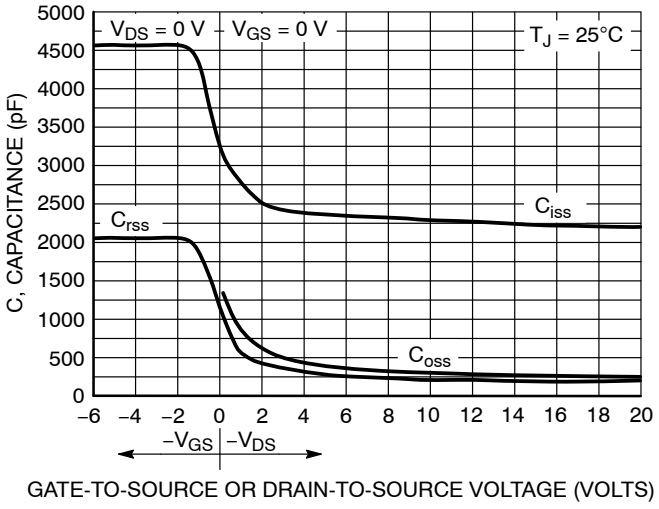


Figure 6. Capacitance Variation

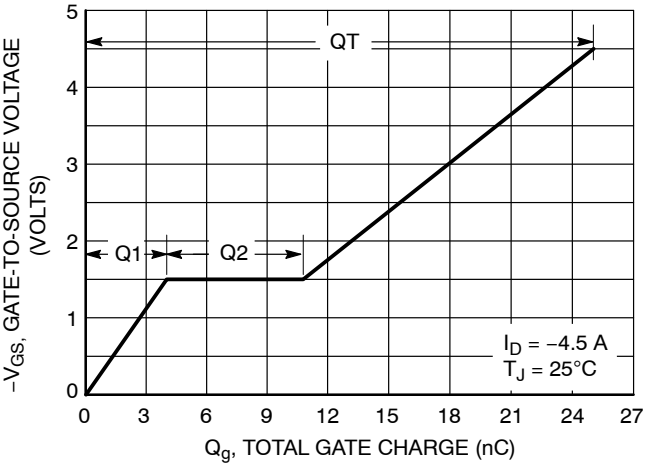


Figure 7. Gate-to-Source and Drain-to-Source Voltage vs. Total Gate Charge

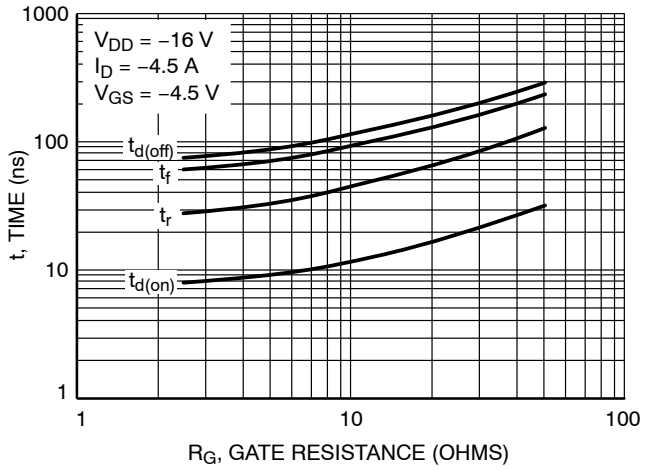


Figure 8. Resistive Switching Time Variation vs. Gate Resistance

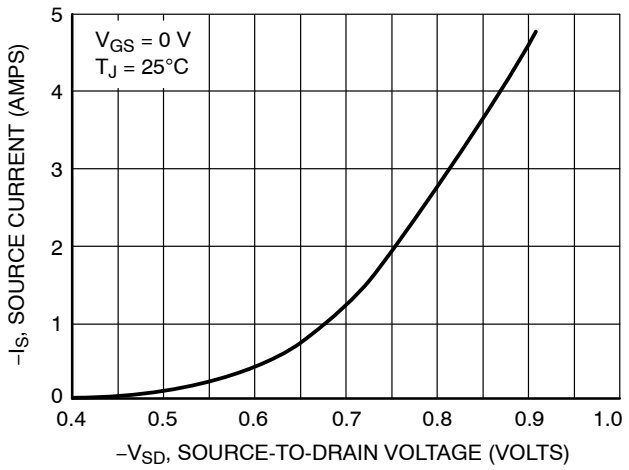


Figure 9. Diode Forward Voltage vs. Current

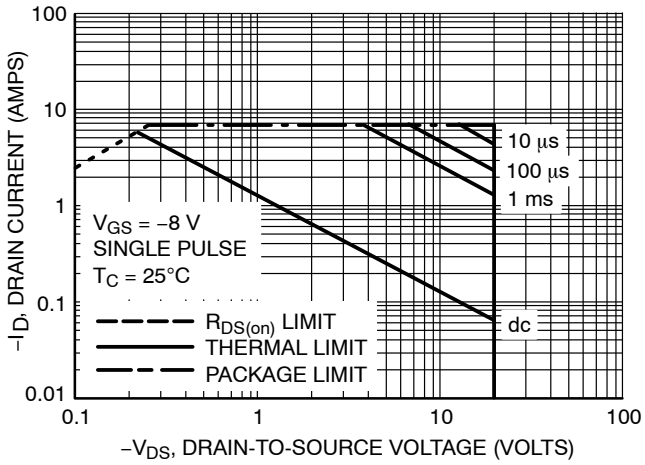


Figure 10. Maximum Rated Forward Biased Safe Operating Area

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REVISION HISTORY

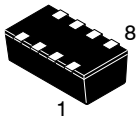
Revision	Description of Changes	Date
5	Rebranded the Data Sheet to **onsemi** format.	2/25/2025

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

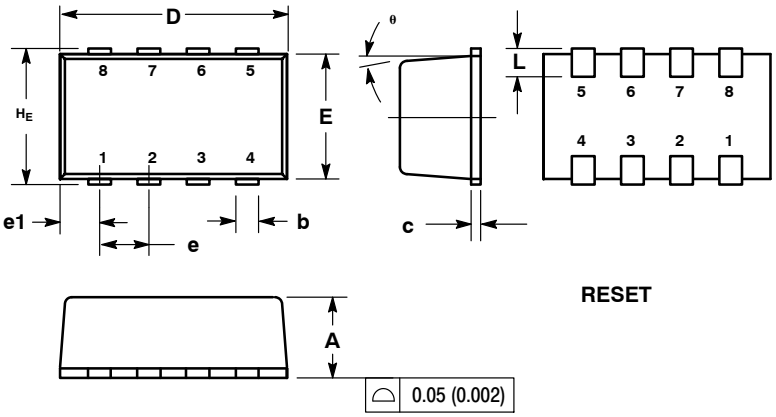
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ChipFET™
CASE1206A−03
ISSUE K

DATE 19 MAY 2009



SCALE 1:1



RESET

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	1.00	1.05	1.10	0.039	0.041	0.043
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	1.55	1.65	1.70	0.061	0.065	0.067
e		0.65 BSC			0.025 BSC	
e1		0.55 BSC			0.022 BSC	
L	0.28	0.35	0.42	0.011	0.014	0.017
H_E	1.80	1.90	2.00	0.071	0.075	0.079
θ		5° NOM			5° NOM	

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. GATE
5. SOURCE
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

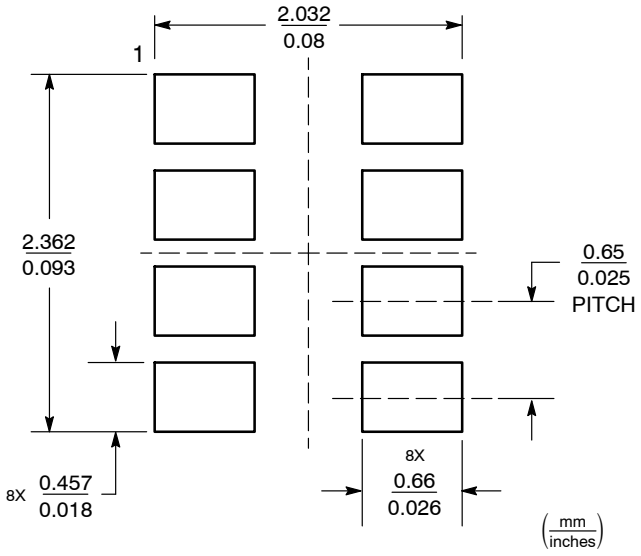
STYLE 3:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 4:
PIN 1. COLLECTOR
2. COLLECTOR
3. COLLECTOR
4. BASE
5. EMITTER
6. COLLECTOR
7. COLLECTOR
8. COLLECTOR

STYLE 5:
PIN 1. ANODE
2. ANODE
3. DRAIN
4. DRAIN
5. SOURCE
6. GATE
7. CATHODE
8. CATHODE

STYLE 6:
PIN 1. ANODE
2. DRAIN
3. DRAIN
4. GATE
5. SOURCE
6. DRAIN
7. DRAIN
8. CATHODE / DRAIN

SOLDERING FOOTPRINT



Basic Style

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Month Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

OPTIONAL SOLDERING FOOTPRINTS ON PAGE 2

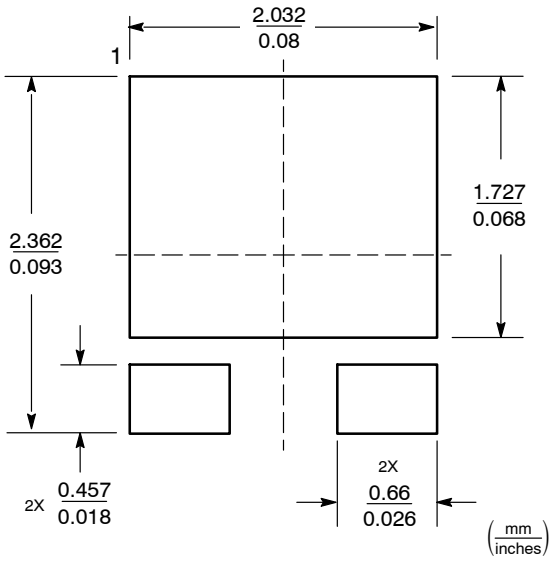
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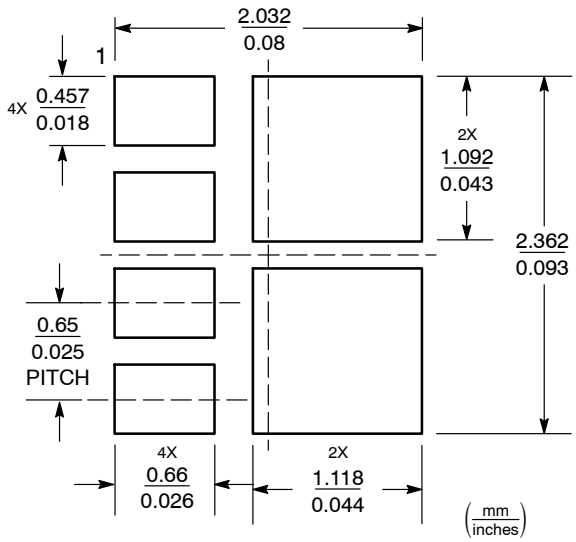
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CASE 1206A−03
ISSUE K

DATE 19 MAY 2009

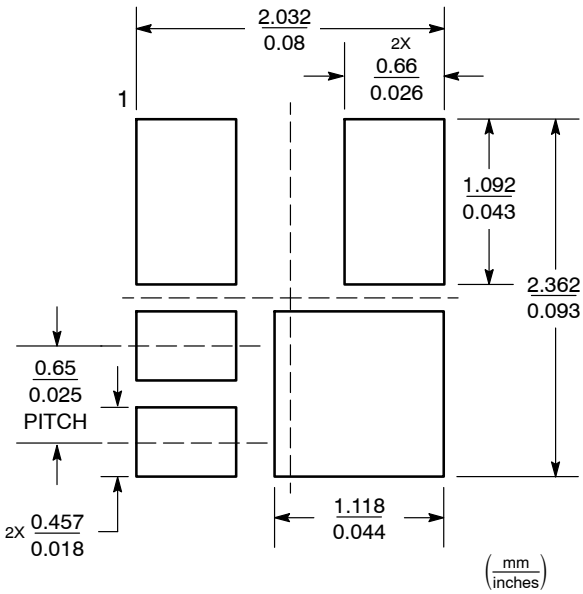
ADDITIONAL SOLDERING FOOTPRINTS*



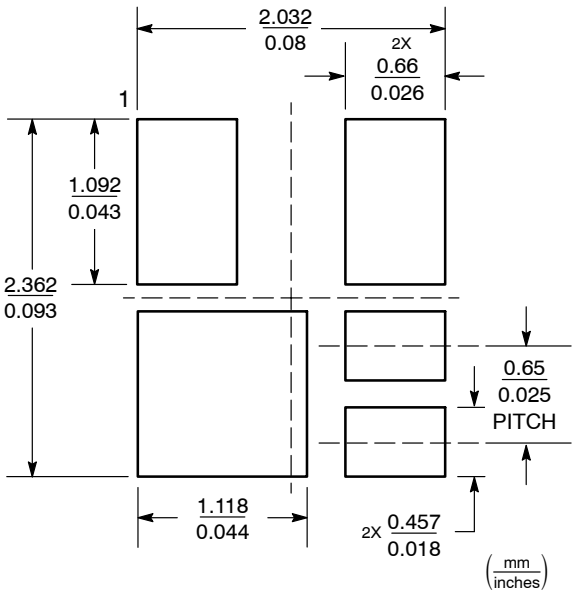
Styles 1 and 4



Style 2



Style 3



Style 5

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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