# Dual Matched General Purpose Transistor

## PNP Matched Pair

# NST65010MW6

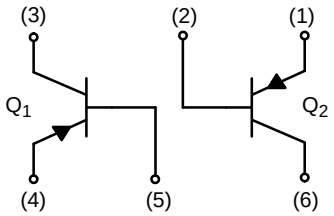
These transistors are housed in an ultra-small SOT-363 package ideally suited for portable products. They are assembled to create a pair of devices highly matched in all parameters, eliminating the need for costly trimming. Applications are Current Mirrors; Differential, Sense and Balanced Amplifiers; Mixers; Detectors and Limiters. Complementary NPN equivalent NST65011MW6T1G is available.

### Features

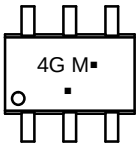
- Current Gain Matching to 10%
- Base-Emitter Voltage Matched to ≤ 2 mV
- Drop-In Replacement for Standard Device
- NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant




**SOT-363**
**CASE 419B**
**STYLE 1**




### MARKING DIAGRAMS




4G = Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

### MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Collector - Emitter Voltage | $V_{CEO}$ | −65 | V |
| Collector - Base Voltage | $V_{CBO}$ | −80 | V |
| Emitter - Base Voltage | $V_{EBO}$ | −5.0 | V |
| Collector Current − Continuous | $I_C$ | −100 | mAdc |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL CHARACTERISTICS

| Characteristic | Symbol | Max | Unit |
|---|---|---|---|
| Total Device Dissipation<br>Per Device<br>FR-5 Board (Note 1)<br>$T_A$ = 25 °C<br>Derate Above 25 °C | $P_D$ | 380<br>250<br><br><br>3.0 | mW<br><br><br><br>mW/°C |
| Thermal Resistance, Junction to Ambient | $R_{\theta JA}$ | 328 | °C/W |
| Junction and Storage Temperature Range | $T_J$, $T_{stg}$ | −55 to +150 | °C |

1. FR-5 = 1.0 x 0.75 x 0.062 in.

### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| NST65010MW6T1G | SOT-363 (Pb-Free) | 3000 / Tape & Reel |
| NSVT65010MW6T1G | SOT-363 (Pb-Free) | 3000 / Tape & Reel |

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25 °C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Collector - Emitter Breakdown Voltage, ($I_C$ = −10 mA) | $V_{(BR)CEO}$ | −65 | − | − | V |
| Collector - Emitter Breakdown Voltage, ($I_C$ = −10 μA, $V_{EB}$ = 0) | $V_{(BR)CES}$ | −80 | − | − | V |
| Collector - Base Breakdown Voltage, ($I_C$ = −10 μA) | $V_{(BR)CBO}$ | −80 | − | − | V |
| Emitter - Base Breakdown Voltage, ($I_E$ = −1.0 μA) | $V_{(BR)EBO}$ | −5.0 | − | − | V |
| Collector Cutoff Current ($V_{CB}$ = −30 V)<br>($V_{CB}$ = −30 V, $T_A$ = 150 °C) | $I_{CBO}$ | −<br>− | −<br>− | −15<br>−5.0 | nA<br>μA |
| **ON CHARACTERISTICS** | | | | | |
| DC Current Gain<br>($I_C$ = −10 μA, $V_{CE}$ = −5.0 V)<br>($I_C$ = −2.0 mA, $V_{CE}$ = −5.0 V)<br>($I_C$ = −2.0 mA, $V_{CE}$ = −5.0 V) (Note 2) | $h_{FE}$<br><br><br>$h_{FE(1)}/h_{FE(2)}$ | <br>−<br>220<br>0.9 | <br>150<br>290<br>1.0 | <br>−<br>475<br>1.1 | − |
| Collector - Emitter Saturation Voltage<br>($I_C$ = −10 mA, $I_B$ = −0.5 mA)<br>($I_C$ = −100 mA, $I_B$ = −5.0 mA) | $V_{CE(sat)}$ | <br>−<br>− | <br>−<br>− | <br>−300<br>−650 | mV |
| Base - Emitter Saturation Voltage<br>($I_C$ = −10 mA, $I_B$ = −0.5 mA)<br>($I_C$ = −100 mA, $I_B$ = −5.0 mA) | $V_{BE(sat)}$ | <br>−<br>− | <br>−700<br>−900 | <br>−<br>− | mV |
| Base - Emitter On Voltage<br>($I_C$ = −2.0 mA, $V_{CE}$ = −5.0 V)<br>($I_C$ = −10 mA, $V_{CE}$ = −5.0 V)<br>($I_C$ = −2.0 mA, $V_{CE}$ = −5.0 V) (Note 3) | $V_{BE(on)}$<br><br><br>$V_{BE(1)} - V_{BE(2)}$ | <br>−600<br>−<br>− | <br>−<br>−<br>−1.0 | <br>−750<br>−820<br>−2.0 | mV |
| **SMALL−SIGNAL CHARACTERISTICS** | | | | | |
| Current−Gain − Bandwidth Product, ($I_C$ = −10 mA, $V_{CE}$ = −5 Vdc, f = 100 MHz) | $f_T$ | 100 | − | − | MHz |
| Output Capacitance, ($V_{CB}$ = −10 V, f = 1.0 MHz) | $C_{ob}$ | − | − | 4.5 | pF |
| Noise Figure, ($I_C$ = −0.2 mA, $V_{CE}$ = −5 Vdc, $R_S$ = 2 kΩ, f = 1 kHz, BW = 200Hz) | NF | − | − | 10 | dB |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. $h_{FE(1)}/h_{FE(2)}$ is the ratio of one transistor compared to the other transistor within the same package. The smaller $h_{FE}$ is used as numerator.
3. $V_{BE(1)} - V_{BE(2)}$ is the absolute difference of one transistor compared to the other transistor within the same package.



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## TYPICAL CHARACTERISTICS

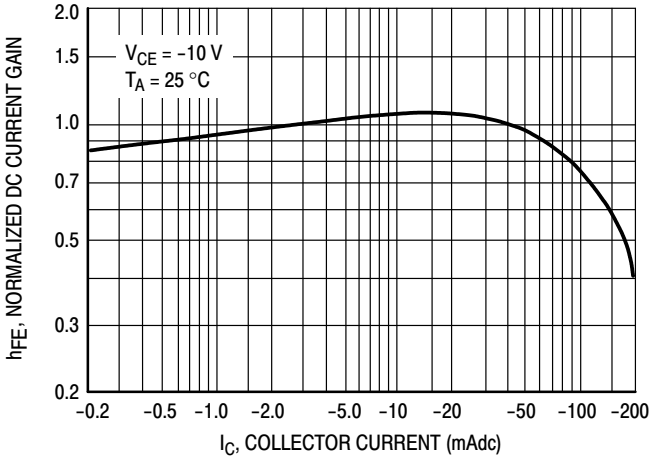



**Figure 1. Normalized DC Current Gain**

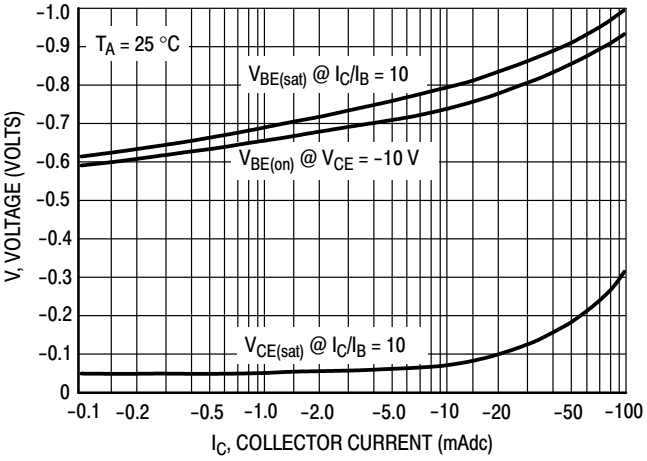



**Figure 2. “Saturation” and “On” Voltages**

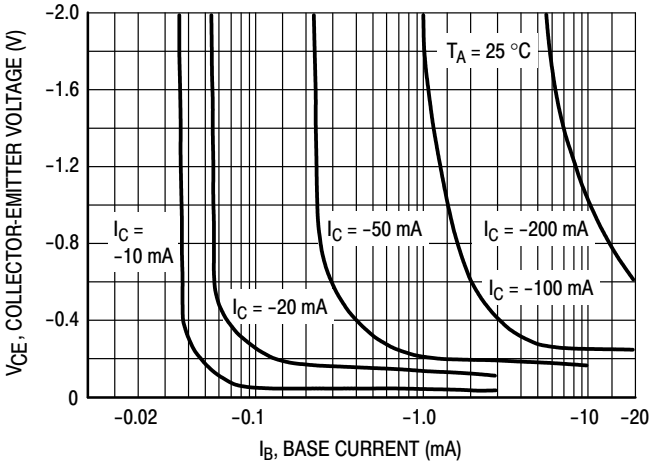



**Figure 3. Collector Saturation Region**

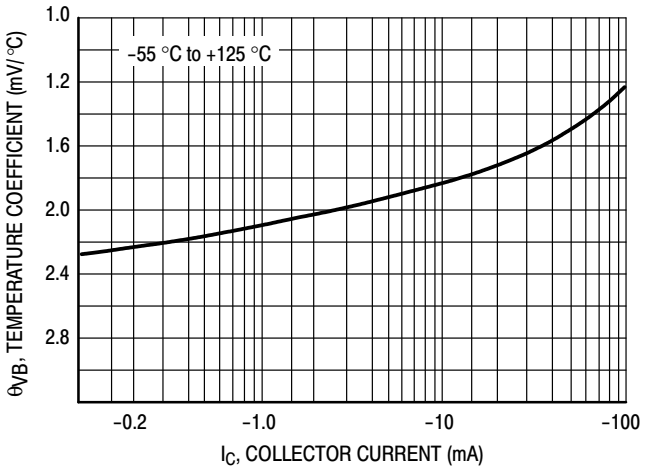



**Figure 4. Base-Emitter Temperature Coefficient**

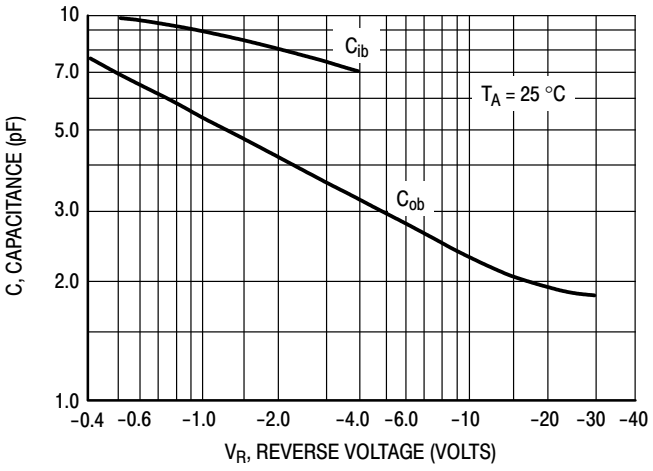



**Figure 5. Capacitances**

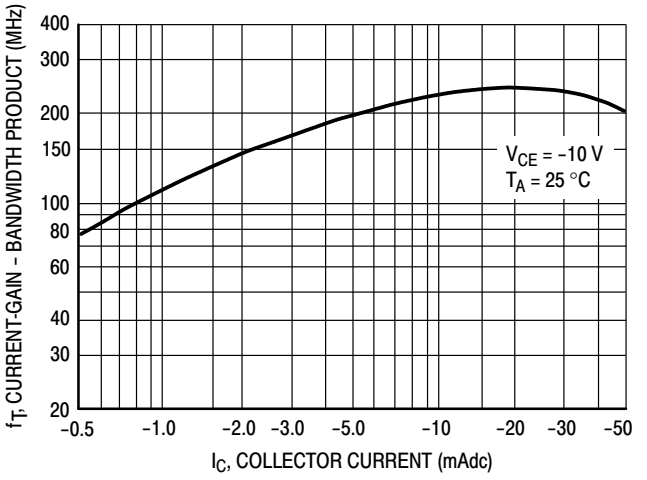



**Figure 6. Current−Gain − Bandwidth Product**



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## TYPICAL CHARACTERISTICS

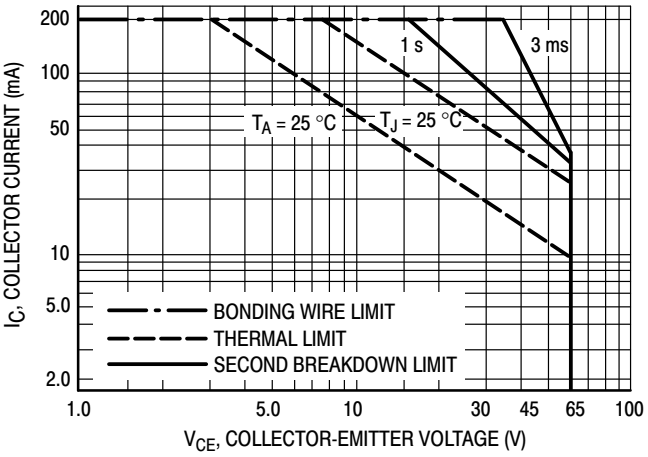



**Figure 7. Active Region Safe Operating Area**

The safe operating area curves indicate $I_C$−$V_{CE}$ limits of the transistor that must be observed for reliable operation. Collector load lines for specific circuits must fall below the limits indicated by the applicable curve.

The data of Figure 7 is based upon $T_{J(pk)}$ = 150 °C; $T_C$ or $T_A$ is variable depending upon conditions.



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## REVISION HISTORY

| Revision | Description of Changes | Date |
|---|---|---|
| 1 | Rebranded the Data Sheet to **onsemi** format. | 6/25/2025 |

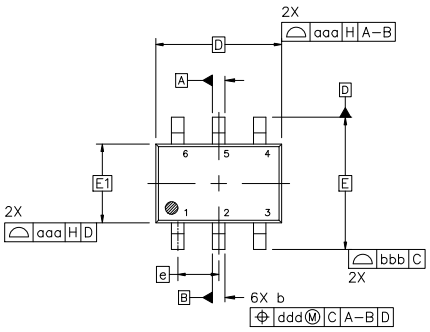


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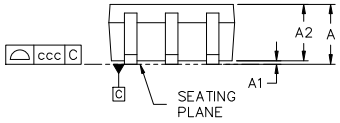


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CASE 419B−02
ISSUE Z

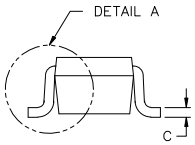
DATE 18 APR 2024



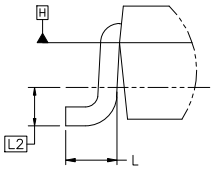

TOP VIEW




SIDE VIEW




END VIEW

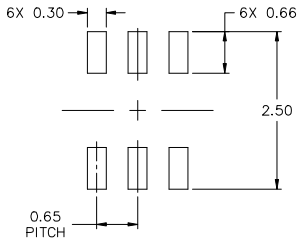



DETAIL A
SCALE 2:1

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

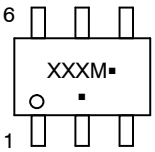
| | MILLIMETERS | | |
|---|---|---|---|
| DIM | MIN. | NOM. | MAX. |
| A | −−− | −−− | 1.10 |
| A1 | 0.00 | −−− | 0.10 |
| A2 | 0.70 | 0.90 | 1.00 |
| b | 0.15 | 0.20 | 0.25 |
| c | 0.08 | 0.15 | 0.22 |
| D | 2.00 BSC | | |
| E | 2.10 BSC | | |
| E1 | 1.25 BSC | | |
| e | 0.65 BSC | | |
| L | 0.26 | 0.36 | 0.46 |
| L2 | 0.15 BSC | | |
| aaa | 0.15 | | |
| bbb | 0.30 | | |
| ccc | 0.10 | | |
| ddd | 0.10 | | |




RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

## GENERIC MARKING DIAGRAM*




XXX = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

**STYLES ON PAGE 2**

| | | | |
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CASE 419B−02
ISSUE Z

DATE 18 APR 2024

STYLE 1:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 2:
CANCELLED

STYLE 3:
CANCELLED

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. COLLECTOR
4. EMITTER
5. BASE
6. ANODE

STYLE 5:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 6:
PIN 1. ANODE 2
2. N/C
3. CATHODE 1
4. ANODE 1
5. N/C
6. CATHODE 2

STYLE 7:
PIN 1. SOURCE 2
2. DRAIN 2
3. GATE 1
4. SOURCE 1
5. DRAIN 1
6. GATE 2

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. EMITTER 2
2. EMITTER 1
3. COLLECTOR 1
4. BASE 1
5. BASE 2
6. COLLECTOR 2

STYLE 10:
PIN 1. SOURCE 2
2. SOURCE 1
3. GATE 1
4. DRAIN 1
5. DRAIN 2
6. GATE 2

STYLE 11:
PIN 1. CATHODE 2
2. CATHODE 2
3. ANODE 1
4. CATHODE 1
5. CATHODE 1
6. ANODE 2

STYLE 12:
PIN 1. ANODE 2
2. ANODE 2
3. CATHODE 1
4. ANODE 1
5. ANODE 1
6. CATHODE 2

STYLE 13:
PIN 1. ANODE
2. N/C
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 14:
PIN 1. VREF
2. GND
3. GND
4. IOUT
5. VEN
6. VCC

STYLE 15:
PIN 1. ANODE 1
2. ANODE 2
3. ANODE 3
4. CATHODE 3
5. CATHODE 2
6. CATHODE 1

STYLE 16:
PIN 1. BASE 1
2. EMITTER 2
3. COLLECTOR 2
4. BASE 2
5. EMITTER 1
6. COLLECTOR 1

STYLE 17:
PIN 1. BASE 1
2. EMITTER 1
3. COLLECTOR 2
4. BASE 2
5. EMITTER 2
6. COLLECTOR 1

STYLE 18:
PIN 1. VIN1
2. VCC
3. VOUT2
4. VIN2
5. GND
6. VOUT1

STYLE 19:
PIN 1. I OUT
2. GND
3. GND
4. V CC
5. V EN
6. V REF

STYLE 20:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 21:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. N/C
6. CATHODE 1

STYLE 22:
PIN 1. D1 (i)
2. GND
3. D2 (i)
4. D2 (c)
5. VBUS
6. D1 (c)

STYLE 23:
PIN 1. Vn
2. CH1
3. Vp
4. N/C
5. CH2
6. N/C

STYLE 24:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 25:
PIN 1. BASE 1
2. CATHODE
3. COLLECTOR 2
4. BASE 2
5. EMITTER
6. COLLECTOR 1

STYLE 26:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 27:
PIN 1. BASE 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. EMITTER 2
6. COLLECTOR 2

STYLE 28:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 29:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE/ANODE
6. CATHODE

STYLE 30:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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