Linear Regulator – High Accuracy, Low Dropout, Power Good Function

500 mA

NCV8537

The NCV8537 is a high performance low dropout linear voltage regulator. Based on the popular NCV8535, the device retains all the best features of its predecessor which includes high accuracy, excellent stability, low noise performance and reverse bias protection but now includes a Power Good output signal to enable monitoring of the supply system. The device is available with fixed or adjustable outputs and is packaged in a 10 pin 3x3 mm DFN package.

Features

- High Accuracy Output Over Line and Load Variances (±0.9% at 25 °C)
- Operating Temperature Range: −40 °C to 125 °C
- Power Good Output to Indicate the Regulator is Within Specified Limits
- Stable Output with Low Value Capacitors of any type and with no Minimum Load Current Requirement
- Incorporates Current Limiting and Reverse Bias Protection
- Thermal Shutdown Protection
- Low Dropout Voltage at Full Load (340 mV typ at V_o = 3.3 V)
- Low Noise (33 μVrms w/ 10 nF C_{nr} and 52 μVrms w/out C_{nr})
- Low Shutdown Current (< 1 mA)
- Reverse Bias Protected
- 2.9 V to 12 V Supply Range
- Available in 1.8 V, 2.5 V, 3.3 V, 5.0 V and Adjustable Output Voltages
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These are Pb-Free Devices

Applications

- Networking Systems, DSL/Cable Modems
- Audio Systems for Automotive Applications
- Navigation Systems
- Satellite Receivers



DFN10
CASE 485C



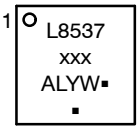
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PIN CONFIGURATION

Pin 1, 2. V_{out}
3. Sense / ADJ
4. GND
5. PWRG
6. NC
7. NR
8. $\overline{SD}$
9, 10. V_{in}
EP, GND

MARKING DIAGRAM





V8537 = Specific Device Code
L8537 = Specific Device Code
xxx = ADJ, 180, 250, 330, 500
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 15 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 15.

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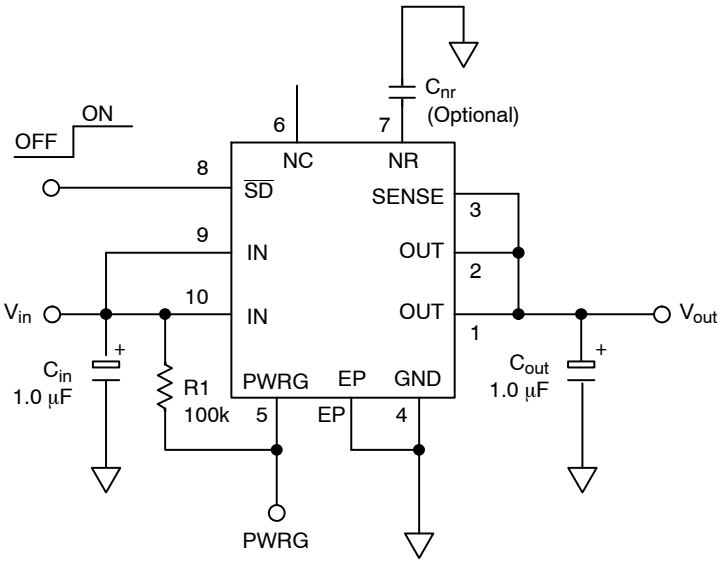


Figure 1. Typical Fixed Version Application Schematic

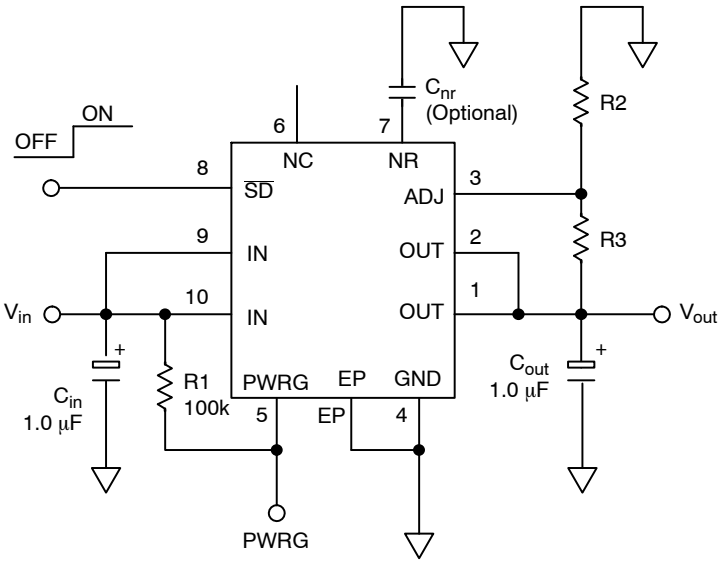


Figure 2. Typical Adjustable Version Application Schematic

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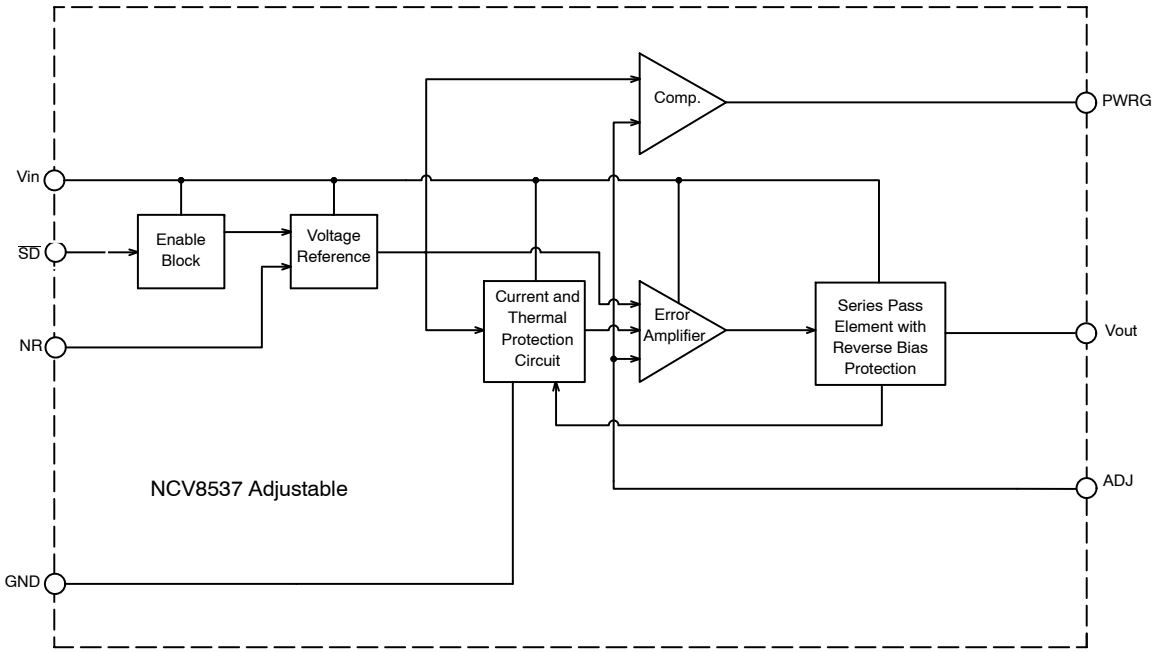


Figure 3. Block Diagram, Adjustable Output Version

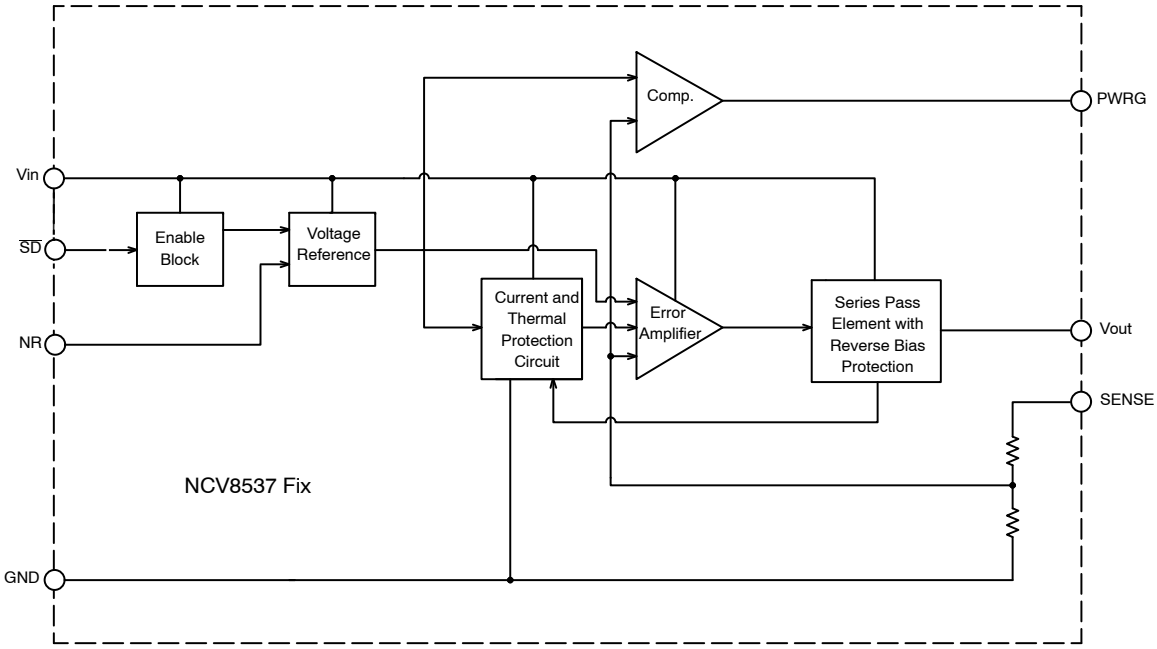


Figure 4. Block Diagram, Fixed Output Version

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PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1, 2	V_{out}	Regulated output voltage. Bypass to ground with $C_{out} \geq 1.0\ \mu F$
3	SENSE/ADJ	For output voltage sensing, connect to Pins 1 and 2.at Fixed output Voltage version Adjustable pin at Adjustable output version
4	GND	Power Supply Ground
5	PWRG	Power Good
6	NC	Not Connected
7	NR	Noise Reduction Pin. This is an optional pin used to further reduce noise.
8	$\overline{SD}$	Shutdown pin. When not in use, this pin should be connected to the input pin.
9, 10	V_{in}	Power Supply Input Voltage
EPAD	EPAD	Exposed thermal pad should be connected to ground.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage	V_{in}	−0.3 to +16	V
Output Voltage	V_{out}	−0.3 to V_{in} +0.3 or 10 V*	V
PWRG Pin Voltage	V_{PWRG}	−0.3 to +16	V
Shutdown Pin Voltage	V_{sh}	−0.3 to +16	V
Junction Temperature Range	T_J	−40 to +150	°C
Storage Temperature Range	T_{stg}	−50 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected. Operating the device outside its recommended conditions, but still within its maximum rated limits may not cause immediate damage. However, doing so can lead to reduced performance, unpredictable behavior, and potentially shorten the device's lifespan or reliability.

NOTE: This device series contains ESD protection and exceeds the following tests:
Human Body Model (HBM) tested per AEC-Q100-002 (EIA/JESD22-A114)
Machine Model (MM) tested per AEC-Q100-003 (EIA/JESD22-A115)
Charged Device Model (CDM) tested per EIA/JESD22-C101.

* Which ever is less. Reverse bias protection feature valid only if ($V_{out} - V_{in}$) ≤ 7 V.

THERMAL CHARACTERISTICS

Characteristic	Test Conditions (Typical Value)		Unit
	Min Pad Board (Note 1)	**1″ Pad Board** (Note 1)	
Junction-to-Air, θJA	215	66	°C/W
Junction-to-Pin, J−L4	58	18	°C/W

1. As mounted on a 35 x 35 x 1.5 mm FR4 Substrate, with a single layer of a specified copper area of 2 oz (0.07 mm thick) copper traces and heat spreading area. JEDEC 51 specifications for a low and high conductivity test board recommend a 2 oz copper thickness. Test conditions are under natural convection or zero air flow.

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ELECTRICAL CHARACTERISTICS – 1.8 V

(V_{out} = 1.8 V typical, V_{in} = 2.9 V, T_A = −40 °C to +125 °C, unless otherwise noted, Note 2)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (Accuracy) V_{in} = 2.9 V to 5.8 V, I_{load} = 0.1 mA to 500 mA, T_A = 25 °C	V_{out}	−0.9% 1.783	1.8	+0.9% 1.817	V
Output Voltage (Accuracy) V_{in} = 2.9 V to 5.8 V, I_{load} = 0.1 mA to 500 mA, T_A = 0 °C to +85 °C	V_{out}	−1.4% 1.774	1.8	+1.4% 1.826	V
Output Voltage (Accuracy) V_{in} = 2.9 V to 5.8 V, I_{load} = 0.1 mA to 500 mA, T_A = −40 °C to +125 °C	V_{out}	−1.5% 1.773	1.8	+1.5% 1.827	V
Minimum Input Voltage	V_{inmin}		2.9		V
Line Regulation V_{in} = 2.9 V to 12 V, I_{load} = 0.1 mA	$Line_{Reg}$		0.04		mV/V
Load Regulation V_{in} = 2.9 V, I_{load} = 0.1 mA to 500 mA	$Load_{Reg}$		0.04		mV/mA
Dropout Voltage (See Figure 9) I_{load} = 500 mA (Notes 3, 4) I_{load} = 300 mA (Notes 3, 4) I_{load} = 50 mA (Notes 3, 4)	V_{DO}		 620 230 95		mV
Peak Output Current (See Figures 14 and 17)	I_{pk}	500	700	830	mA
Short Output Current (See Figure 14) V_{in} < 7 V, T_A = 25 °C	I_{sc}			900	mA
Thermal Shutdown / Hysteresis	T_J		160/10		°C
Ground Current In Regulation I_{load} = 500 mA (Note 3) I_{load} = 300 mA (Note 3) I_{load} = 50 mA I_{load} = 0.1 mA In Dropout V_{in} = 2.2 V, I_{load} = 0.1 mA In Shutdown V_{SD} = 0 V	I_{GND} I_{GNDsh}		 9.0 4.6 0.8 – 	 14 7.5 2.5 220 500 1.0	 mA µA µA µA
Output Noise C_{nr} = 0 nF, I_{load} = 500 mA, f = 10 Hz to 100 kHz, C_{out} = 10 µF C_{nr} = 10 nF, I_{load} = 500 mA, f = 10 Hz to 100 kHz, C_{out} = 10 µF	V_{noise}		 52 33		 µVrms µVrms
Power Good Voltage Low Threshold Hysteresis High Threshold	V_{elft}	 93	 95 2 97	 99	% of V_{out}
Power Good Pin Voltage Saturation (I_{ef} – 1.0 mA)	V_{efdo}		200		mV
Power Good Pin Leakage	I_{efleak}		1.0		µA
Power Good Blanking Time (Note 7)	t_{ef}		50		µs
Shutdown Threshold Voltage ON Threshold Voltage OFF	V_{SD}	 2.0		 0.4	 V V
SD Input Current, V_{SD} = 0 V to 0.4 V or V_{SD} = 2.0 V to V_{in}	I_{SD}		0.07	1.0	µA
Output Current In Shutdown Mode, V_{out} = 0 V	I_{OSD}		0.07	1.0	µA
Reverse Bias Protection, Current Flowing from the Output Pin to GND (V_{in} = 0 V, V_{out_forced} = 1.8 V)	I_{OUTR}		10		µA

2. Performance guaranteed over the operating temperature range by design and/or characterization, production tested at $T_J = T_A$ = 25 °C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
3. T_A must be greater than 0 °C.
4. Maximum dropout voltage is limited by minimum input voltage V_{in} = 2.9 V recommended for guaranteed operation.

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ELECTRICAL CHARACTERISTICS – 2.5 V

(V_{out} = 2.5 V typical, V_{in} = 2.9 V, T_A = −40 °C to +125 °C, unless otherwise noted, Note 5)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (Accuracy) V_{in} = 2.9 V to 6.5 V, I_{load} = 0.1 mA to 500 mA, T_A = 25 °C	V_{out}	−0.9% 2.477	2.5	+0.9% 2.523	V
Output Voltage (Accuracy) V_{in} = 2.9 V to 6.5 V, I_{load} = 0.1 mA to 500 mA, T_A = 0°C to +85 °C	V_{out}	−1.4% 2.465	2.5	+1.4% 2.535	V
Output Voltage (Accuracy) V_{in} = 2.9 V to 6.5 V, I_{load} = 0.1 mA to 500 mA, T_A = −40°C to +125 °C	V_{out}	−1.5% 2.462	2.5	+1.5% 2.538	V
Minimum Input Voltage	V_{inmin}		2.9		V
Line Regulation V_{in} = 2.9 V to 12 V, I_{load} = 0.1 mA	$Line_{Reg}$		0.04		mV/V
Load Regulation V_{in} = 2.9 V, I_{load} = 0.1 mA to 500 mA	$Load_{Reg}$		0.04		mV/mA
Dropout Voltage (See Figure 10) I_{load} = 500 mA (Note 6) I_{load} = 300 mA (Note 6) I_{load} = 50 mA I_{load} = 0.1mA	V_{DO}		 340 230 110 10		mV
Peak Output Current (See Figures 14 and 18)	I_{pk}	500	700	800	mA
Short Output Current (See Figure 14) V_{in} < 7 V, T_A = 25 °C	I_{sc}			900	mA
Thermal Shutdown / Hysteresis	T_J		160/10		°C
Ground Current In Regulation I_{load} = 500 mA (Note 6) I_{load} = 300 mA (Note 6) I_{load} = 50 mA I_{load} = 0.1 mA In Dropout V_{in} = 2.4 V, I_{load} = 0.1 mA In Shutdown V_{SD} = 0 V	I_{GND} I_{GNDsh}		 9.0 4.6 0.8 – 	 14 7.5 2.5 220 500 1.0	 mA µA µA µA
Output Noise C_{nr} = 0 nF, I_{load} = 500 mA, f = 10 Hz to 100 kHz, C_{out} = 10 µF C_{nr} = 10 nF, I_{load} = 500 mA, f = 10 Hz to 100 kHz, C_{out} = 10 µF	V_{noise}		 56 35		 µVrms µVrms
Power Good Voltage Low Threshold Hysteresis High Threshold	V_{elft}	 93	 95 2 97	 99	% of V_{out}
Power Good Pin Voltage Saturation (I_{ef} – 1.0 mA)	V_{efdo}		200		mV
Power Good Pin Leakage	I_{efleak}		1.0		µA
Power Good Blanking Time (Note 7)	t_{ef}		50		µs
Shutdown Threshold Voltage ON Threshold Voltage OFF	V_{SD}	 2.0		 0.4	 V V
S_D Input Current, V_{SD} = 0 V to 0.4 V or V_{SD} = 2.0 V to V_{in}	I_{SD}		0.07	1.0	µA
Output Current In Shutdown Mode, V_{out} = 0 V	I_{OSD}		0.07	1.0	µA
Reverse Bias Protection, Current Flowing from the Output Pin to GND (V_{in} = 0 V, V_{out_forced} = 2.5 V)	I_{OUTR}		10		µA

5. Performance guaranteed over the operating temperature range by design and/or characterization, production tested at $T_J = T_A$ = 25 °C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
6. T_A must be greater than 0 °C.
7. Can be disabled per customer request.

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ELECTRICAL CHARACTERISTICS – 3.3 V

(V_{out} = 3.3 V typical, V_{in} = 3.7 V, T_A = −40 °C to +125 °C, unless otherwise noted, Note 8)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (Accuracy) V_{in} V_{in} = 3.7 V to 7.3 V, I_{load} = 0.1 mA to 500 mA, T_A = 25 °C	V_{out}	−0.90% 3.27	3.3	0.90% 3.33	V
Output Voltage (Accuracy) V_{in} = 3.7 V to 7.3 V, I_{load} = 0.1 mA to 500 mA, T_A = 0 °C to +85 °C	V_{out}	−1.40% 3.254	3.3	1.40% 3.346	V
Output Voltage (Accuracy) V_{in} = 3.7 V to 7.3 V, I_{load} = 0.1 mA to 500 mA, T_A = −40 °C to +125 °C	V_{out}	−1.50% 3.25	3.3	1.50% 3.35	V
Line Regulation V_{in} = 3.7 V to 12 V, I_{load} = 0.1 mA	$Line_{Reg}$		0.04		mV/V
Load Regulation V_{in} = 3.7 V, I_{load} = 0.1 mA to 500 mA	$Load_{Reg}$		0.04		mV/mA
Dropout Voltage I_{load} = 500 mA I_{load} = 300 mA I_{load} = 50 mA I_{load} = 0.1 mA	V_{DO}		 340 230 110 10		mV
Peak Output Current (See Figure 14)	I_{pk}	500	700	800	mA
Short Output Current (See Figure 14) V_{in} < 7 V, T_A = 25 °C	I_{sc}			900	mA
Thermal Shutdown / Hysteresis	T_J		160/10		°C
Ground Current In Regulation I_{load} = 500 mA (Note 8) I_{load} = 300 mA I_{load} = 50 mA I_{load} = 0.1 mA In Dropout V_{in} = 3.7 V, I_{load} = 0.1 mA In Shutdown V_{SD} = 0 V	I_{GND} I_{GNDsh}		 9 4.6 0.8 – 	 14 7.5 2.5 220 500 1	 mA μA μA μA
Output Noise C_{nr} = 0 nF, I_{load} = 500 mA, f = 10 Hz to 100 kHz, C_{out} = 10 μF C_{nr} = 10 nF, I_{load} = 500 mA, f = 10 Hz to 100 kHz, C_{out} = 10 μF	V_{noise}		 69 46		μVrms
Power Good Voltage Low Threshold Hysteresis High Threshold	V_{elft}	 93	 95 2 97	 99	% of V_{out}
Power Good Pin Voltage Saturation (I_{ef} = 1.0 mA)	V_{efdo}		200		mV
Power Good Pin Leakage	I_{efleak}		1		μA
Power Good Blanking Time (Note 9)	t_{ef}		50		μs
Shutdown Threshold Voltage ON Threshold Voltage OFF	V_{SD}	 2		 0.4	V
SD Input Current, V_{SD} = 0 V to 0.4 V or V_{SD} = 2.0 V to V_{in}	I_{SD}		0.07	1	μA
Output Current In Shutdown Mode, V_{out} = 0 V	I_{OSD}		0.07	1	μA
Reverse Bias Protection, Current Flowing from the Output Pin to GND (V_{in} = 0 V, V_{out_forced} = 3.3 V)	I_{OUTR}		10		μA

8. Performance guaranteed over the operating temperature range by design and/or characterization, production tested at $T_J = T_A$ = 25 °C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
9. Can be disabled per customer request.

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ELECTRICAL CHARACTERISTICS – 5 V

(V_{out} = 5.0 V typical, V_{in} = 5.4 V, T_A = −40 °C to +125 °C, unless otherwise noted, Note 10)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (Accuracy) V_{in} V_{in} = 5.4 V to 7.3 V, I_{load} = 0.1 mA to 500 mA, T_A = 25 °C	V_{out}	−0.90% 4.955	5	0.90% 5.045	V
Output Voltage (Accuracy) V_{in} = 5.4 V to 7.3 V, I_{load} = 0.1 mA to 500 mA, T_A = 0 °C to +85 °C	V_{out}	−1.40% 4.93	5	1.40% 5.07	V
Output Voltage (Accuracy) V_{in} = 5.4 V to 7.3 V, I_{load} = 0.1 mA to 500 mA, T_A = −40 °C to +125 °C	V_{out}	−1.50% 4.925	5	1.50% 5.075	V
Line Regulation V_{in} = 5.4 V to 12 V, I_{load} = 0.1 mA	$Line_{Reg}$		0.04		mV/V
Load Regulation V_{in} = 5.4 V, I_{load} = 0.1 mA to 500 mA	$Load_{Reg}$		0.04		mV/mA
Dropout Voltage I_{load} = 500 mA I_{load} = 300 mA I_{load} = 50 mA I_{load} = 0.1 mA	V_{DO}			 340 230 110 10	mV
Peak Output Current (See Figure 14)	I_{pk}	500	700	830	mA
Short Output Current (See Figure 14) V_{in} < 7 V, T_A = 25 °C	I_{sc}			930	mA
Thermal Shutdown / Hysteresis	T_J		160/10		°C
Ground Current In Regulation I_{load} = 500 mA (Note 10) I_{load} = 300 mA I_{load} = 50 mA I_{load} = 0.1 mA In Dropout V_{in} = 3.2 V, I_{load} = 0.1 mA In Shutdown V_{SD} = 0 V	I_{GND} I_{GNDsh}		 9 4.6 0.8 – 	 14 7.5 2.5 220 500 1	 mA μA μA μA
Output Noise C_{nr} = 0 nF, I_{load} = 500 mA, f = 10 Hz to 100 kHz, C_{out} = 10 μF C_{nr} = 10 nF, I_{load} = 500 mA, f = 10 Hz to 100 kHz, C_{out} = 10 μF	V_{noise}		 93 58		μVrms
Power Good Voltage Low Threshold Hysteresis High Threshold	V_{elft}	 93	 95 2 97	 99	% of V_{out}
Power Good Pin Voltage Saturation (I_{ef} = 1.0 mA)	V_{efdo}		200		mV
Power Good Pin Leakage	I_{efleak}		1		μA
Power Good Blanking Time (Note 11)	t_{ef}		50		μs
Shutdown Threshold Voltage ON Threshold Voltage OFF	V_{SD}	 2		 0.4	V
SD Input Current, V_{SD} = 0 V to 0.4 V or V_{SD} = 2.0 V to V_{in}	I_{SD}		0.07	1	μA
Output Current In Shutdown Mode, V_{out} = 0 V	I_{OSD}		0.07	1	μA
Reverse Bias Protection, Current Flowing from the Output Pin to GND (V_{in} = 0 V, V_{out_forced} = 5 V)	I_{OUTR}		10		μA

10. Performance guaranteed over the operating temperature range by design and/or characterization, production tested at $T_J = T_A$ = 25 °C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
11. Can be disabled per customer request.

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ELECTRICAL CHARACTERISTICS – ADJUSTABLE

(V_{out} = 1.25 V typical, V_{in} = 2.9 V, T_A = –40 °C to +125 °C, unless otherwise noted, Note 12)

Characteristic	Symbol	Min	Typ	Max	Unit
Reference Voltage (Accuracy) V_{in} = 2.9 V to V_{out} +4.0 V, I_{load} = 0.1 mA to 500 mA, T_A = 25 °C	V_{ref}	–0.90% 1.239	1.25	0.90% 1.261	V
Reference Voltage (Accuracy) V_{in} = 2.9 V to V_{out} + 4.0 V, I_{load} = 0.1 mA to 500 mA, T_A = 0 °C to +85 °C	V_{ref}	–1.40% 1.233	1.25	1.40% 1.268	V
Reference Voltage (Accuracy) V_{in} = 2.9 V to V_{out} + 4.0 V, I_{load} = 0.1 mA to 500 mA, T_A = –40 °C to +125 °C	V_{ref}	–1.50% 1.231	1.25	1.50% 1.269	V
Line Regulation V_{in} = 2.9 V to 12 V, I_{load} = 0.1 mA	$Line_{Reg}$		0.04		mV/V
Load Regulation V_{in} = 2.9 V to 12 V, I_{load} = 0.1 mA to 500 mA	$Load_{Reg}$		0.04		mV/mA
Dropout Voltage (V_{out} = 2.5 V – 10 V) I_{load} = 500 mA I_{load} = 300 mA I_{load} = 50 mA I_{load} = 0.1 mA	V_{DO}		 340 230 110 10		mV
Peak Output Current (See Figure 14)	I_{pk}	500	700	830	mA
Short Output Current (See Figure 14) V_{in} < 7 V, T_A = 25 °C $V_{out} \leq$ 3.3 V V_{out} > 3.3 V	I_{sc}			 900 930	mA
Thermal Shutdown / Hysteresis	T_J		160/ 10		°C
Ground Current In Regulation I_{load} = 500 mA (Note 12) I_{load} = 300 mA I_{load} = 50 mA I_{load} = 0.1 mA In Dropout Vin = V_{out} + 0.1 V or 2.9 V (whichever is higher), I_{load} = 0.1 mA In Shutdown V_{SD} = 0 V	I_{GND} I_{GNDsh}		 9 4.6 0.8 	 14 7.5 2.5 220 500 1	 mA µA µA µA
Output Noise C_{nr} = 0 nF, I_{load} = 500 mA, f = 10 Hz to 100 kHz, Cout = 10 µF C_{nr} = 10 nF, I_{load} = 500 mA, f = 10 Hz to 100 kHz, Cout = 10 µF	V_{noise}		 69 46		μV_{rms}
Power Good Voltage Low Threshold Hysteresis High Threshold	V_{elft}	 93	 95 2 97	 99	% of V_{out}
Power Good Pin Voltage Saturation (I_{ef} = 1.0 mA)	V_{efdo}		200		mV
Power Good Pin Leakage	I_{efleak}		1		µA
Power Good Pin Blanking Time (Note 13)	t_{ef}		50		µs
Shutdown Threshold Voltage ON Threshold Voltage OFF	V_{SD}	 2		 0.4	V
SD Input Current, V_{SD} = 0 V to 0.4 V or V_{SD} = 2.0 V to V_{in} $V_{in} \leq$ 5.4 V V_{in} > 5.4 V	I_{SD}		 0.07	 1 5	µA
Output Current In Shutdown Mode, V_{out} = 0 V	I_{OSD}		0.07	1	µA
Reverse Bias Protection, Current Flowing from the Output Pin to GND (V_{in} = 0 V, V_{out_forced} = $V_{out\ (nom)} \leq$ 7 V)	I_{OUTR}		1		µA

12. Performance guaranteed over the operating temperature range by design and/or characterization, production tested at $T_J = T_A$ = 25 °C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
13. Can be disabled per customer request.

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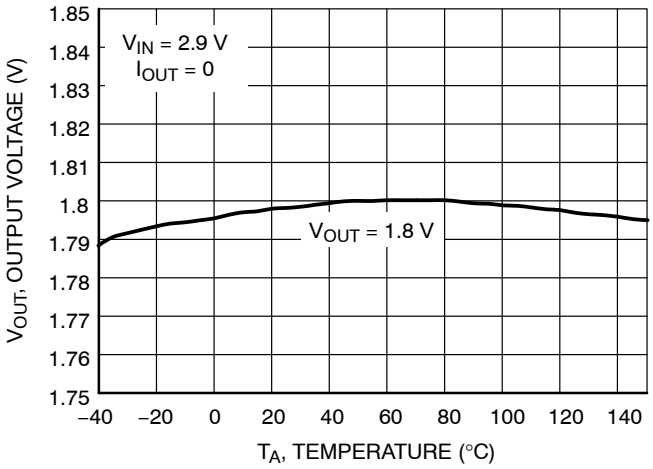


Figure 5. Output Voltage vs. Temperature 1.8 V Version

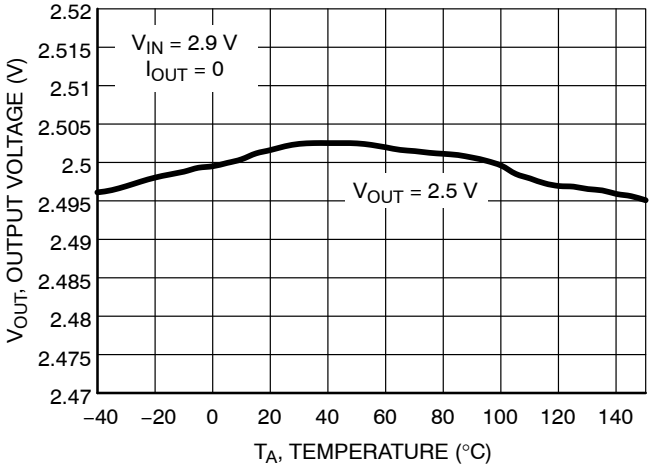


Figure 6. Output Voltage vs. Temperature 2.5 V Version

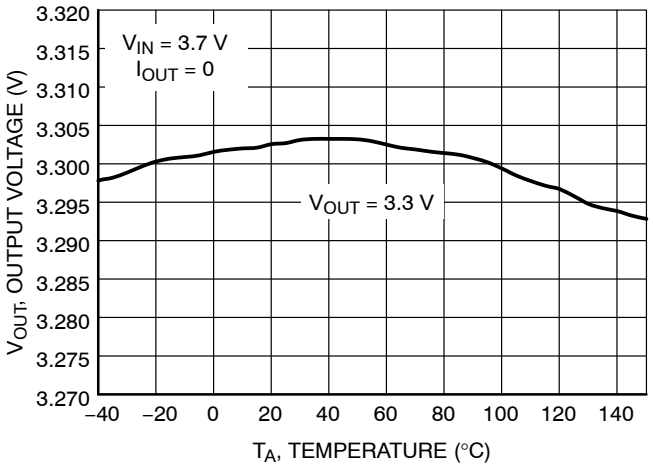


Figure 7. Output Voltage vs. Temperature 3.3 V Version

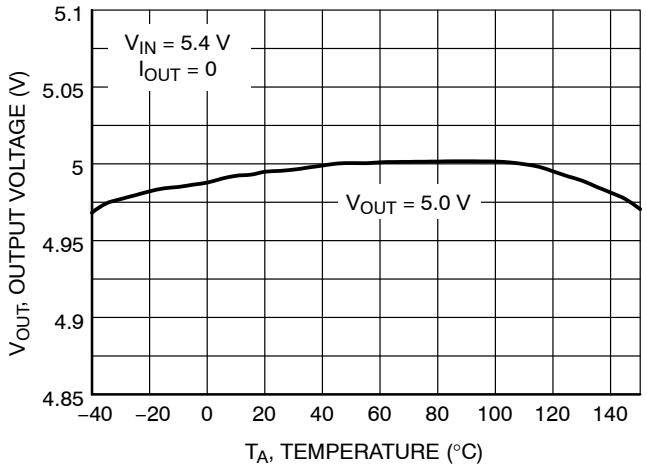


Figure 8. Output Voltage vs. Temperature 5.0 V Version

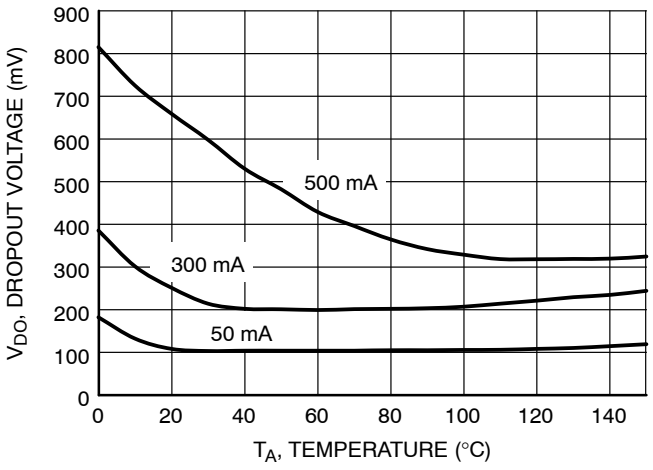


Figure 9. Dropout Voltage vs. Temperature 1.8 V Version

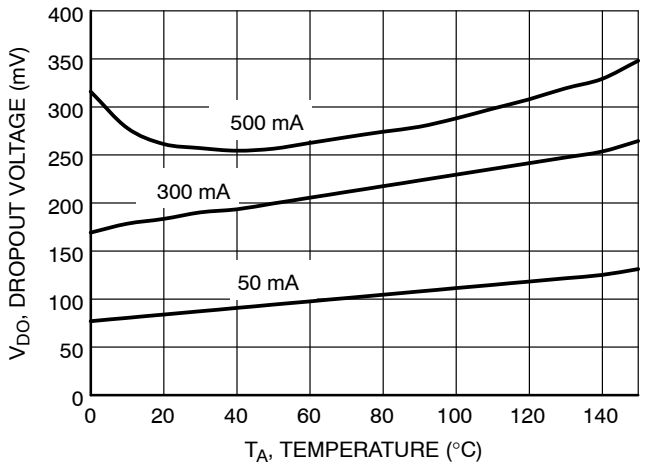


Figure 10. Dropout Voltage vs. Temperature 2.5 V Version

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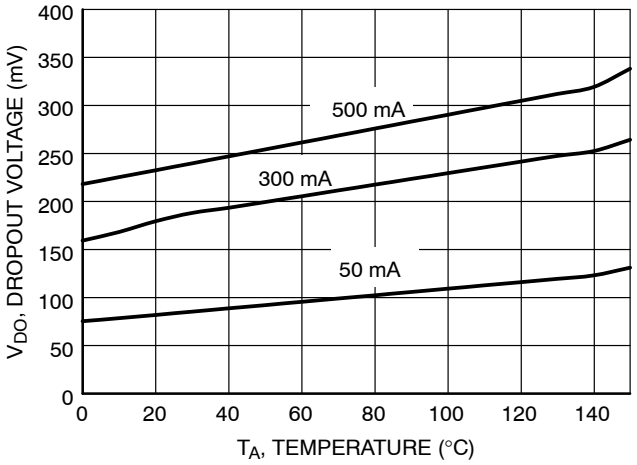


Figure 11. Dropout Voltage vs. Temperature 3.3 V Version

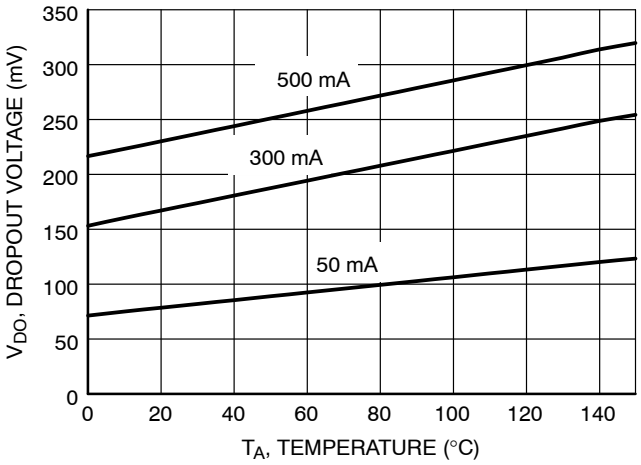


Figure 12. Dropout Voltage vs. Temperature 5.0 V Version

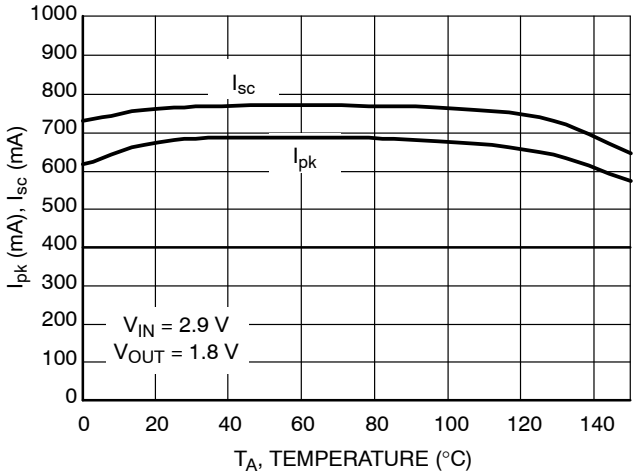
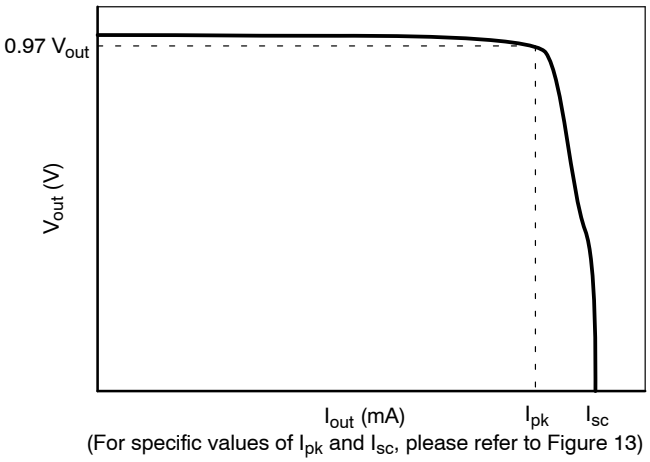


Figure 13. Peak and Short Current vs. Temperature



(For specific values of I_{pk} and I_{sc}, please refer to Figure 13)

Figure 14. Output Voltage vs. Output Current

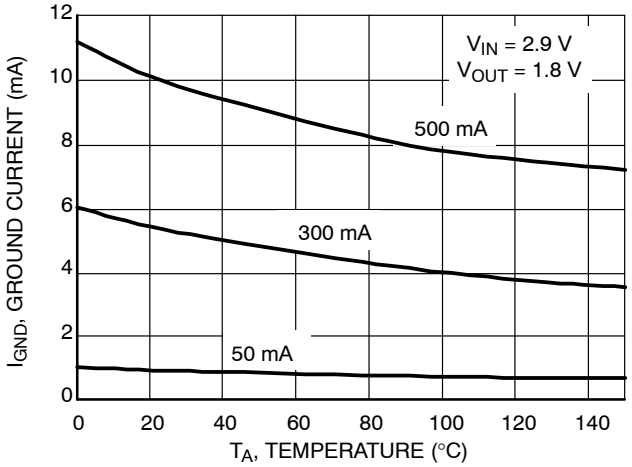


Figure 15. Ground Current vs. Temperature

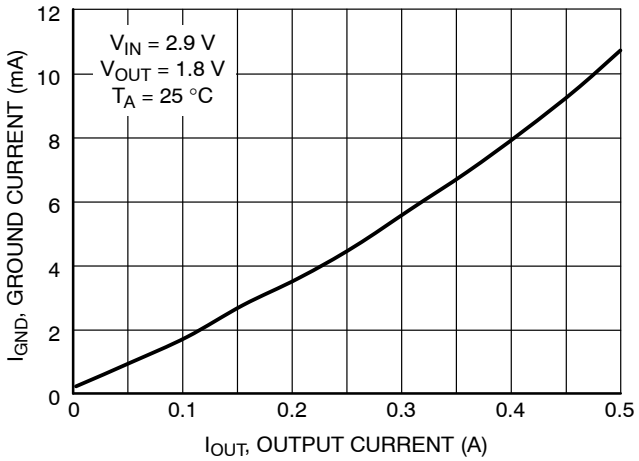


Figure 16. Ground Current vs. Output Current

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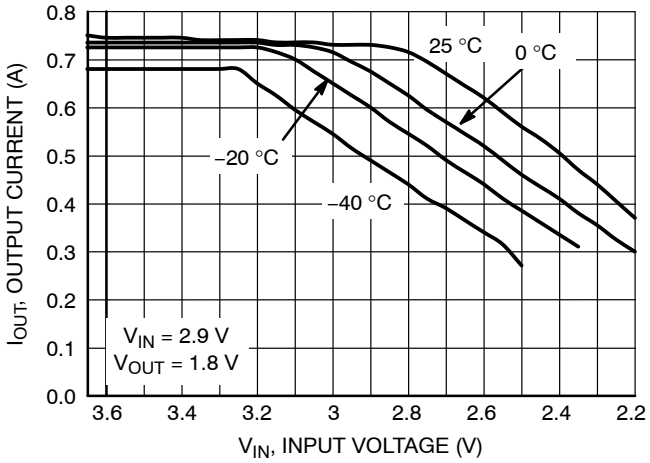


Figure 17. Output Current Capability for the 1.8 V Version

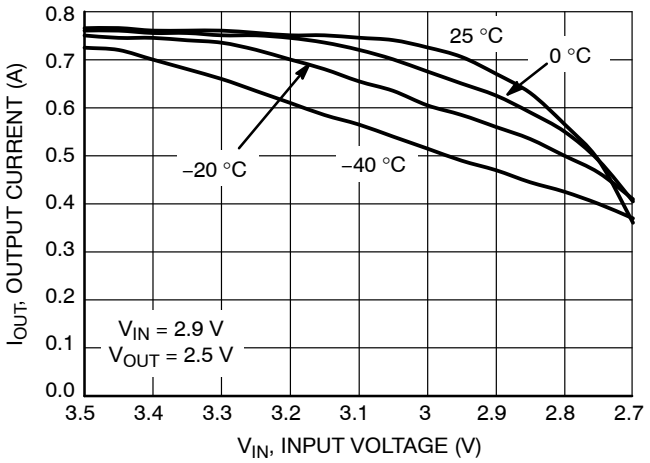


Figure 18. Output Current Capability for the 2.5 V Version

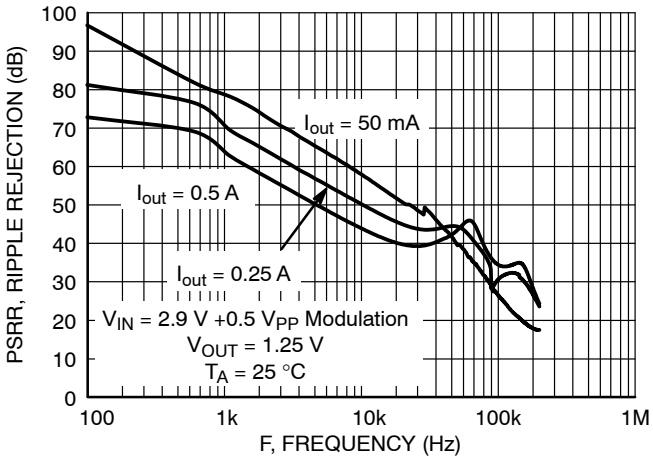


Figure 20. PSRR vs. Frequency Adjustable Version

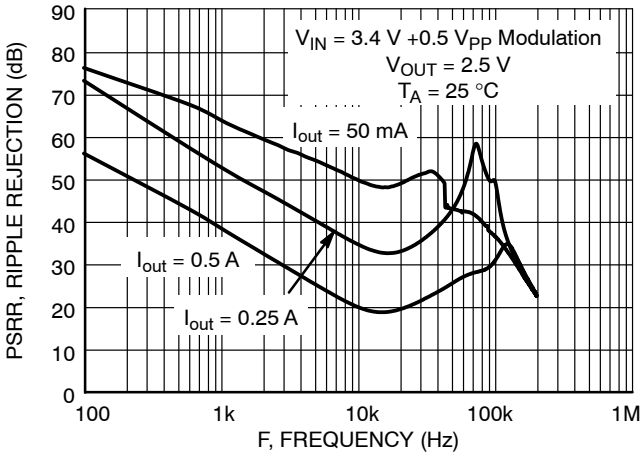


Figure 21. PSRR vs. Frequency 2.5 V Version

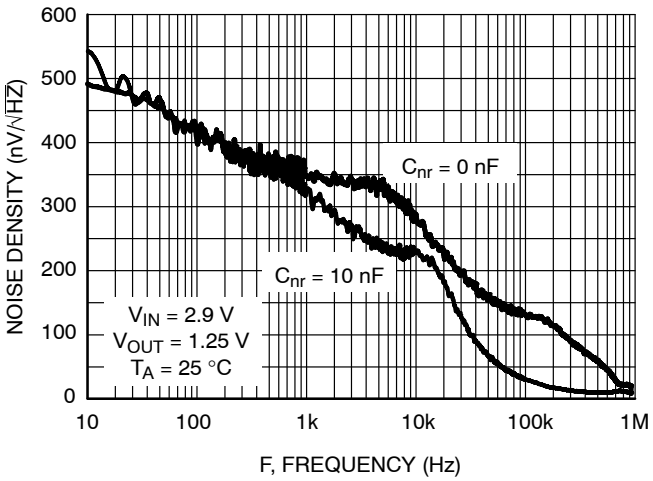


Figure 22. Output Noise Density Adjustable Version

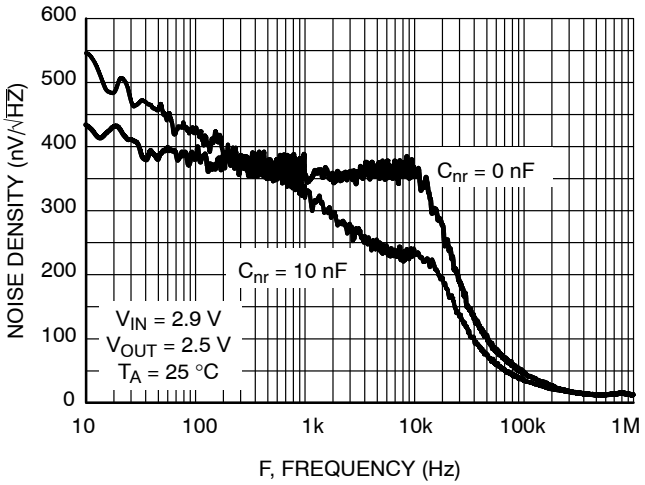


Figure 23. Output Noise Density 2.5 V Version

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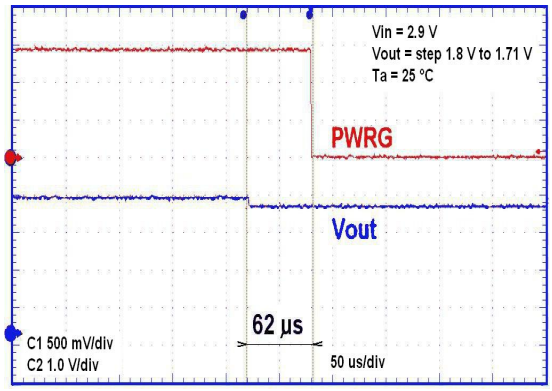


Figure 24. Power Good Activation

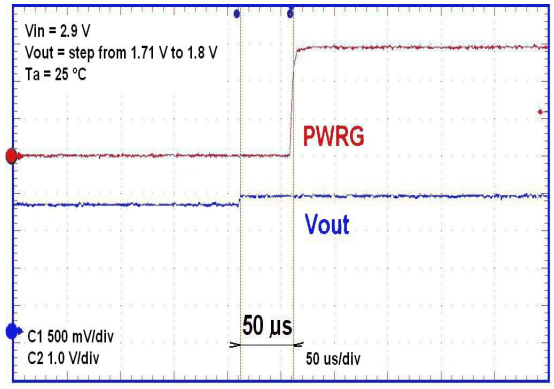


Figure 25. Power Good Inactivation

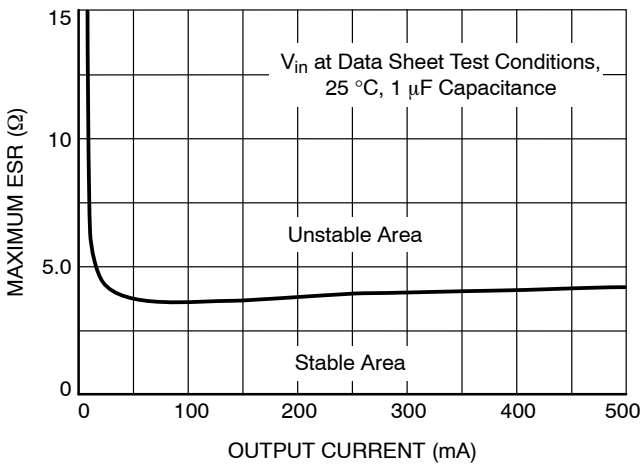


Figure 26. Stability with ESR vs. Output Current

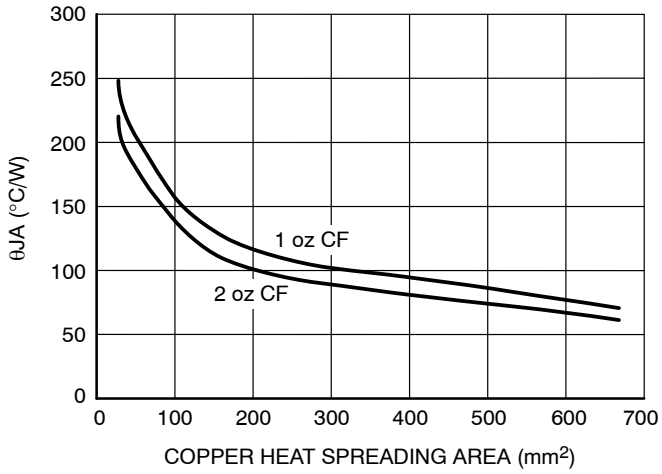


Figure 27. DFN10 Self-Heating Thermal Characterstics as a Function of Copper Area on the PCB

NOTE: Typical characteristics were measured with the same conditions as electrical characteristics.

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APPLICATIONS INFORMATION

Reverse Bias Protection

Reverse bias is a condition caused when the input voltage goes to zero, but the output voltage is kept high either by a large output capacitor or another source in the application which feeds the output pin.

Normally in a bipolar LDO all the current will flow from the output pin to input pin through the PN junction with limited current capability and with the potential to destroy the IC.

Due to an improved architecture, the NCV8537 can withstand up to 7.0 V on the output pin with virtually no current flowing from output pin to input pin, and only negligible amount of current (tens of μA) flowing from the output pin to ground for infinite duration.

Input Capacitor

An input capacitor of at least 1.0 μF, any type, is recommended to improve the transient response of the regulator and/or if the regulator is located more than a few inches from the power source. It will also reduce the circuit's sensitivity to the input line impedance at high frequencies. The capacitor should be mounted with the shortest possible track length directly across the regular's input terminals.

Output Capacitor

The NCV8537 remains stable with any type of capacitor as long as it fulfills its 1.0 μF requirement. There are no constraints on the minimum ESR and it will remain stable up to an ESR of 5.0 Ω. Larger capacitor values will improve the noise rejection and load transient response.

Noise Reduction Pin

Output noise can be greatly reduced by connecting a 10 nF capacitor (C_{nr}) between the noise reduction pin and ground (see Figure 1). In applications where very low noise is not required, the noise reduction pin can be left unconnected.

Dropout Voltage

The voltage dropout is measured at 97% of the nominal output voltage.

Thermal Considerations

Internal thermal limiting circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. This feature provides protection from a catastrophic device failure due to accidental overheating. This protection feature is not intended to be used as a substitute to heat sinking. The maximum power that can be dissipated, can be calculated with the equation below:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}} \quad \text{(eq. 1)}$$

For improved thermal performance, contact the factory for the DFN package option. The DFN package includes an exposed metal pad that is specifically designed to reduce the junction to air thermal resistance, $R_{\theta JA}$.

Adjustable Operation

The output voltage can be set by using a resistor divider as shown in Figure 2 with a range of 1.25 to 10 V. The appropriate resistor divider can be found by solving the equation below. The recommended current through the resistor divider is from 10 μA to 100 μA. This can be accomplished by selecting resistors in the kΩ range. As result, the I_{adj} * R2 becomes negligible in the equation and can be ignored.

$$V_{out} = 1.25 * (1 + R3/R2) + I_{adj} * R2 \quad \text{(eq. 2)}$$

Power Good Operation

The Power Good pin on the NCV8537 will produce a logic Low when it drops below the nominal output voltage. Refer to the electrical characteristics for the threshold values at which point the Power Good goes Low. When the NCV8537 is above the nominal output voltage, the Power Good will remain at logic High.

The external pullup resistor needs to be connected between V_{in} and the Power Good pin. A resistor of approximately 100 kΩ is recommended to minimize the current consumption. No pullup resistor is required if the Power Good output is not being used. The Power Good does not function during thermal shutdown and when the part is disabled.

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ORDERING INFORMATION

Device*	Voltage Option	Marking	Package	Package	Shipping†
NCV8537MN180R2G	1.8 V	V8537 180	DFN10 (Pb-Free)	Non-Wettable Flank	3000 / Tape & Reel
NCV8537MN250R2G	2.5 V	V8537 250			
NCV8537MN330R2G	3.3 V	V8537 330			
NCV8537MNADJR2G	Adj	V8537 ADJ			
NCV8537ML180R2G	1.8 V	L8537 180	DFNW10 (Pb-Free)	Wettable Flank SLP Process	3000 / Tape & Reel
NCV8537ML250R2G	2.5 V	L8537 250			
NCV8537ML330R2G	3.3 V	L8537 330			
NCV8537ML500R2G	5.0 V	L8537 500			
NCV8537MLADJR2G	Adj	L8537 ADJ			

DISCONTINUED (Note 14)

NCV8537MN500R2G	5.0 V	V8537 500	DFN10 (Pb-Free)	Non−Wettable Flank	3000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

* NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

14. **DISCONTINUED:** This device is not available. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.

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REVISION HISTORY

Revision	Description of Changes	Date
7	Document rebranded to **onsemi** format. NCV8537MN500R2G OPN marked as discontinued.	2/18/2026

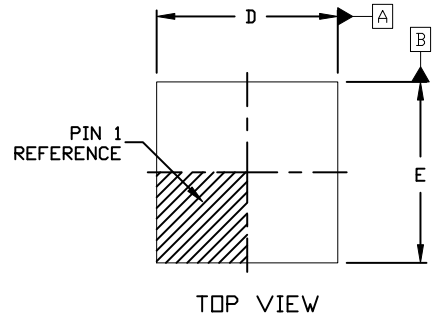
This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

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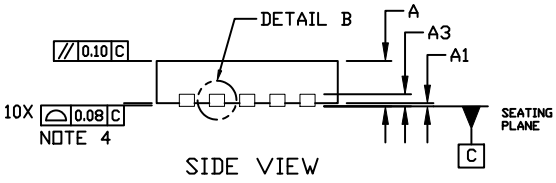
DFN10, 3x3, 0.5P
CASE 485C
ISSUE F

DATE 16 DEC 2021

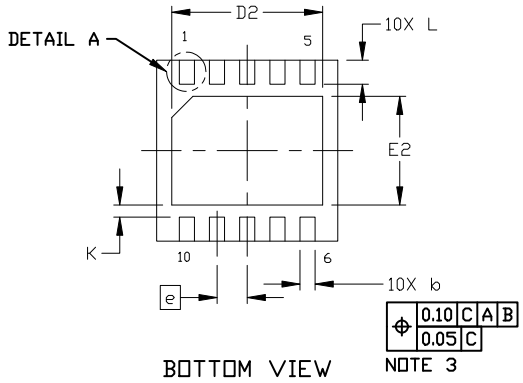
SCALE 2:1



TOP VIEW

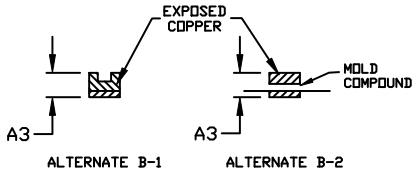


SIDE VIEW

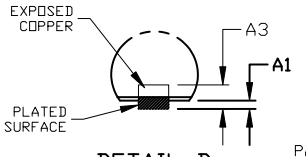


BOTTOM VIEW

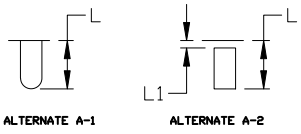
NOTES:
1. DIMENSION AND TOLERANCING PER ASME Y14.5, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. TERMINAL b MAY HAVE MOLD COMPOUND MATERIAL ALONG SIDE EDGE. MOLD FLASH MAY NOT EXCEED 30 MICRONS ONTO BOTTOM SURFACE OF TERMINAL.
6. FOR DEVICE OPN CONTAINING W OPTION, DETAIL A AND DETAIL B ALTERNATE CONSTRUCTIONS ARE NOT APPLICABLE. WETTABLE FLANK CONSTRUCTION IS DETAIL B AS SHOWN ON SIDE VIEW OF PACKAGE.



DETAIL B
ALTERNATE CONSTRUCTION

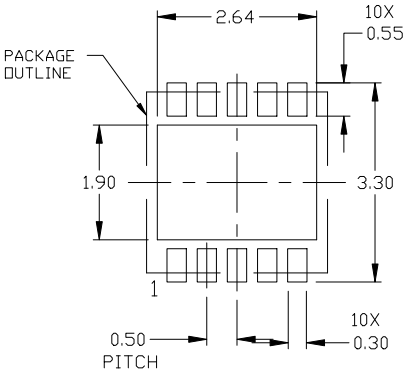


DETAIL B
WETTABLE FLANK
CONSTRUCTION



DETAIL A
ALTERNATE CONSTRUCTION

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	---	0.05
A3		0.20 REF	
b	0.18	0.23	0.30
D	2.90	3.00	3.10
D2	2.40	2.50	2.60
E	2.90	3.00	3.10
E2	1.70	1.80	1.90
e		0.50 BSC	
K		0.20 REF	
L	0.30	0.40	0.50
L1	---	---	0.03



RECOMMENDED
MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

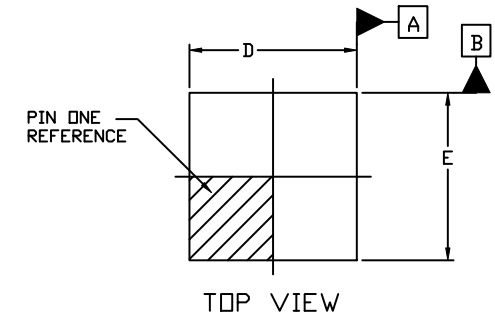
*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**DFN10, 3X3 MM, 0.5 MM PITCH**		**PAGE 1 OF 1**

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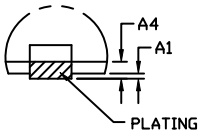
DFNW10 3x3, 0.5P
CASE 507AM
ISSUE A

DATE 12 JUN 2018



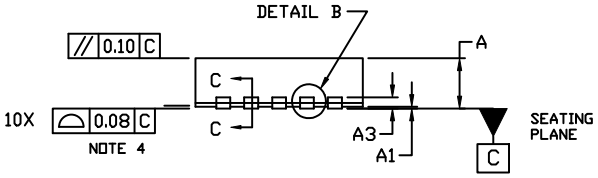
TOP VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
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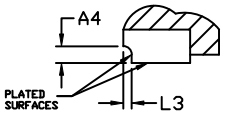


DETAIL B

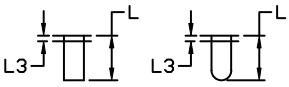
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	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	---	0.05
A3		0.20 REF	
A4	0.10	---	---
b	0.20	0.25	0.30
D	2.85	3.00	3.15
D2	2.40	2.50	2.60
E	2.85	3.00	3.15
E2	1.70	1.80	1.90
e		0.50 BSC	
k		0.19 REF	
L	0.35	0.40	0.45
L3	---	0.05	0.10

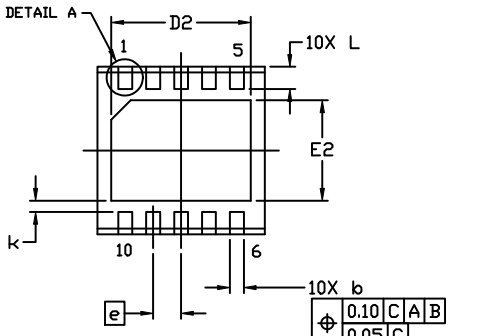


SIDE VIEW



SECTION C-C

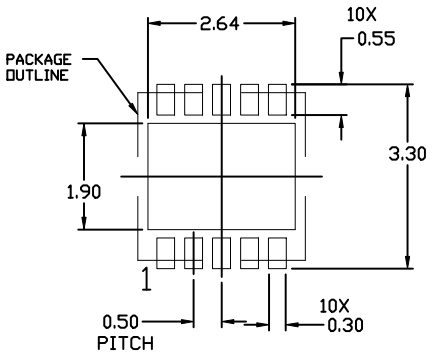




BOTTOM VIEW

ALTERNATE
CONSTRUCTION

DETAIL A



RECOMMENDED
MOUNTING FOOTPRINT

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**DFNW10 3x3, 0.5P**	**PAGE 1 OF 1**

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