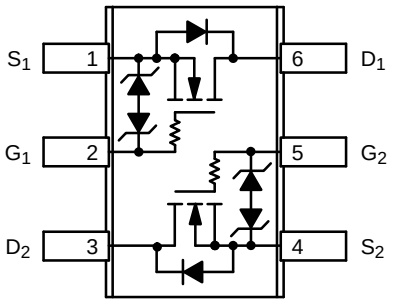
MOSFET – Dual, N-Channel, Small Signal, ESD Protection, SC-88

20 V

NTJD4401N, NVJD4401N

$V_{(BR)DSS}$	$R_{DS(on)}$ Typ	I_D Max
20 V	0.29 Ω @ 4.5 V	0.63 A
	0.36 Ω @ 2.5 V	

SC-88 (SOT-363)



Top View

Features

- Small Footprint (2 x 2 mm)
- Low Gate Charge N-Channel Device
- ESD Protected Gate
- Same Package as SC-70 (6 Leads)
- AEC-Q101 Qualified and PPAP Capable − NVJD4401N
- These Devices are Pb-Free and are RoHS Compliant

Applications

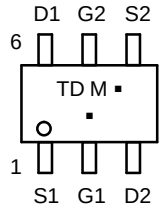
- Load Power Switching
- Li-Ion Battery Supplied Devices
- Cell Phones, Media Players, Digital Cameras, PDAs
- DC-DC Conversion

MARKING DIAGRAM & PIN ASSIGNMENT



1

SC-88/SOT-363
CASE 419B
STYLE 28



TD = Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

MAXIMUM RATINGS (T_J = 25 °C unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	20	V
Gate-to-Source Voltage			V_{GS}	±12	V
Continuous Drain Current (Based on $R_{\theta JA}$)	Steady State	T_A = 25 °C	I_D	0.63	A
		T_A = 85 °C		0.46	
Power Dissipation (Based on $R_{\theta JA}$)	Steady State	T_A = 25 °C	P_D	0.27	W
		T_A = 85 °C		0.14	
Continuous Drain Current (Based on $R_{\theta JL}$)	Steady State	T_A = 25 °C	I_D	0.91	A
		T_A = 85 °C		0.65	
Power Dissipation (Based on $R_{\theta JL}$)	Steady State	T_A = 25 °C	P_D	0.55	W
		T_A = 85 °C		0.29	
Pulsed Drain Current		t ≤10 μs	I_{DM}	±1.2	A
Operating Junction and Storage Temperature			T_J, T_{STG}	−55 to 150	°C
Continuous Source Current (Body Diode)			I_S	0.63	A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	°C

THERMAL RESISTANCE RATINGS (Note 1)

Parameter	Symbol	Typ	Max	Units
Junction-to-Ambient − Steady State	$R_{\theta JA}$	400	458	°C/W
Junction-to-Lead (Drain) − Steady State	$R_{\theta JL}$	194	252	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface mounted on FR4 board using 1 oz Cu area = 0.9523 in sq.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

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ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise stated)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		20	27		V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				22		mV/ °C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 16 V				1.0	μA
Gate-to-Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±12 V				10	μA
ON CHARACTERISTICS (Note 2)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		0.6	0.92	1.5	V
Gate Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				−2.1		mV/ °C
Drain-to-Source On Resistance	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D = 0.63 A			0.29	0.375	Ω
		V_{GS} = 2.5 V, I_D = 0.40 A			0.36	0.445	
Forward Transconductance	g_{FS}	V_{DS} = 4.0 V, I_D = 0.63 A			2.0		S
CHARGES AND CAPACITANCES							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = 20 V			33	46	pF
Output Capacitance	C_{OSS}				13	22	
Reverse Transfer Capacitance	C_{RSS}				2.8	5.0	
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 10 V, I_D = 0.63 A			1.3	3.0	nC
Threshold Gate Charge	$Q_{G(TH)}$				0.1		
Gate-to-Source Charge	Q_{GS}				0.2		
Gate-to-Drain Charge	Q_{GD}				0.4		
SWITCHING CHARACTERISTICS (Note 3)							
Turn-On Delay Time	$td_{(ON)}$	V_{GS} = 4.5 V, V_{DD} = 10 V, I_D = 0.5 A, R_G = 20 Ω			0.083		μs
Rise Time	tr				0.227		
Turn-Off Delay Time	$td_{(OFF)}$				0.786		
Fall Time	tf				0.506		
DRAIN-SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S =0.23 A	T_J = 25 °C		0.76	1.1	V
			T_J = 125 °C		0.63		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI_S/dt = 100 A/μs, I_S = 0.63 A			0.410		μs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperatures.

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TYPICAL PERFORMANCE CURVES (T_J = 25 °C unless otherwise noted)

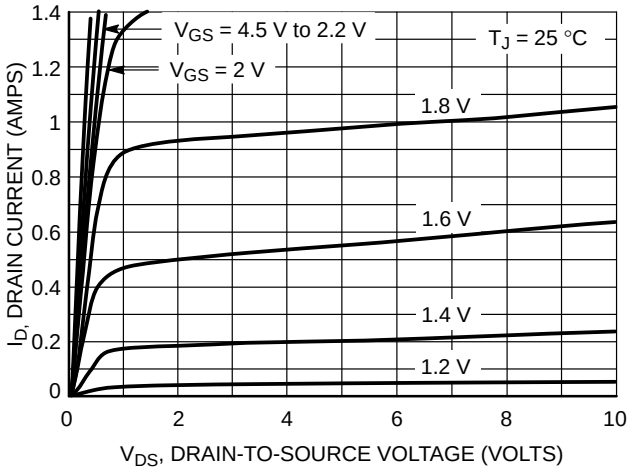

Figure 1. On-Region Characteristics

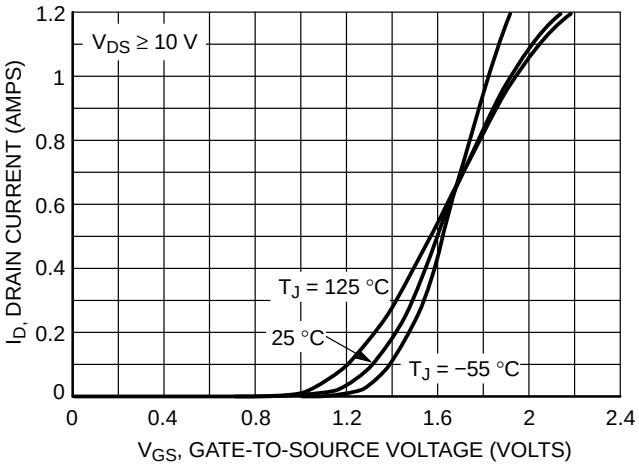

Figure 2. Transfer Characteristics

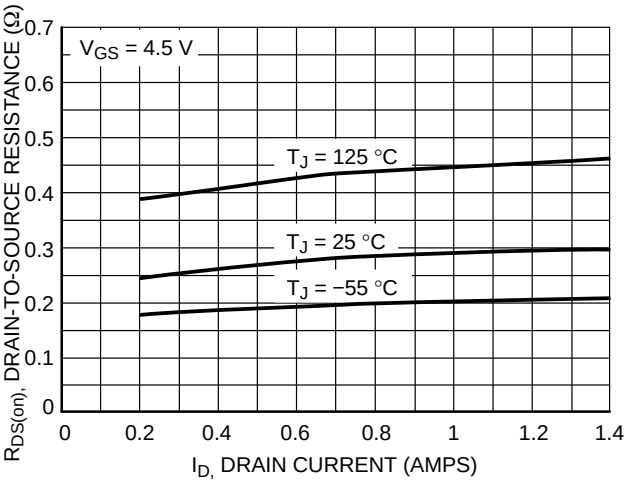

Figure 3. On-Resistance vs. Drain Current and Temperature

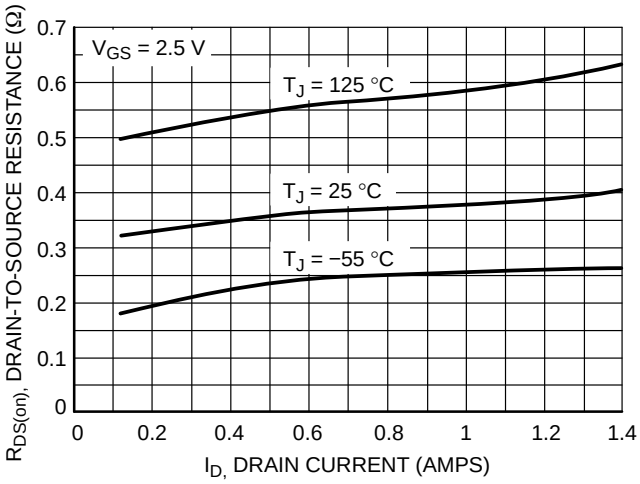

Figure 4. On-Resistance vs. Drain Current and Temperature

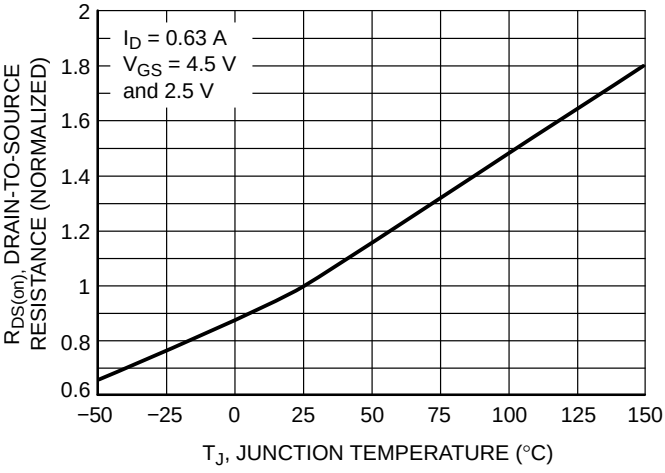

Figure 5. On-Resistance Variation with Temperature

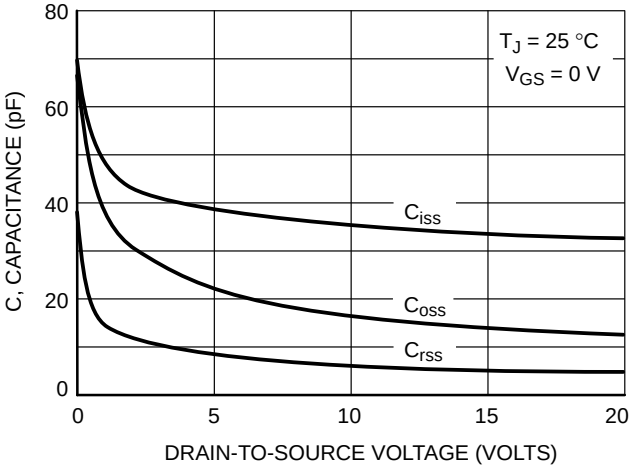

Figure 6. Capacitance Variation

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TYPICAL PERFORMANCE CURVES (T_J = 25 °C unless otherwise noted)

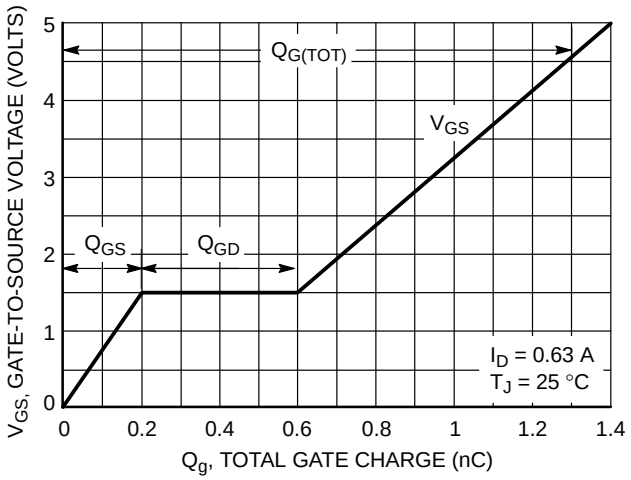

Figure 7. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

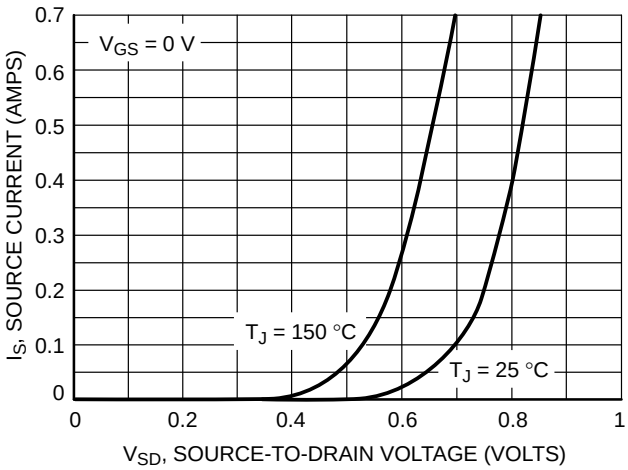

Figure 8. Diode Forward Voltage vs. Current

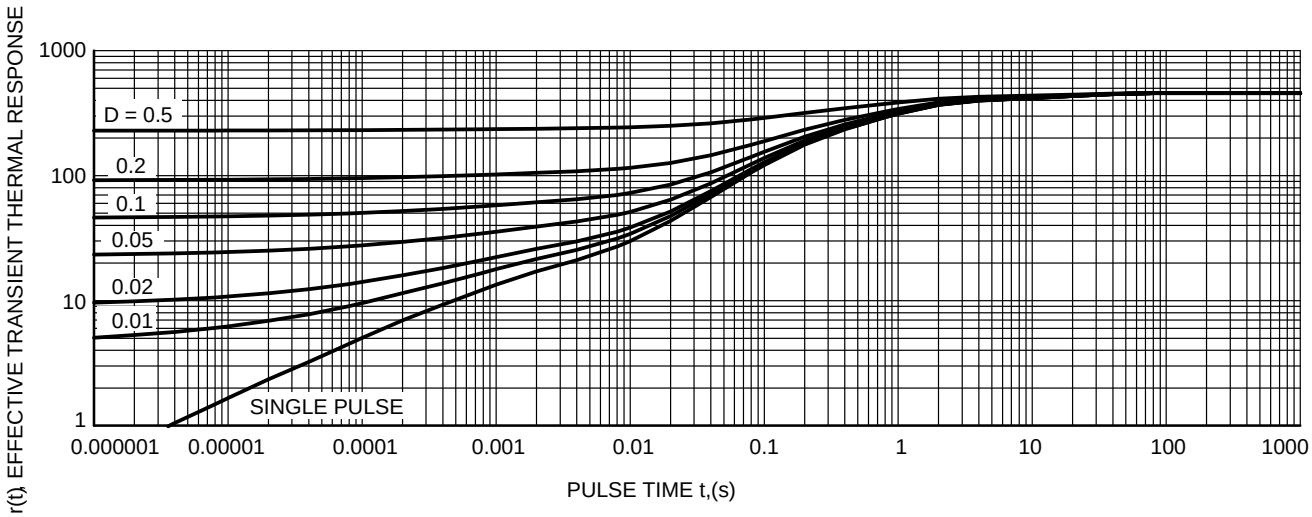

Figure 9. Thermal Response

ORDERING INFORMATION

Device	Package	Shipping†
NTJD4401NT1G	SC-88 (Pb-Free)	3000 / Tape & Reel
NVJD4401NT1G	SC-88 (Pb-Free)	3000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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REVISION HISTORY

Revision	Description of Changes	Date
8	Rebranded the document to **onsemi** format.	2/6/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

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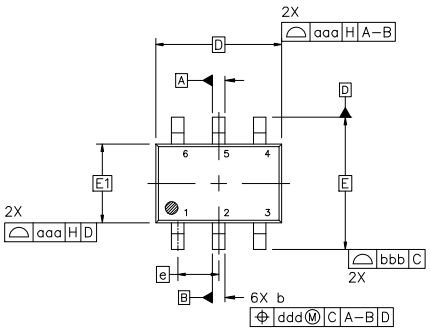
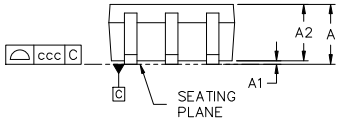
SC−88 2.00x1.25x0.90, 0.65P
CASE 419B−02
ISSUE Z

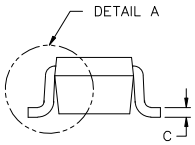
DATE 18 APR 2024



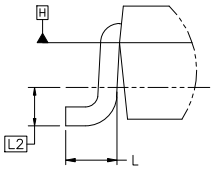
TOP VIEW



SIDE VIEW



END VIEW

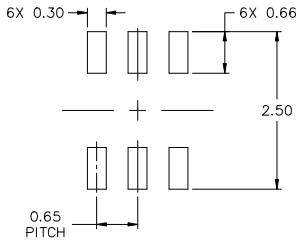


DETAIL A
SCALE 2:1

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

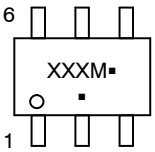
	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	−−−	−−−	1.10
A1	0.00	−−−	0.10
A2	0.70	0.90	1.00
b	0.15	0.20	0.25
c	0.08	0.15	0.22
D	2.00 BSC		
E	2.10 BSC		
E1	1.25 BSC		
e	0.65 BSC		
L	0.26	0.36	0.46
L2	0.15 BSC		
aaa	0.15		
bbb	0.30		
ccc	0.10		
ddd	0.10		



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SC−88 2.00x1.25x0.90, 0.65P
CASE 419B−02
ISSUE Z

DATE 18 APR 2024

STYLE 1:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 2:
CANCELLED

STYLE 3:
CANCELLED

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. COLLECTOR
4. EMITTER
5. BASE
6. ANODE

STYLE 5:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 6:
PIN 1. ANODE 2
2. N/C
3. CATHODE 1
4. ANODE 1
5. N/C
6. CATHODE 2

STYLE 7:
PIN 1. SOURCE 2
2. DRAIN 2
3. GATE 1
4. SOURCE 1
5. DRAIN 1
6. GATE 2

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. EMITTER 2
2. EMITTER 1
3. COLLECTOR 1
4. BASE 1
5. BASE 2
6. COLLECTOR 2

STYLE 10:
PIN 1. SOURCE 2
2. SOURCE 1
3. GATE 1
4. DRAIN 1
5. DRAIN 2
6. GATE 2

STYLE 11:
PIN 1. CATHODE 2
2. CATHODE 2
3. ANODE 1
4. CATHODE 1
5. CATHODE 1
6. ANODE 2

STYLE 12:
PIN 1. ANODE 2
2. ANODE 2
3. CATHODE 1
4. ANODE 1
5. ANODE 1
6. CATHODE 2

STYLE 13:
PIN 1. ANODE
2. N/C
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 14:
PIN 1. VREF
2. GND
3. GND
4. IOUT
5. VEN
6. VCC

STYLE 15:
PIN 1. ANODE 1
2. ANODE 2
3. ANODE 3
4. CATHODE 3
5. CATHODE 2
6. CATHODE 1

STYLE 16:
PIN 1. BASE 1
2. EMITTER 2
3. COLLECTOR 2
4. BASE 2
5. EMITTER 1
6. COLLECTOR 1

STYLE 17:
PIN 1. BASE 1
2. EMITTER 1
3. COLLECTOR 2
4. BASE 2
5. EMITTER 2
6. COLLECTOR 1

STYLE 18:
PIN 1. VIN1
2. VCC
3. VOUT2
4. VIN2
5. GND
6. VOUT1

STYLE 19:
PIN 1. I OUT
2. GND
3. GND
4. V CC
5. V EN
6. V REF

STYLE 20:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 21:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. N/C
6. CATHODE 1

STYLE 22:
PIN 1. D1 (i)
2. GND
3. D2 (i)
4. D2 (c)
5. VBUS
6. D1 (c)

STYLE 23:
PIN 1. Vn
2. CH1
3. Vp
4. N/C
5. CH2
6. N/C

STYLE 24:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 25:
PIN 1. BASE 1
2. CATHODE
3. COLLECTOR 2
4. BASE 2
5. EMITTER
6. COLLECTOR 1

STYLE 26:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 27:
PIN 1. BASE 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. EMITTER 2
6. COLLECTOR 2

STYLE 28:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 29:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE/ANODE
6. CATHODE

STYLE 30:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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