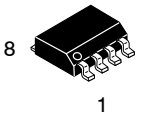
Secondary Side Synchronous Rectification Driver for High Efficiency SMPS Topologies

NCP4306



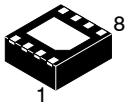
SOIC−8 NB
CASE 751−07



TSOP−6
CASE 318G−02



DFN8, 4x4
CASE 488AF



DFN8, 2.0x2.2, 0.5P
CASE 506BP

The NCP4306 is high performance driver tailored to control a synchronous rectification MOSFET in switch mode power supplies. Thanks to its high performance drivers and versatility, it can be used in various topologies such as DCM or CCM flyback, quasi resonant flyback, forward and half bridge resonant LLC.

The combination of externally or fixed adjustable minimum off-time and on-time blanking periods helps to fight the ringing induced by the PCB layout and other parasitic elements. A reliable and noise less operation of the SR system is insured due to the Self Synchronization feature. The NCP4306 also utilizes Kelvin connection of the driver to the MOSFET to achieve high efficiency operation at full load and utilizes a light load detection architecture to achieve high efficiency at light load.

The precise turn−off threshold, extremely low turn−off delay time and high sink current capability of the driver allow the maximum synchronous rectification MOSFET conduction time and enables maximum SMPS efficiency. The high accuracy driver and 5 V gate clamp enables the use of GaN MOSFETs.

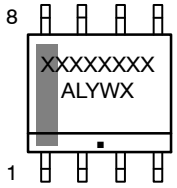
Features

- Self−Contained Control of Synchronous Rectifier in CCM, DCM and QR for Flyback or LLC Applications
- Precise True Secondary Zero Current Detection
- Typically 15 ns Turn off Delay from Current Sense Input to Driver
- Rugged Current Sense Pin (up to 200 V)
- Ultrafast Turn−off Trigger Interface / Disable Input (10.5 ns)
- Adjustable or Fixed Minimum ON−Time
- Adjustable or Fixed Minimum OFF-Time with Ringing Detection
- Improved Robust Self Synchronization Capability
- 7 A / 2 A Peak Current Sink / Source Drive Capability
- Operating Voltage Range up to V_{CC} = 35 V
- Automatic Light−load Disable Mode
- GaN Transistor Driving Capability
- Low Startup and Disable Current Consumption
- Maximum Operation Frequency up to 1 MHz
- TSOP6, SOIC8, DFN8 4x4 and DFN8 2x2.2 Packages
- This is a Pb−Free Device

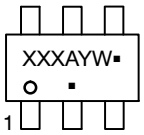
Typical Applications

- Notebook Adapters
- High Power Density AC / DC Power Supplies (Cell Phone Chargers)
- LCD TVs
- All SMPS with High Efficiency Requirements

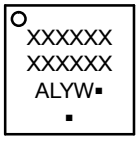
MARKING DIAGRAMS



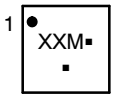
SOIC−8 NB



TSOP−6



DFN8, 4x4



DFN8, 2.0x2.2, 0.5P

See detailed marking information on page 2 of this data sheet.

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

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ORDERING INFORMATION TABLE

Table 1. AVAILABLE DEVICES

Device	Package Marking	Package	Shipping †
NCP4306AAAZZZADR2G	6AAAZZZA	SOIC−8 (Pb−Free)	2500 / Tape and Reel
NCP4306AADZZZADR2G	6AADZZZA		
NCP4306AAHZZZADR2G	6AAHZZZA		
NCP4306ABHZZZADR2G	6ABHZZZA		
NCP4306DADZZDASNT1G	6AC	TSOP−6 (Pb−Free)	3000 / Tape and Reel
NCP4306DAHZZAASNT1G	6AD		
NCP4306DADZZBASNT1G	6AK		
NCP4306AAAZZZAMNTWG	4306AAAZZZA	DFN−8 4x4 (Pb−Free)	4000 / Tape and Reel
NCP4306AADZZZAMNTWG	4306AADZZZA		
NCP4306ABHZZZAMNTWG	4306ABHZZZA		
NCP4306AAAZZZAMN1TBG	6A	DFN−8 2x2.2 (Pb−Free)	3000 / Tape and Reel
NCP4306AADZZZAMN1TBG	6D		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

See the **onsemi** Device Nomenclature document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

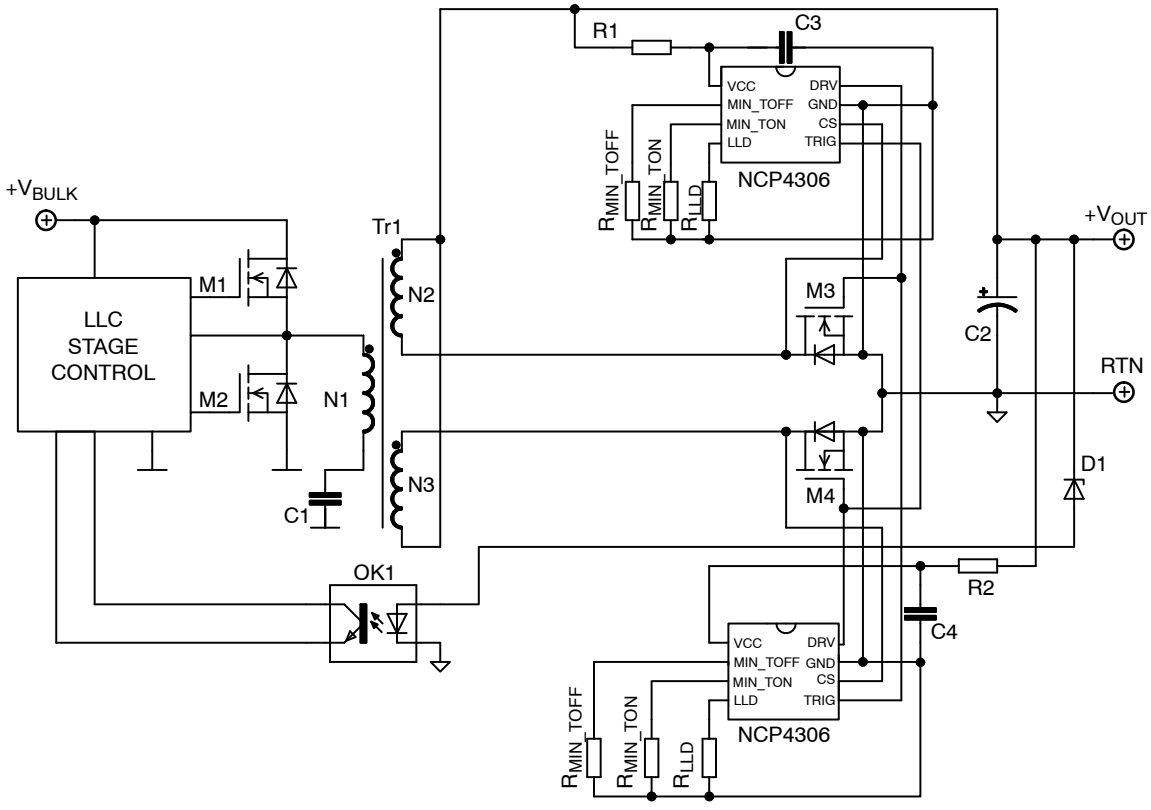


Figure 1. Typical Application Example – LLC Converter with optional LLD and Trigger Utilization

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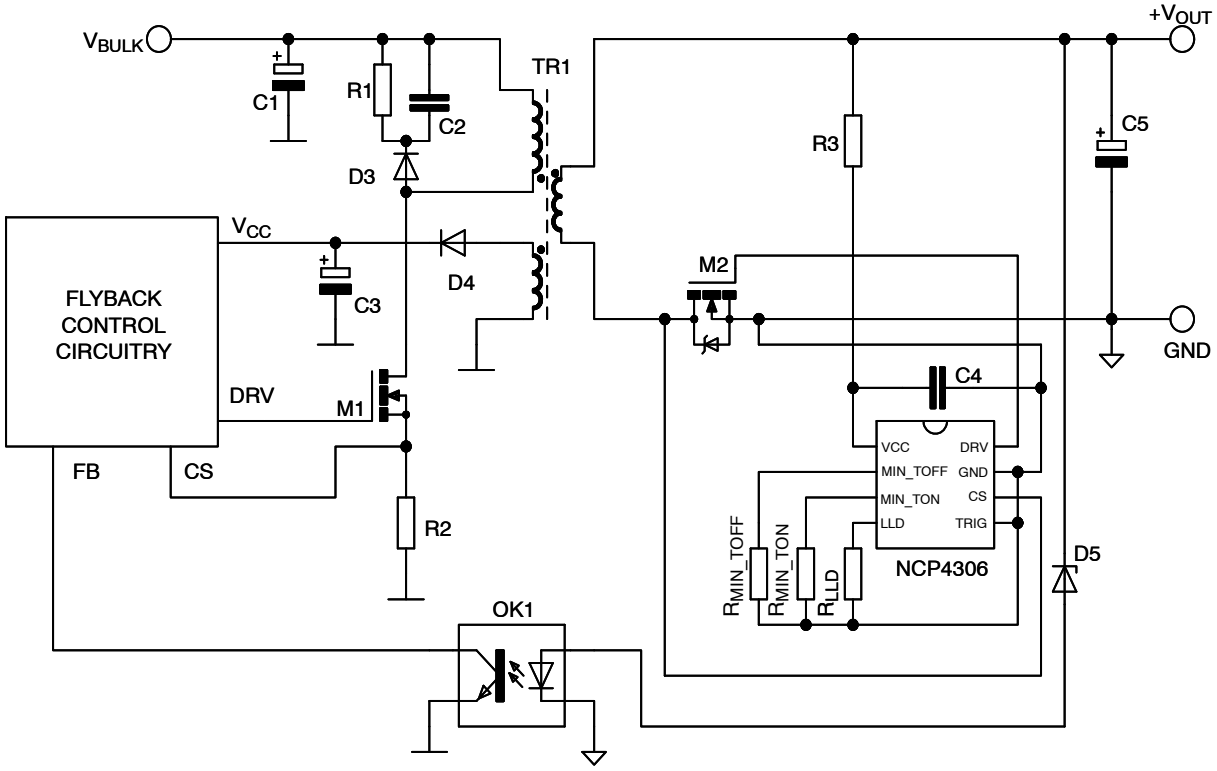


Figure 2. Typical Application Example – DCM, CCM or QR Flyback Converter with optional LLD and disabled TRIG

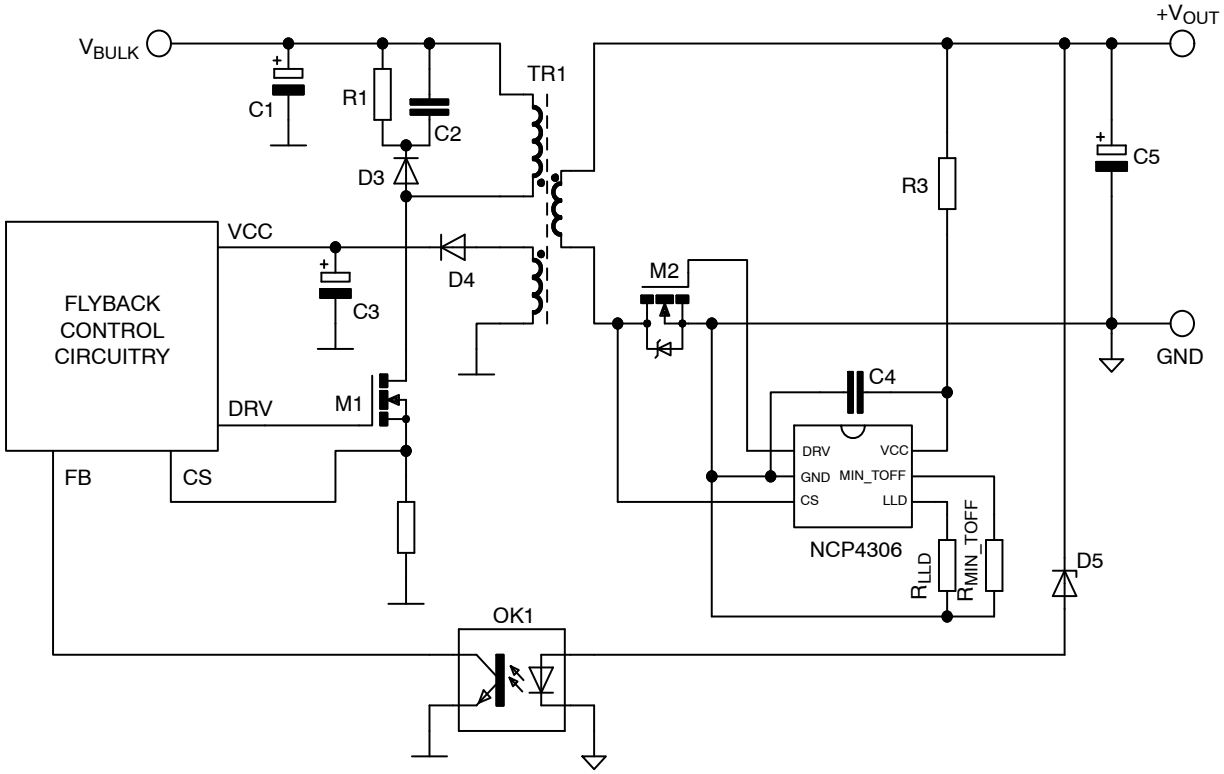


Figure 3. Typical Application Example – DCM, CCM or QR Flyback Converter with NCP4306 in TSOP6 (v Cxxxxxx)

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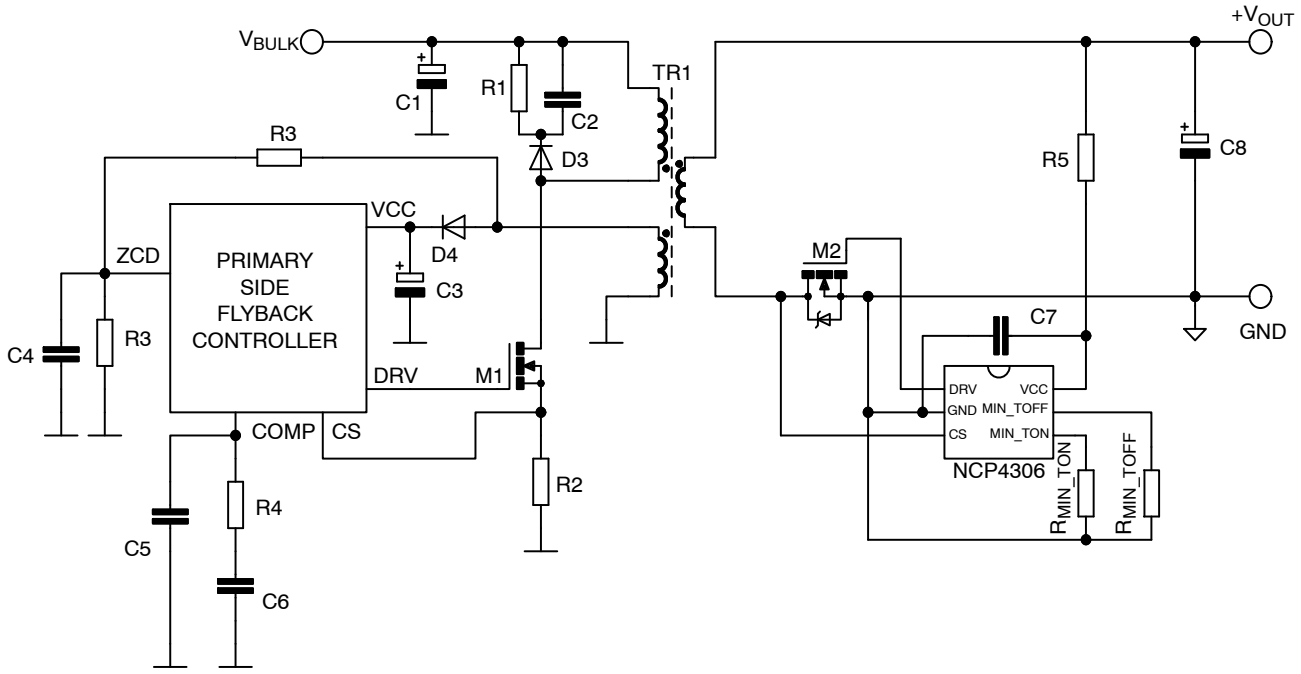


Figure 4. Typical Application Example – Primary Side Flyback Converter and NCP4306 in TSOP6

PIN FUNCTION DESCRIPTION

Table 2. PIN FUNCTION DESCRIPTION

TSOP6 Bxxxxxx	TSOP6 Cxxxxxx	TSOP6 Dxxxxxx	TSOP6 Exxxxxx	TSOP6 Fxxxxxx	TSOP6 Gxxxxxx	SOIC8, DFN8 Axxxxxx	Pin Name	Description
6	6	6	6	6	6	1	VCC	Supply voltage pin
–	5	5	5	–		2	MIN_TOFF	Adjust the minimum off time period by connecting resistor to ground
5	–	4	–	5	–	3	MIN_TON	Adjust the minimum on time period by connecting resistor to ground
4	4	–	–	–	4	4	LLD	This input modulates the driver clamp level and / or turns the driver off during light load conditions
–	–	–	4	4	5	5	TRIG / DIS	Ultrafast turn−off input that can be used to turn off the SR MOSFET in CCM applications in order to improve efficiency. Activates disable mode if pulled−up for more than 100 μs
3	3	3	3	3	3	6	CS	Current sense pin detects if the current flows through the SR MOSFET and / or its body diode
2	2	2	2	2	2	7	GND	Ground connection for the SR MOSFET driver and V_{CC} decoupling capacitor. Ground connection for minimum t_{ON} and t_{OFF} adjust resistors, LLD and trigger inputs. GND pin should be wired directly to the SR MOSFET source terminal / soldering point using Kelvin connection. DFN8 exposed flag should be connected to GND.
1	1	1	1	1	1	8	DRV	Driver output for the SR MOSFET

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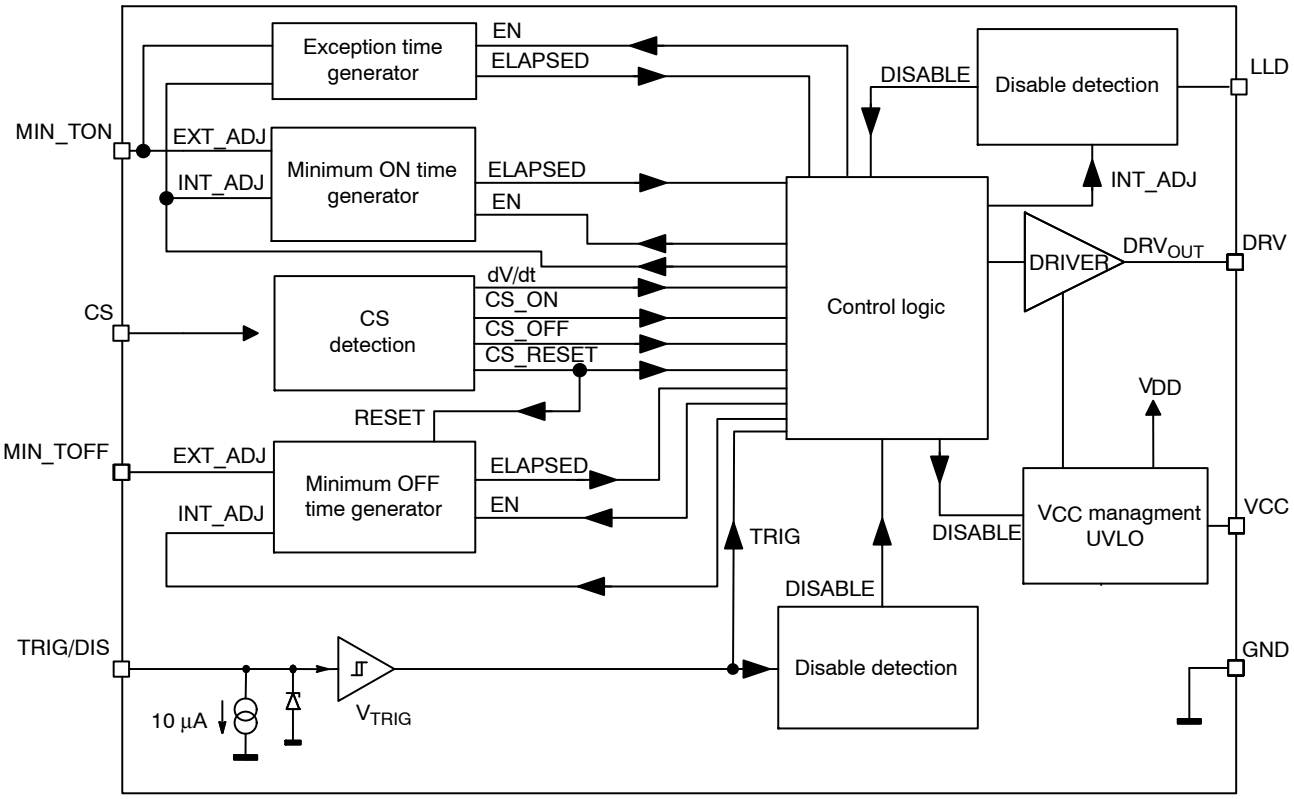


Figure 5. Internal Circuit Architecture – NCP4306

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ABSOLUTE MAXIMUM RATINGS

Table 3. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to 37.0	V
TRIG / DIS, MIN_TON, MIN_TOFF, LLD Input Voltage (Note 3)	$V_{TRIG\ /\ DIS}$, V_{MIN_TON}, V_{MIN_TOFF}, V_{LLD}	−0.3 to V_{CC}	V
Driver Output Voltage	V_{DRV}	−0.3 to 17.0	V
Current Sense Input Voltage	V_{CS}	−4 to 200	V
Current Sense Dynamic Input Voltage (t_{PW} = 200 ns)	V_{CS_DYN}	−10 to 200	V
MIN_TON, MIN_TOFF, LLD, TRIG Input Current	I_{MIN_TON}, I_{MIN_TOFF}, I_{LLD}, I_{TRIG}	−10 to 10	mA
DRV Pin Current (t_{PW} = 10 μs)	I_{DRV_DYN}	−3 to 12	A
VCC Pin Current (t_{PW} = 10 μs)	I_{VCC_DYN}	3	A
Junction to Air Thermal Resistance, 1 oz 1 in2 Copper Area, SOIC8	$R_{\theta J-A_SOIC8}$	200	°C / W
Junction to Air Thermal Resistance, 1 oz 1 in2 Copper Area TSOP6	$R_{\theta J-A_TSOP6}$	250	°C / W
Junction to Air Thermal Resistance, 1 oz 1 in2 Copper Area DFN8 4x4	$R_{\theta J-A_DFN8_4x4}$	80	°C / W
Junction to Air Thermal Resistance, 1 oz 1 in2 Copper Area DFN8 2x2.2	$R_{\theta J-A_DFN8_2x2.2}$	85	°C / W
Maximum Junction Temperature	T_{JMAX}	150	°C
Storage Temperature	T_{STG}	−60 to 150	°C
ESD Capability, Human Body Model (except pin CS) (Note 1)	ESD_{HBM}	2000	V
ESD Capability, Human Body Model Pin CS	ESD_{HBM}	600	V
ESD Capability, Machine Model (Note 1)	ESD_{MM}	200	V
ESD Capability, Charged Device Model (Note 1)	ESD_{CDM}	Class C3	-

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series contains ESD protection and exceeds the following tests:
   Except pin CS: Human Body Model 2000 V per JEDEC Standard JESD22−A114E.
   All pins: Machine Model Method 200 V per JEDEC Standard JESD22−A115−A
   Charged Machine Model per JEDEC Standard JESD22−C101F
2. This device meets latchup tests defined by JEDEC Standard JESD78D.
3. If voltage higher than 22 V is connected to pin, pin input current increases. Internal ESD clamp contains 24 V Zener diode with 3 kΩ in series. It is recommended to add serial resistance in case of higher input voltage to limit input pin current.

Table 4. RECOMMENDED OPERATING CONDITION

Parameter	Symbol	Min	Max	Unit
Maximum Operating Voltage	V_{CC}		35	V
Operating Junction Temperature	T_J	−40	125	°C

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ELECTRICAL CHARACTERISTICS

Table 5. ELECTRICAL CHARACTERISTICS

−40 °C ≤ T_J ≤ 125 °C; V_{CC} = 12 V; C_{DRV} = 0 nF; R_{MIN_TON} = R_{MIN_TOFF} = 10 kΩ or internally set values; V_{LLD} = 3.0 V or LLD internally disabled; $V_{TRIG\ /\ DIS}$ = 0 V; V_{CS} = 4 V, unless otherwise noted. Typical values are at T_J = +25 °C

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
SUPPLY SECTION							
VCC UVLO	V_{CC} rising		V_{CCON}	3.7	4.0	4.2	V
	V_{CC} falling		V_{CCOFF}	3.2	3.5	3.7	
VCC UVLO Hysteresis			V_{CCHYS}		0.5		V
Start−up Delay	V_{CC} rising from 0 to V_{CCON} + 1 V @ tr = 10 µs		t_{START_DEL}		50	80	µs
Current Consumption, t_{MIN_TON} = t_{MIN_TOFF} = 1 µs, t_{LLD} = 130 µs	C_{DRV} = 0 nF, f_{CS} = 100 kHz	xAxxxxx	I_{CC}		1.8	2.5	mA
		xBxxxxx			1.7	2.4	
	C_{DRV} = 1 nF, f_{CS} = 100 kHz	xAxxxxx			2.8	4.0	
		xBxxxxx			2.1	3.4	
	C_{DRV} = 10 nF, f_{CS} = 100 kHz	xAxxxxx			12	15	
		xBxxxxx			6.7	9.0	
Current Consumption			I_{CC}		1.4	2.2	mA
Current Consumption below UVLO	V_{CC} = V_{CCOFF} − 0.1 V		I_{CC_UVLO}		35	60	µA
Current Consumption in Disable Mode	t > t_{LLD} , V_{LLD} = 0.55 V		I_{CC_DIS}		60	100	µA
	$V_{TRIG\ /\ DIS}$ = 5 V; V_{LLD} = 0.55 V				60	100	
	t > t_{LLD}, LLD set internally				37	80	
	$V_{TRIG\ /\ DIS}$ = 5 V, LLD set internally				37	80	
DRIVER OUTPUT							
Output Voltage Rise−Time	C_{DRV} = 10 nF, 10 % to 90 % V_{DRVMAX}, V_{CS} = 4 to −1 V		t_r		60	100	ns
Output Voltage Fall−Time	C_{DRV} = 10 nF, 90 % to 10 % V_{DRVMAX}, V_{CS} = −1 to 4 V		t_f		25	45	ns
Driver Source Resistance			R_{DRV_SOURCE}		2		Ω
Driver Sink Resistance			R_{DRV_SINK}		0.5		Ω
Output Peak Source Current			I_{DRV_SOURCE}		2		A
Output Peak Sink Current			I_{DRV_SINK}		7		A
Maximum Driver Pulse Length			$t_{DRV_ON_MAX}$		4		ms
Maximum Driver Output Voltage	V_{CC} = 35 V, C_{DRV} > 1 nF, (ver. xAxxxxx)		V_{DRVMAX}	9	10	11	V
	V_{CC} = 35 V, C_{DRV} > 1 nF, (ver. xBxxxxx)			4.5	5.0	5.5	
Minimum Driver Output Voltage	V_{CC} = V_{CCOFF} + 200 mV, (ver. xAxxxxxx)		V_{DRVMIN}	3.4	3.7	3.9	V
	V_{CC} = V_{CCOFF} + 200 mV, (ver. xBxxxxxx)			3.4	3.7	3.9	
CS INPUT							
Total Propagation Delay From CS to DRV Output On	V_{CS} goes down from 4 to −1 V, t_{f_CS} <= 5 ns		t_{PD_ON}		30	60	ns
Total Propagation Delay From CS to DRV Output Off	V_{CS} goes up from −1 to 4 V, t_{r_CS} <= 5 ns		t_{PD_OFF}		13	23	ns
Turn On CS Threshold Voltage			$V_{TH_CS_ON}$	−120	−75	−40	mV
Turn Off CS Threshold Voltage	Guaranteed by Design		$V_{TH_CS_OFF}$	−1		0	mV
Turn Off Timer Reset Threshold Voltage			$V_{TH_CS_RESET}$	0.4	0.5	0.6	V
CS Leakage Current	V_{CS} = 200 V		$I_{CS_LEAKAGE}$			500	nA
dV / dt Detector High Threshold			$V_{CS_DVDT_H}$		3.0		V

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Table 5. ELECTRICAL CHARACTERISTICS (continued)

$-40\ ^{\circ}C \le T_J \le 125\ ^{\circ}C$; V_{CC} = 12 V; C_{DRV} = 0 nF; $R_{MIN_TON} = R_{MIN_TOFF}$ = 10 kΩ or internally set values; V_{LLD} = 3.0 V or LLD internally disabled; $V_{TRIG\ /\ DIS}$ = 0 V; V_{CS} = 4 V, unless otherwise noted. Typical values are at T_J = +25 °C

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
CS INPUT							
dV / dt Detector Low Threshold			$V_{CS_DVDT_L}$		0.5		V
dV / dt Detector Threshold	(Note 4)	ver. xxDxxxx	$t_{dV\ /\ dt}$	13	25	37	ns
TRIGGER DISABLE INPUT							
Minimum Trigger Pulse Duration	$V_{TRIG\ /\ DIS}$ = 5 V; Shorter pulses may not be proceeded		$t_{TRIG_PW_MIN}$			10	ns
Trigger Threshold Voltage			V_{TRIG_TH}	1.6	2.0	2.2	V
Trigger to DRV Propagation Delay	$V_{TRIG\ /\ DIS}$ goes from 0 to 5 V, $t_{r_TRIG\ /\ DIS}$ <= 5 ns		t_{PD_TRIG}		10.0	16.5	ns
Trigger Blank Time After DRV Turn−on Event	V_{CS} drops below $V_{TH_CS_ON}$		t_{TRIG_BLANK}	30	55	80	ns
Delay to Disable Mode	$V_{TRIG\ /\ DIS}$ goes from 0 to 5 V		t_{DIS_TIM}	75	100	125	µs
Disable Recovery Timer	$V_{TRIG\ /\ DIS}$ goes down from 5 to 0 V; t_{MIN_TOFF} = 130 ns		t_{DIS_REC}		1.5	3.0	µs
Minimum Pulse Duration to Disable Mode End	$V_{TRIG\ /\ DIS}$ = 0 V; Shorter pulses may not be proceeded		t_{DIS_END}			200	ns
Pull Down Current	$V_{TRIG\ /\ DIS}$ = 5 V		$I_{TRIG\ /\ DIS}$	7	11	15	µA
Maximum Transition Time	$V_{TRIG\ /\ DIS}$ goes from 1 to 3 V or from 3 to 1 V		t_{TRIG_TRAN}			10	µs
MINIMUM T_{ON} AND T_{OFF} ADJUST							
Minimum t_{ON} time	R_{MIN_TON} = 0 Ω (ver. xxxZxxx)		t_{ON_MIN}		55		ns
Minimum t_{OFF} time	R_{MIN_TOFF} = 0 Ω (ver. xxxxZxx)		t_{OFF_MIN}		70		ns
Minimum t_{ON} time	R_{MIN_TON} = 10 kΩ (ver. xxxZxxx)		t_{ON_MIN}	0.90	1.00	1.10	µs
Minimum t_{OFF} time	R_{MIN_TOFF} = 10 kΩ (ver. xxxxZxx)		t_{OFF_MIN}	0.90	1.00	1.10	µs
Minimum t_{ON} time	R_{MIN_TON} = 50 kΩ (ver. xxxZxxx)		t_{ON_MIN}	4.50	5.00	5.50	µs
Minimum t_{OFF} time	R_{MIN_TOFF} = 50 kΩ (ver. xxxxZxx)		t_{OFF_MIN}	4.40	4.90	5.40	µs
Internal minimum t_{ON} time	t_{ON_MIN} = 130 ns, (ver. xxxAxxx)		t_{ON_MIN}	−20%	t_{ON_MIN}	+20%	ns
	t_{ON_MIN} = 220, 310, 400 ns (ver. xxx[B−D]xxx)		t_{ON_MIN}	−15%	t_{ON_MIN}	+15%	ns
	t_{ON_MIN} = 500, 600, 700, 800, 1000, 1200, 1400, 1700, 2000 ns (ver. xxx[E−M]xxx)		t_{ON_MIN}	−10%	t_{ON_MIN}	+10%	ns
Internal minimum t_{OFF} time	t_{OFF_MIN} = 0.9, 1.0, 1.1, 1.2, 1.4, 1.6, 1.8, 2.0, 2.2, 2.4, 2.6, 2.9, 3.2, 3.5, 3.9 µs (ver. xxxx[A−O]xx)		t_{OFF_MIN}	−10%	t_{OFF_MIN}	+10%	µs
LLD ADJUST							
LLD Pull Up Current	(ver. xxxxxZx)		I_{LLD}	−21	−20	−19	µA
LLD Time Selection	IC disabled		V_{LLD}			0.3	V
	t_{LLD} = 68 µs			0.40	0.51	0.63	
	t_{LLD} = 130 µs			0.75	0.89	1.03	
	t_{LLD} = 280 µs			1.15	1.32	1.50	
	t_{LLD} = 540 µs			1.68	1.82	1.97	
	t_{LLD} = 1075 µs			2.20	2.50	2.70	
	LLD function disabled			3.10			
LLD Main Time	V_{LLD} = 0.51 V or ver. xxxxxAx		t_{LLD}	53	68	83	µs
	V_{LLD} = 0.89 V or ver. xxxxxBx			100	130	160	
	V_{LLD} = 1.32 V or ver. xxxxxCx			220	280	340	
	V_{LLD} = 1.82 V or ver. xxxxxDx			420	540	660	
	V_{LLD} = 2.45 V or ver. xxxxxEx			840	1075	1310	

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Table 5. ELECTRICAL CHARACTERISTICS (continued)

$-40\ ^{\circ}C \le T_J \le 125\ ^{\circ}C$; V_{CC} = 12 V; C_{DRV} = 0 nF; $R_{MIN_TON} = R_{MIN_TOFF}$ = 10 kΩ or internally set values; V_{LLD} = 3.0 V or LLD internally disabled; $V_{TRIG\ /\ DIS}$ = 0 V; V_{CS} = 4 V, unless otherwise noted. Typical values are at T_J = +25 °C

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
LLD ADJUST						
LLD Reduced Time	Disable mode activated	t_{LLD_RED}		0.5 × t_{LLD}		µs
LLD Blanking Time		t_{LLD_BLK}		0.25 × t_{LLD}		µs
Disable Recovery Time	$t_{MIN\ TOFF}$ = 130 ns	$t_{LLD\ DIS\ REC}$		1.5	3.0	µs
EXCEPTION TIMER						
Exception Time	(ver. xxHxxxx)	t_{EXC}		4 × t_{MIN_TON}		µs
Exception Timer Ratio Accuracy		$Ratio_{EXC}$	−15		+15	%

4. Test signal:

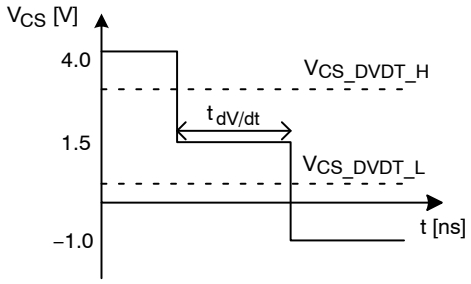


Figure 6. Test Signal

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TYPICAL CHARACTERISTICS

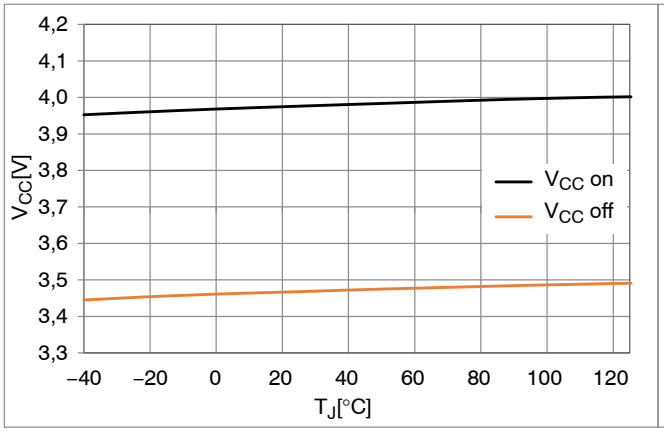


Figure 7. V_{CCON} and V_{CCOFF} Levels

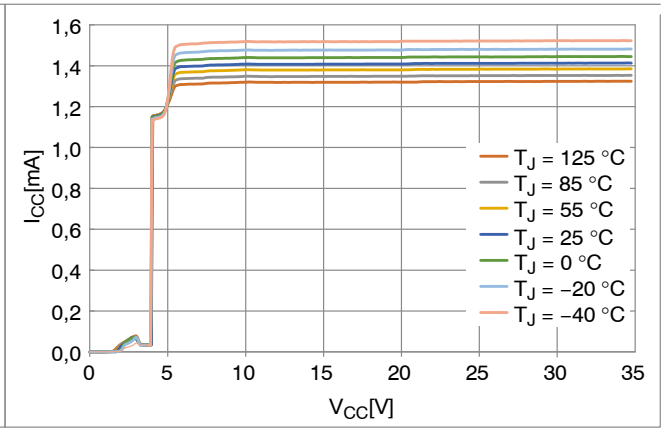


Figure 8. Current Consumption V_{CS} = 4 V

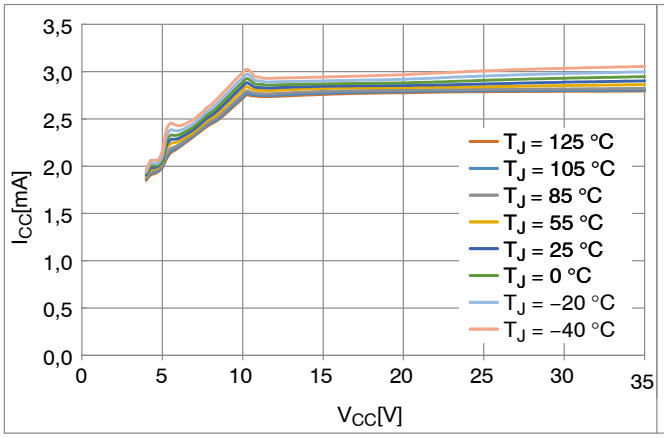


Figure 9. Current Consumption, f_{CS} = 100 kHz, C_{DRV} = 1 nF, Ver. xAxxxxx

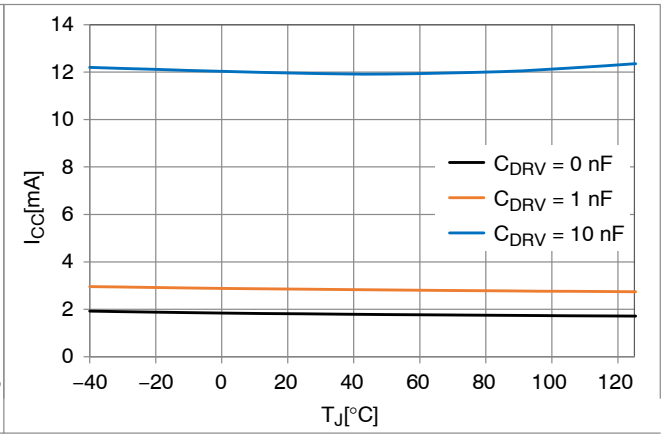


Figure 10. Current Consumption, f_{CS} = 100 kHz, Ver. xAxxxxx

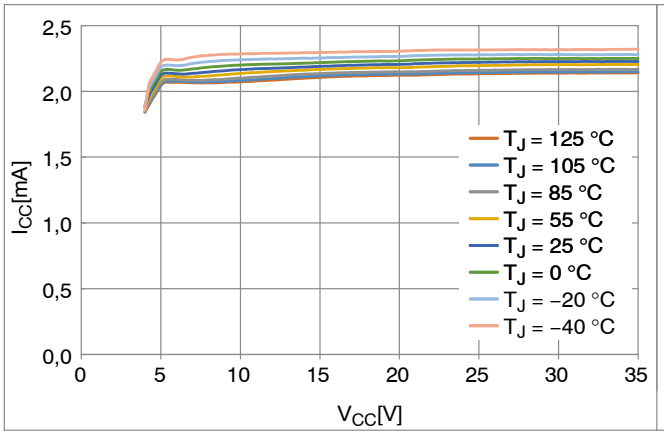


Figure 12. Current Consumption, f_{CS} = 100 kHz, C_{DRV} = 1 nF, Ver. xBxxxx

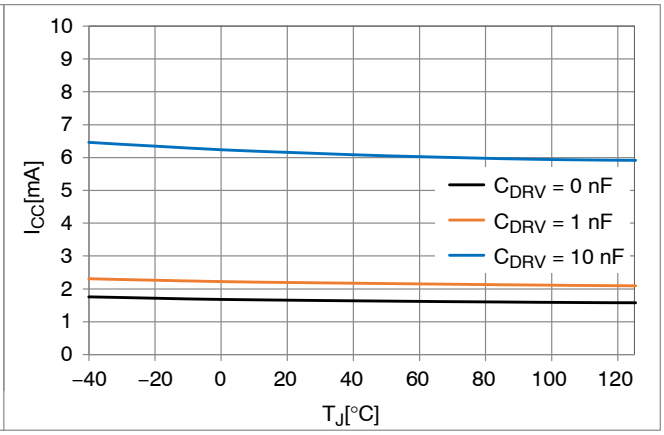


Figure 11. Current Consumption, f_{CS} = 100 kHz, Ver. xBxxxxx

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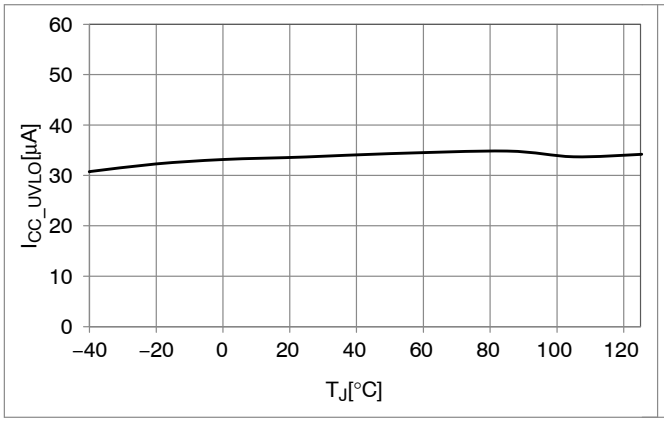


Figure 13. Current Consumption below UVLO, $V_{CC} = V_{CCOFF} - 0.1$ V

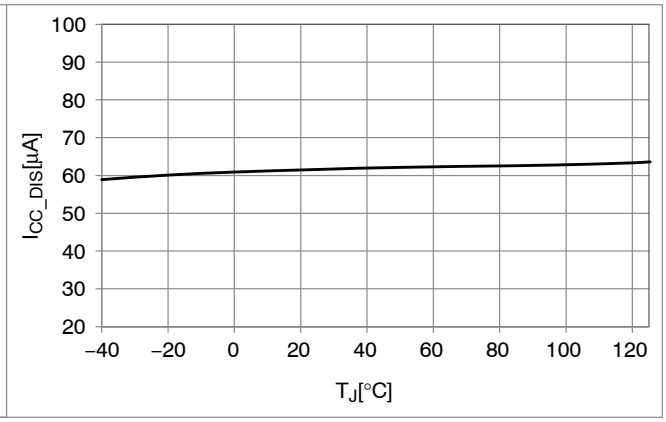


Figure 14. Current Consumption in Disable Mode $V_{CS} = 4$ V, $t > t_{LLD}$

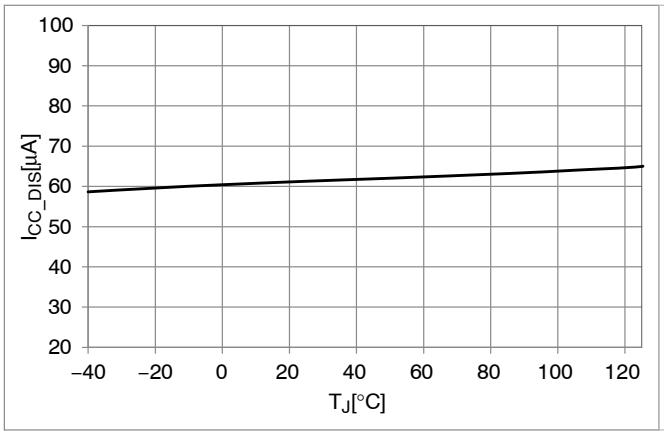


Figure 15. Current Consumption in Disable Mode, $V_{TRIG/DIS} = 5$ V

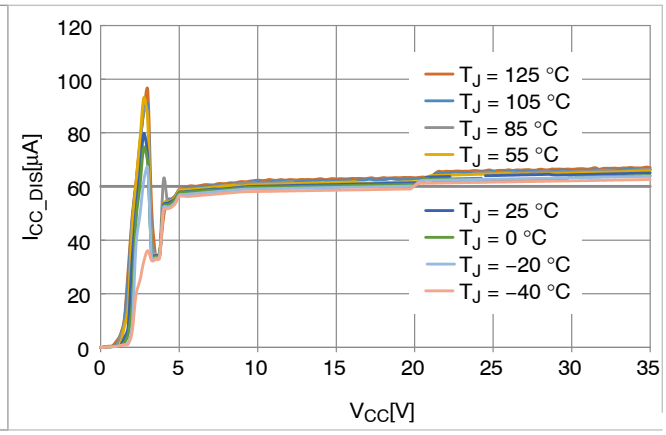


Figure 16. Current Consumption in Disable Mode, $V_{CS} = 4$ V, $t > t_{LLD}$

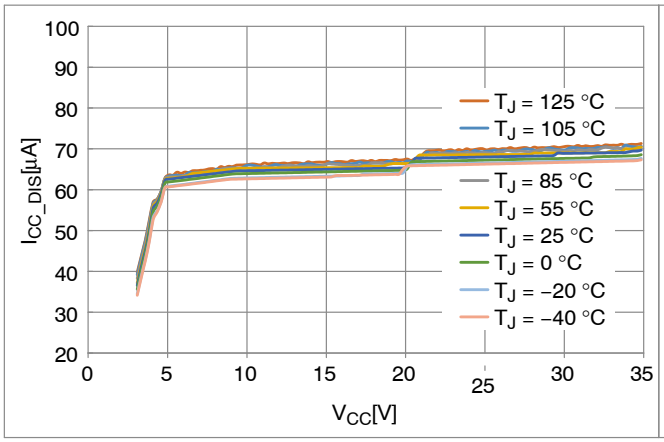


Figure 17. Current Consumption in Disable Mode, $V_{TRIG/DIS} = 5$ V

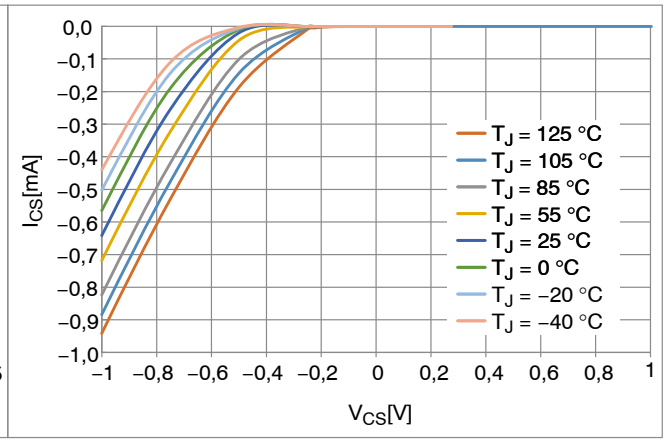


Figure 18. CS Input Current

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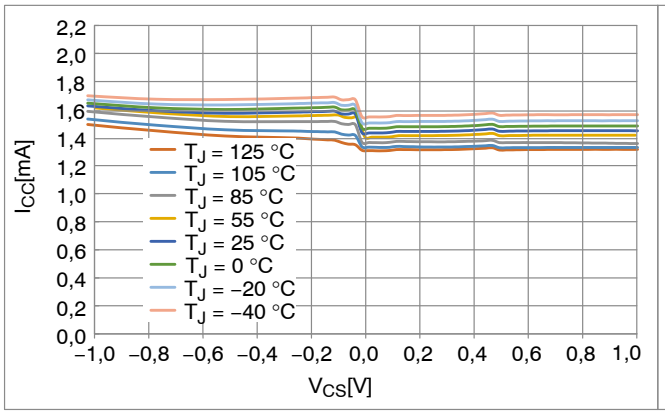


Figure 19. Supply Current vs. CS Voltage

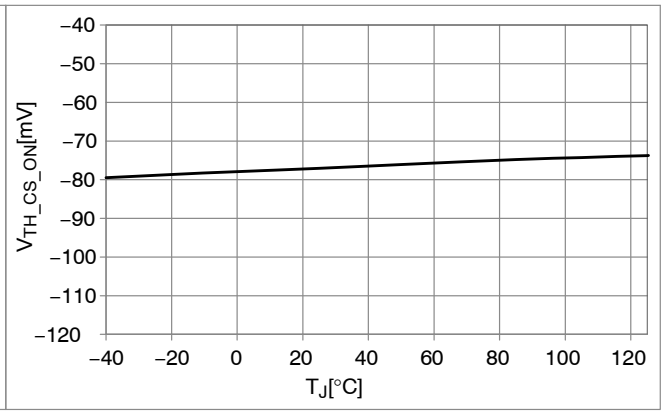


Figure 20. CS Turn−on Threshold

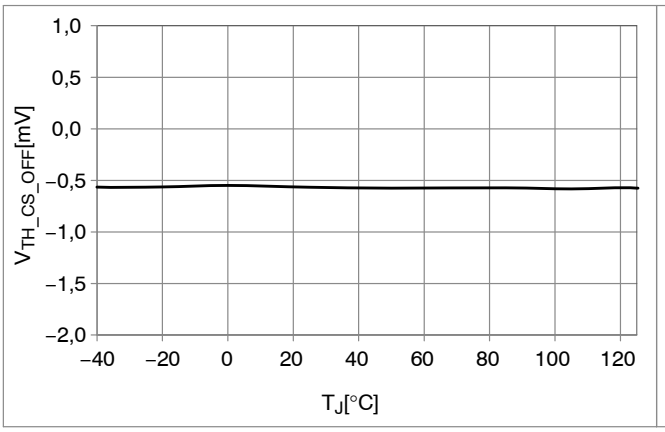


Figure 21. CS turn−off Threshold

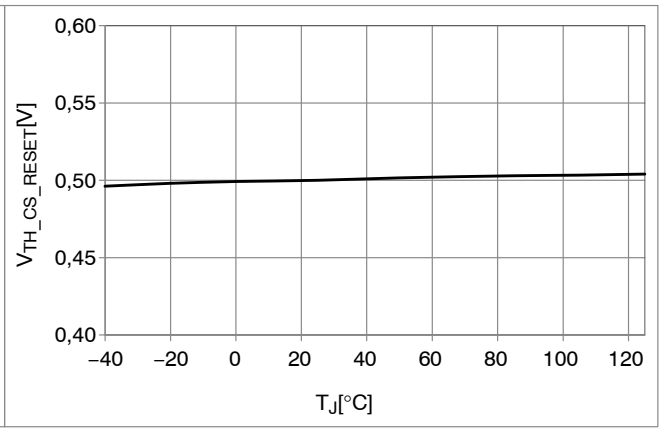


Figure 22. CS Reset Threshold

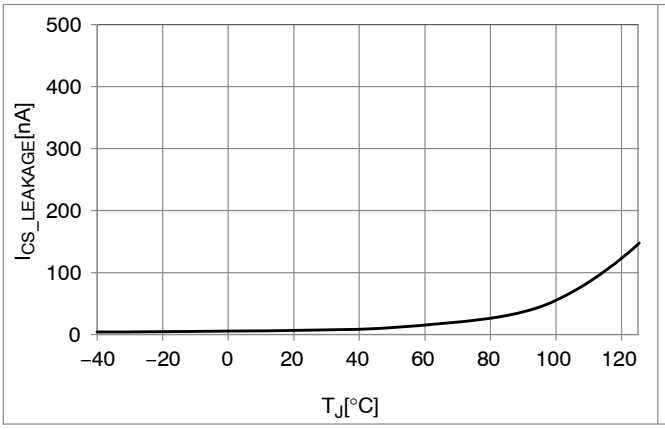


Figure 23. CS Input Leakage V_{CS} = 200 V

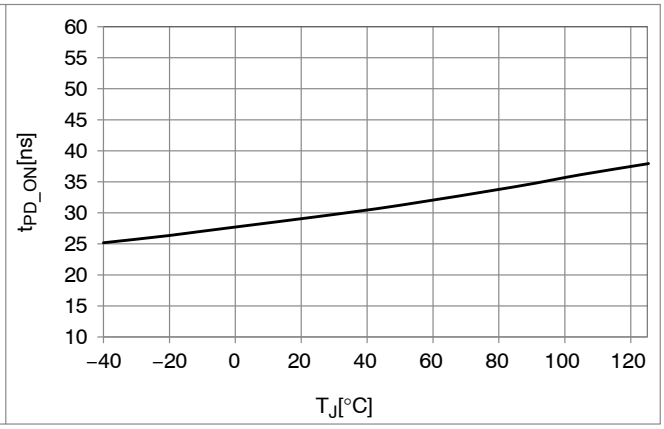


Figure 24. Propagation Delay from CS to DRV Output On

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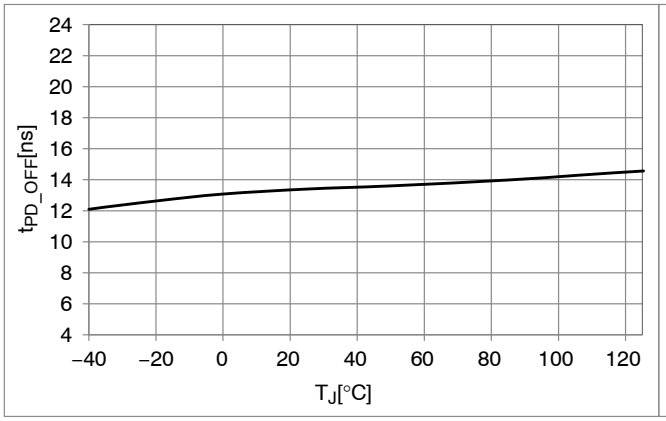


Figure 25. Propagation Delay from CS to DRV Output Off

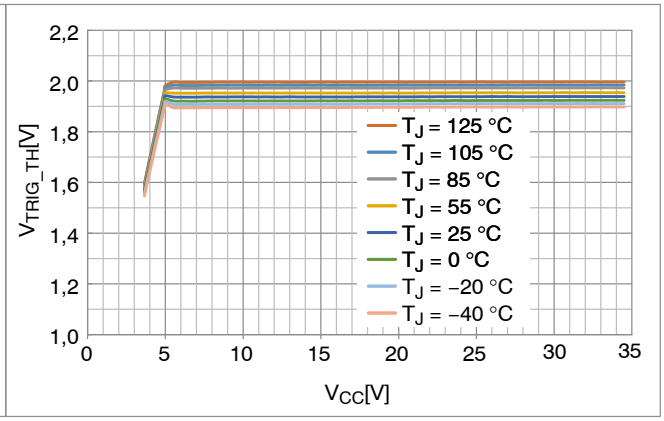


Figure 26. Trigger Pin Threshold

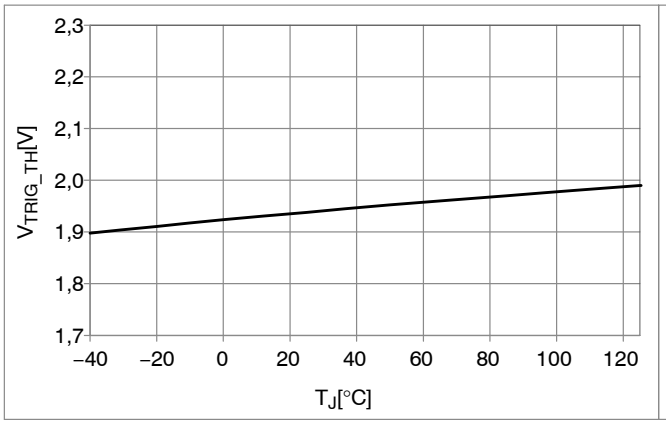


Figure 27. Trigger Pin Threshold

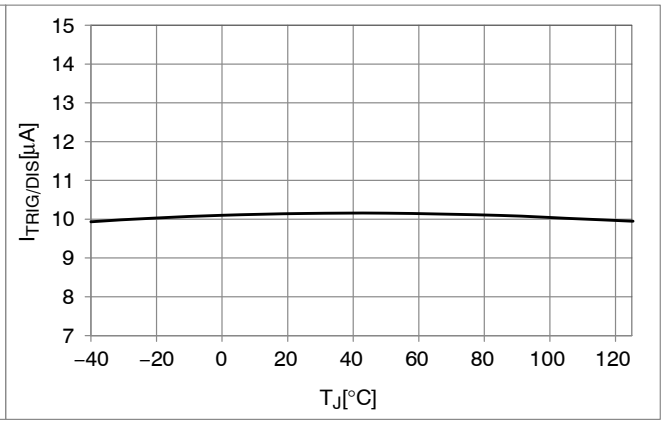


Figure 28. Trigger Pin Pull Down Current

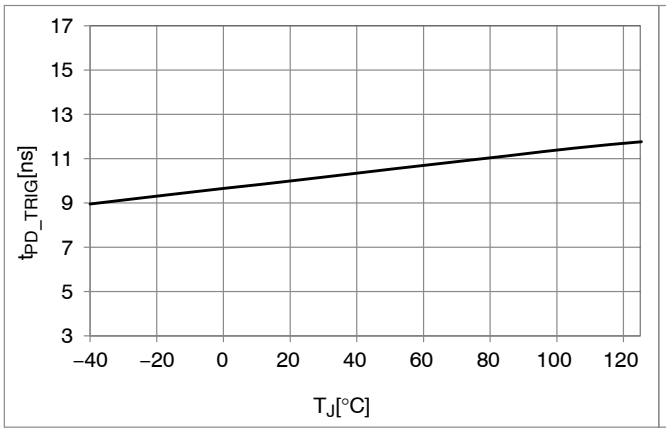


Figure 29. Propagation Delay from TRIG to DRV Output Off

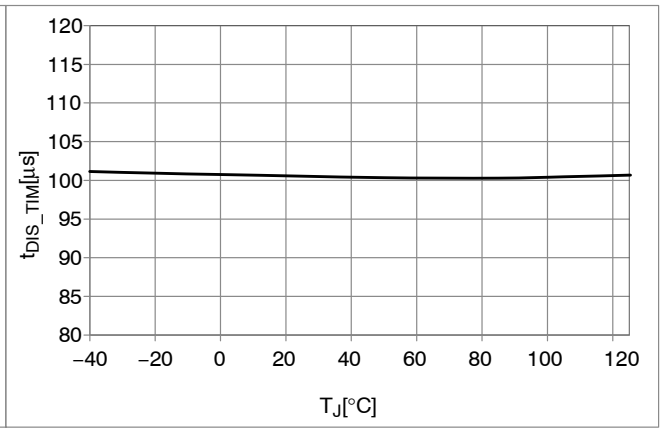


Figure 30. Delay to Disable Mode, $V_{TRIG/DIS}$ = 5 V

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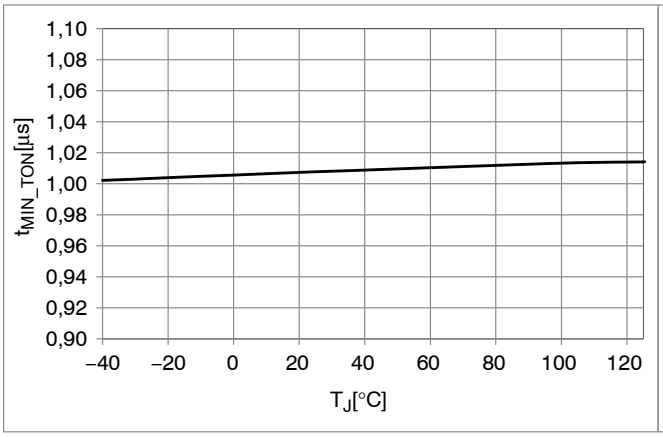


Figure 31. Minimum on Time R_{MIN_TON} = 10 kΩ

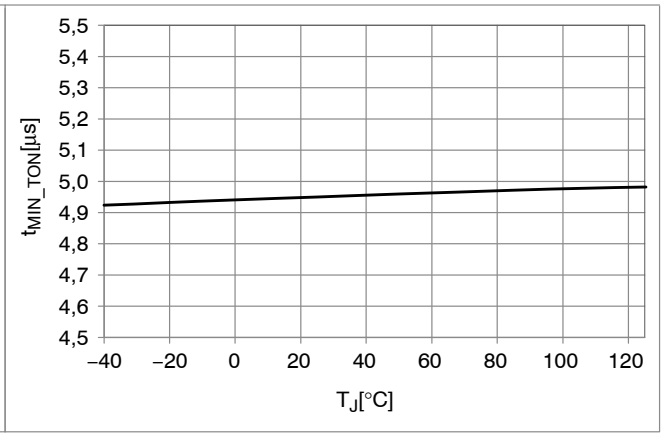


Figure 32. Minimum on Time R_{MIN_TON} = 50 kΩ

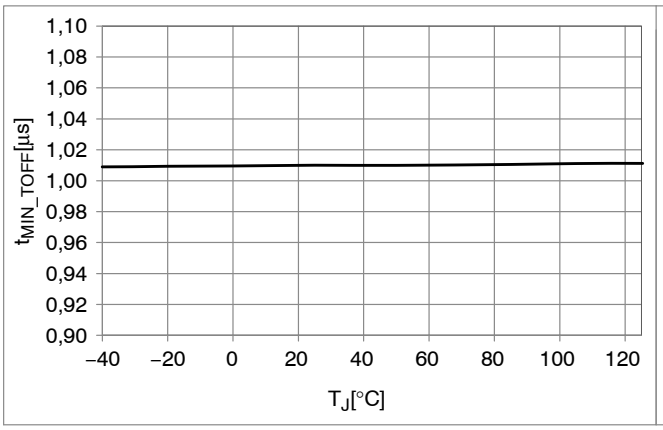


Figure 33. Minimum on Time R_{MIN_TOFF} = 10 kΩ

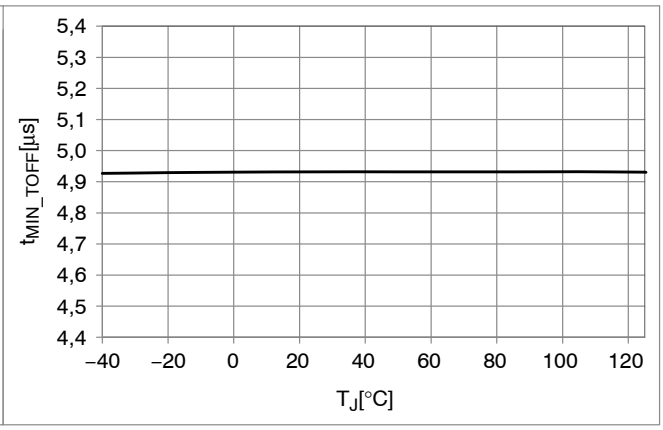


Figure 34. Minimum on Time R_{MIN_TOFF} = 50 kΩ

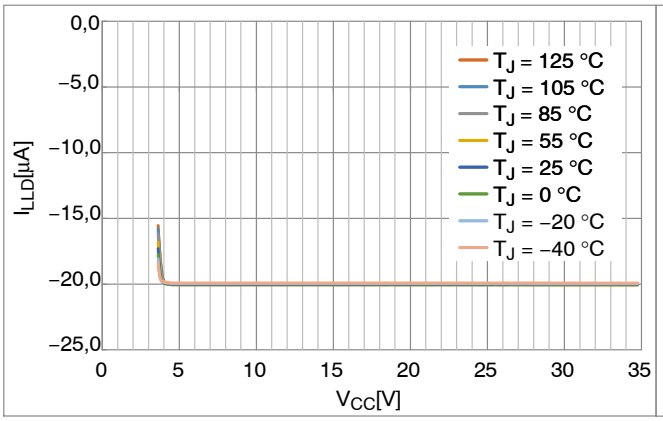


Figure 35. LLD Current, V_{LLD} = 3.0 V

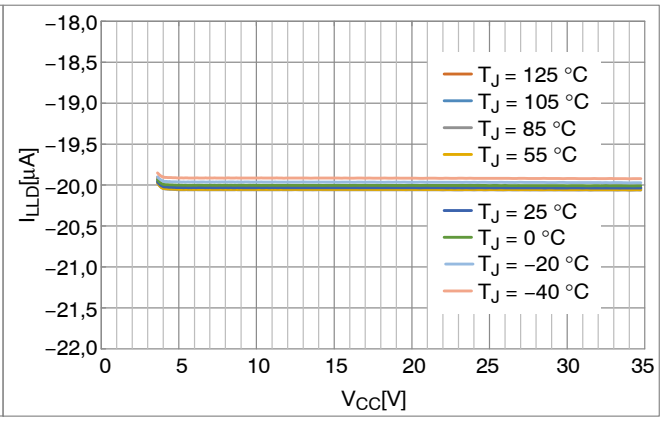


Figure 36. LLD current, V_{LLD} = 2.5 V

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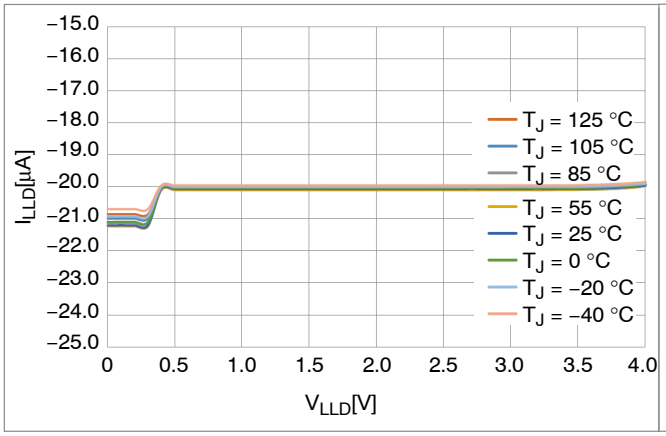


Figure 37. LLD Current

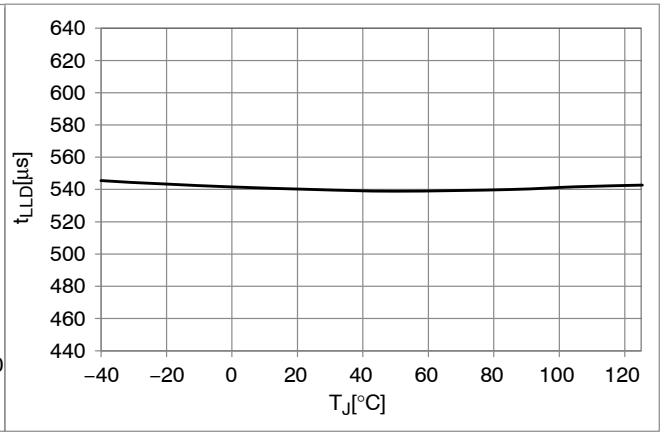


Figure 38. LLD Time, V_{LLD} = 1.82 V (or Internal Option)

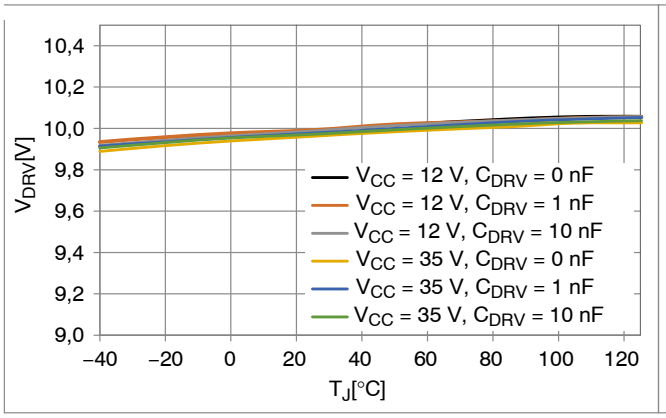


Figure 39. Driver Output Voltage, Ver. xAxxxxx

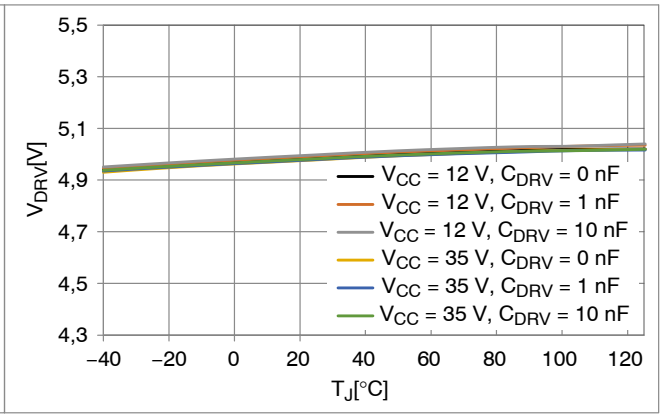


Figure 40. Driver Output Voltage, Ver. xBxxxxx

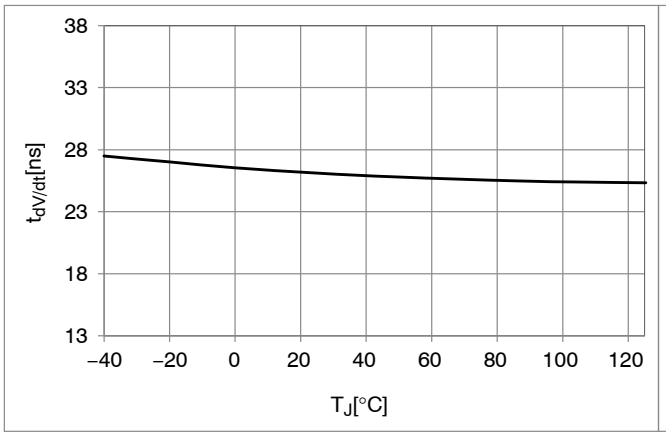


Figure 41. dV/dt Detector Time Threshold, Ver. xxDxxxx

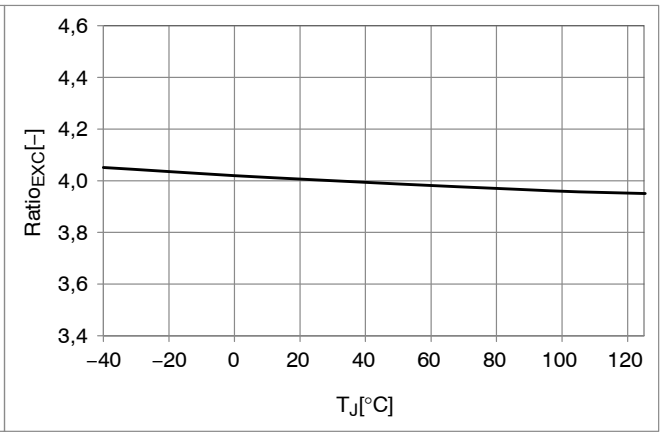


Figure 42. Exception Timer Ratio to t_{MIN_TON}, Ver. xxHxxxx

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GENERAL DESCRIPTION

The NCP4306 is designed to operate either as a standalone IC or as a companion IC to a primary side controller to help achieve efficient synchronous rectification in switch mode power supplies. This controller features a high current gate driver along with high−speed logic circuitry to provide appropriately timed drive signals to a synchronous rectification MOSFET. With its novel architecture, the NCP4306 has enough versatility to keep the synchronous rectification system efficient under any operating mode.

The NCP4306 works from an available voltage with range from 4.0 / 3.5 V to 35 V (typical). The wide V_{CC} range allows direct connection to the SMPS output voltage of most adapters such as notebooks, cell phone chargers and LCD TV adapters.

Precise turn−off threshold of the current sense comparator together with an accurate offset current source allows the user to adjust for any required turn−off current threshold of the SR MOSFET switch using a single resistor. Compared to other SR controllers that provide turn−off thresholds in the range of −10 mV to −5 mV, the NCP4306 offers a turn−off threshold of 0 mV. When using a low R_{DS_ON} SR (1 mΩ) MOSFET our competition, with a −10 mV turn off, will turn off with 10 A still flowing through the SR FET, while our 0 mV turn off turns off the FET at 0 A; significantly reducing the turn−off current threshold and improving efficiency. Many of the competitor parts maintain a drain source voltage across the MOSFET causing the SR MOSFET to operate in the linear region to reduce turn−off time. Thanks to the 6 A sink current of the NCP4306 significantly reduces turn off time allowing for a minimal drain source voltage to be utilized and efficiency maximized.

To overcome false triggering issues after turn−on and turn−off events, the NCP4306 provides adjustable minimum on−time and off−time blanking periods. Blanking times can be set internally during production or adjusted independently of IC VCC using external resistors connected to GND (internal or external option depends on IC variant). If needed, externally set blanking periods can be modulated using additional components.

An extremely fast turn−off comparator, implemented on the current sense pin, allows for NCP4306 implementation in CCM applications without any additional components or external triggering.

An ultrafast trigger input offers the possibility to further increase efficiency of synchronous rectification systems operated in CCM mode (for example, CCM flyback or forward). The time delay from trigger input to driver turn off event is t_{PD_TRIG}. Additionally, the trigger input can be used to disable the IC and activate a low consumption standby mode. This feature can be used to decrease standby consumption of an SMPS. If the trigger input is not wanted than the trigger pin can be tied to GND.

An output driver features capability to keep SR transistor turned−off even when there is no supply voltage for the NCP4306. SR transistor drain voltage goes up and down during SMPS operation and this is transferred through drain gate capacitance to gate and may open transistor. The NCP4306 keeps DRV pin pulled low even without any supply voltage and thanks to this the risk of turned−on SR transistor before enough V_{CC} is applied to the NCP4306 is eliminated.

Finally, the NCP4306 features a Light Load Detection function that can be set internally or externally at LLD pin by resistor connected to ground. This function detects light load or no load conditions and during them between conduction phases it decreases current consumption. This helps to improve SMPS efficiency. If LLD function is not needed pin can be left open.

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SUPPLY SECTION

Supply voltage should be connected to VCC pin. Minimum voltage for proper operation is 4.0 / 3.5 V typically and maximum level is 35 V. Decoupling capacitor between VCC and GND pin is needed for proper operation and its recommended value is 1 μF. If IC is supplied from SMPS output voltage, few ohm resistor is recommended between SMPS output voltage and VCC pin. Resistor task is to divide decoupling cap from output to avoid closing HF currents through NCP4306 decoupling cap, because these currents may causes drops at GND connection that affects SR transistor sensing and incorrect SR transistor turn−off.

SR transistor is usually used in low side configuration (placed in return path), but it may be also used in high side configuration (placed in positive line). It is not possible to use SMPS V_{OUT} for SR supply in high side configuration so it is needed to provide supply differently. One possibility is to use auxiliary winding as shown in Figure 43. Voltage from auxiliary winding is rectified, filtered and use as supply voltage.

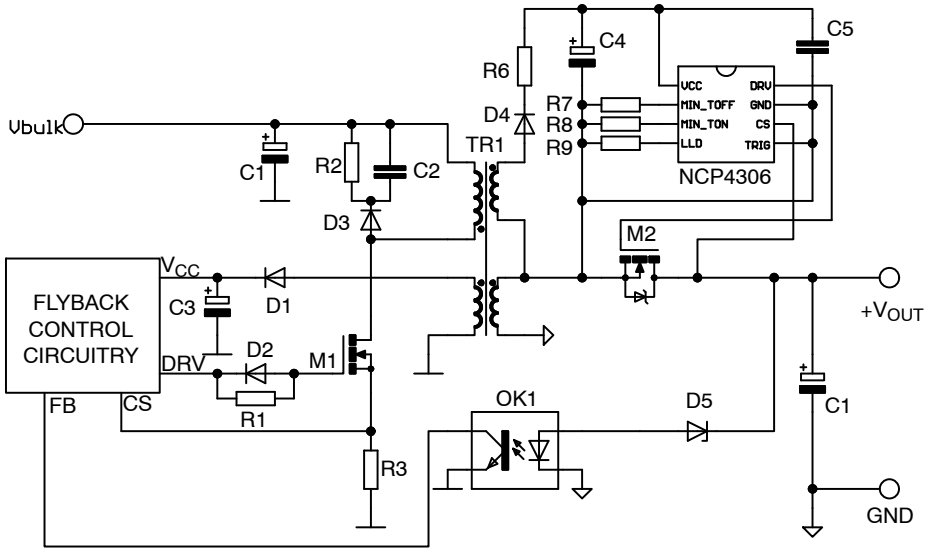


Figure 43. High Side Configuration Supplied from Auxiliary Winding

If auxiliary winding is not acceptable, transformer forward voltage can be used as supply source (Figure 44). Forward voltage is regulated by simple voltage regulator to fit NCP4306 VCC restriction. Penalty for this solution is slightly lower efficiency.

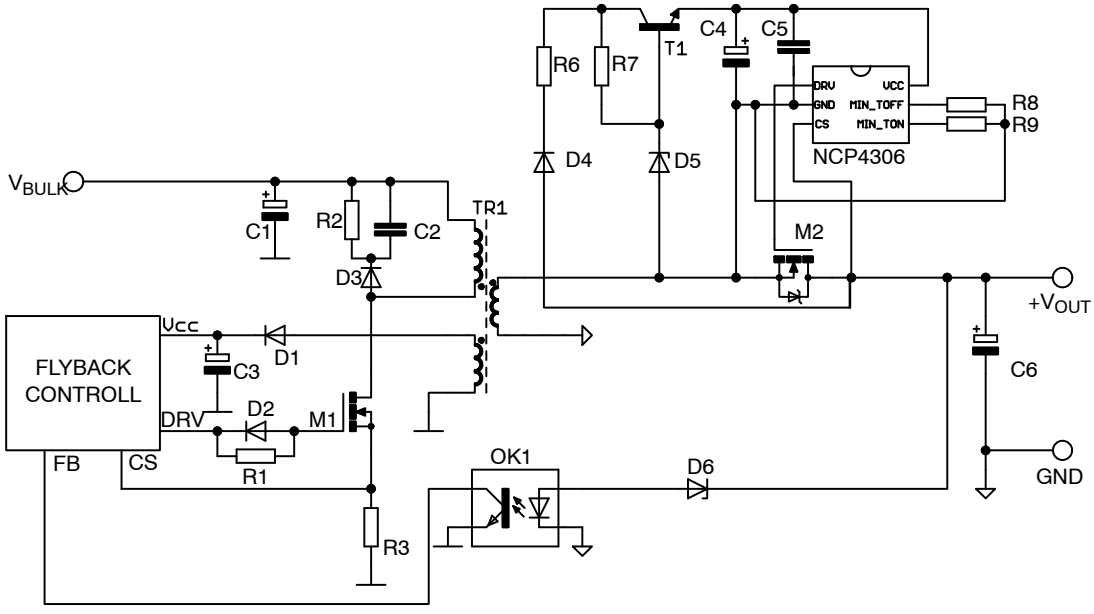


Figure 44. High Side Configuration Supplied from Transformer Forward Voltage

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Auxiliary winding or forward voltage can be used as supply source also for low side configuration if V_{OUT} is not high enough (Figure 45). Do not focus just on SR controller UVLO, but also on SR transistor characteristics. Some transistors may be not turned−on enough even at 5 V so in these case SR controller supply voltage should be increased.

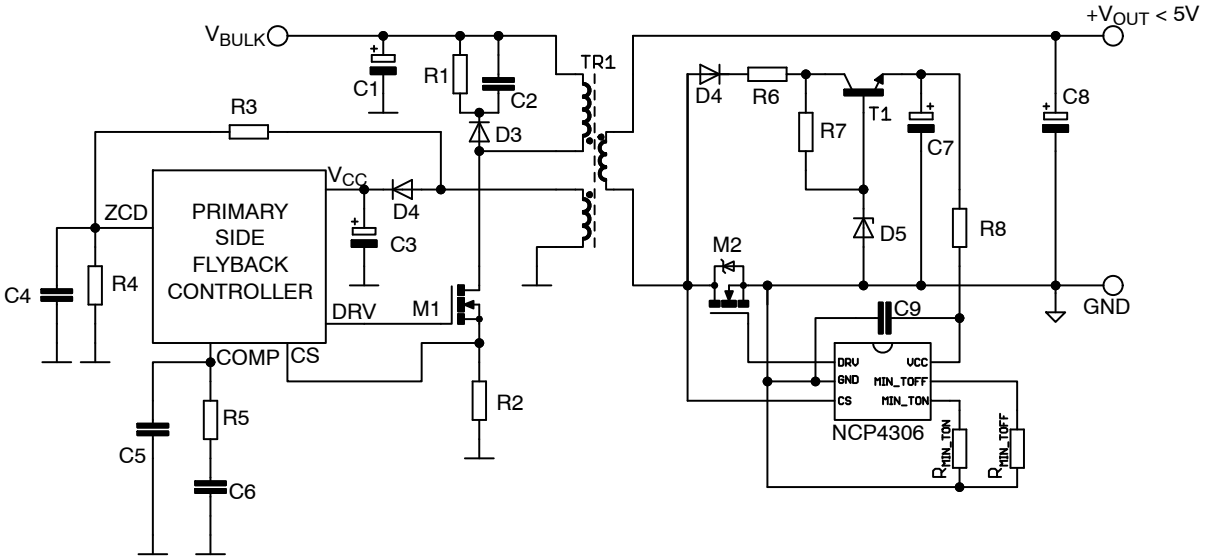


Figure 45. Low Side Configuration Supplied from Transformer Forward Voltage for Low V_{OUT} SMPS

Current Sense Input

Figure 46 shows the internal connection of the CS circuitry on the current sense input. When the voltage on the secondary winding of the SMPS reverses, the body diode of M1 starts to conduct current and the voltage of M1's drain drops approximately to −1 V. Once the voltage on the CS pin is lower than $V_{TH_CS_ON}$ threshold, M1 is turned−on. Because of parasitic impedances, significant ringing can occur in the application. To overcome false sudden turn−off due to mentioned ringing, the minimum conduction time of the SR MOSFET is activated. Minimum conduction time can be adjusted using the R_{MIN_TON} resistor or can be chosen from internal fixed values.

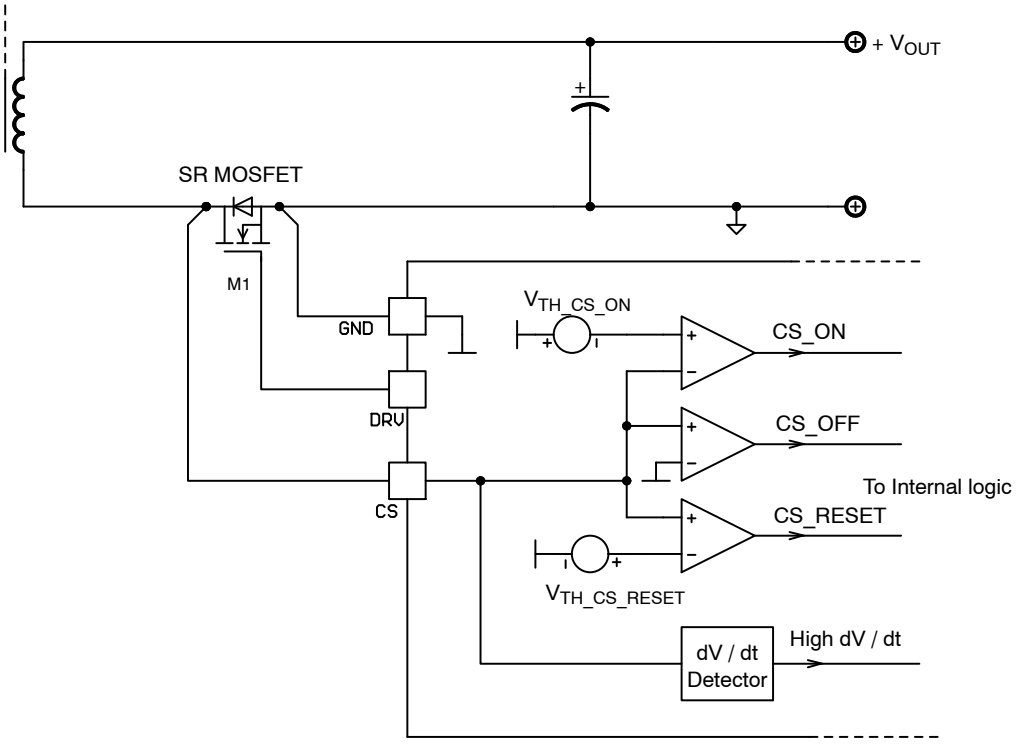


Figure 46. Current Sensing Circuitry Functionality

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The SR MOSFET is turned−off as soon as the voltage on the CS pin is higher than $V_{TH_CS_OFF}$ (typically −0.5 mV). For the same ringing reason, a minimum off−time timer is asserted once the V_{CS} goes above $V_{TH_CS_RESET}$. The minimum off−time can be externally adjusted using R_{MIN_TOFF} resistor or can be chosen from internally fixed values (depends on version). The minimum off−time generator can be re−triggered by MIN_TOFF reset comparator if some spurious ringing occurs on the CS input after SR MOSFET turn−off event. This feature significantly simplifies SR system implementation in flyback converters.

In an LLC converter the SR MOSFET M1 channel conducts while secondary side current is decreasing (refer to Figure 47). Therefore the turn−off current depends on MOSFET R_{DSON}. The −0.5 mV threshold provides an optimum switching period usage while keeping enough time margin for the gate turn−off. To ensure proper switching, the min_t_{OFF} timer is reset, when the V_{DS} of the MOSFET rings and falls down past the $V_{TH_CS_RESET}$. The minimum off−time needs to expire before another drive pulse can be initiated. Minimum off−time timer is started again when V_{DS} rises above $V_{TH_CS_RESET}$.

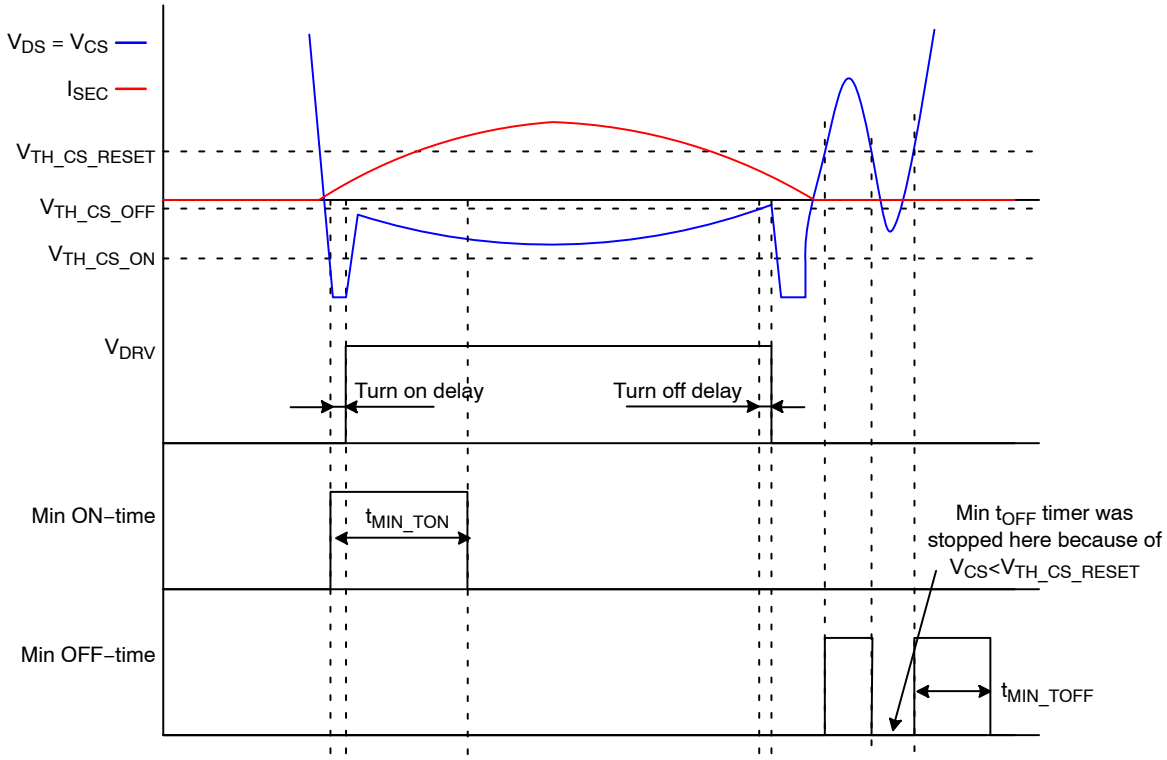


Figure 47. CS Input Comparators Thresholds and Blanking Periods Timing in LLC

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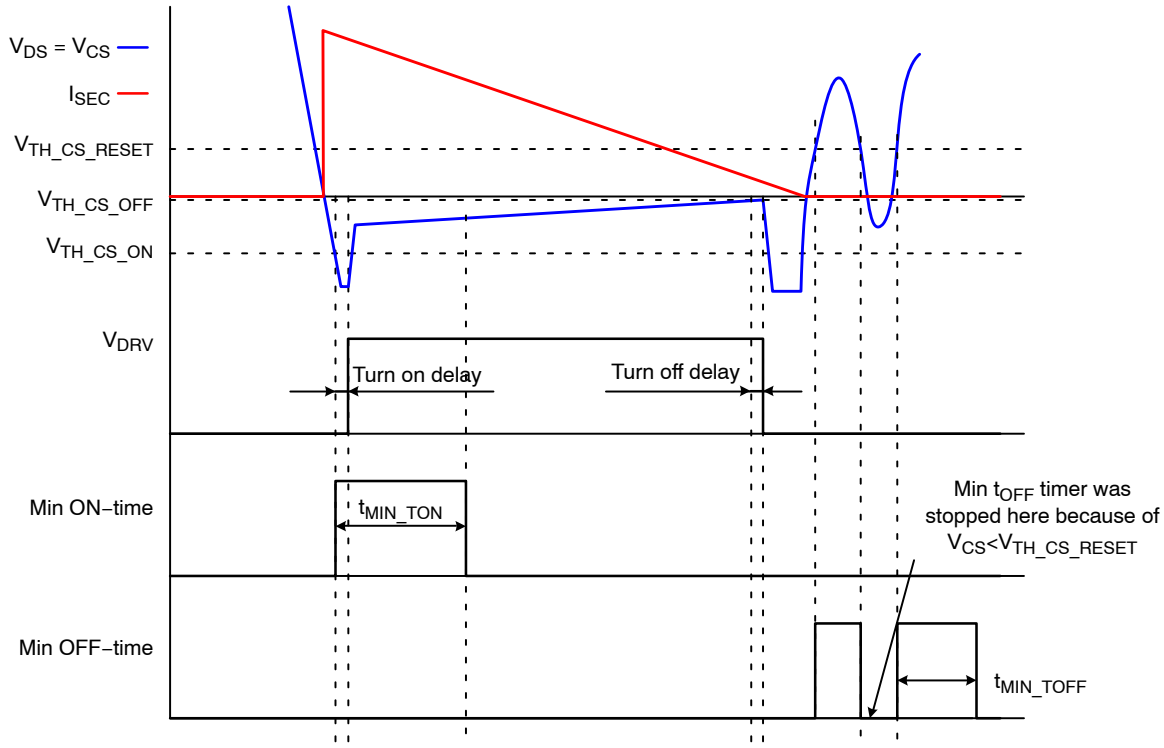


Figure 48. CS Input Comparators Thresholds and Blanking Periods Timing in Flyback

SR Transistor Selection

An SMPS designer should consider all important SR MOSFET parameters for its optimum selection in given application and not stick only to the lowest $R_{DS(ON)}$ requirement. The lower $R_{DS(ON)}$ device is selected the more significant role the lead parasitic inductances play in turn−of threshold sensing i.e. the more premature turn−off will happen (refer to section below for parasitic inductance impact to V_{DS} sensing). The lower $R_{DS(ON)}$ switch also usually features higher input capacitance that increases driving losses. The higher output capacitance and higher reverse recovery charge of body diode then results in higher drain−to source voltage peaks in CCM applications. Thus the higher $R_{DS(ON)}$ MOSFET can usually provide better or at least same efficiency result when compare to a switch which was selected with minimum available $R_{DS(ON)}$ resistance requirement only.

Sensing V_{DS} drop across the SR transistor, which is ideally product of transistor's $R_{DS(ON)}$ and secondary side current, is affected by voltage drop at parasitic inductance of package (bonding, leads, …) and PCB layout−(refer to Figure 49). The current that flows through the SR MOSFET experiences a high $\Delta i(t) / \Delta t$ that induces an error voltage on the SR MOSFET bonds and leads due to their parasitic inductance. This error voltage is proportional to the derivative of the SR MOSFET current; and shifts the CS input voltage to zero when significant current still flows through the MOSFET channel. As a result, the SR MOSFET is turned−off prematurely and the efficiency of the SMPS is not optimized – refer to Figure 50 for a better understanding.

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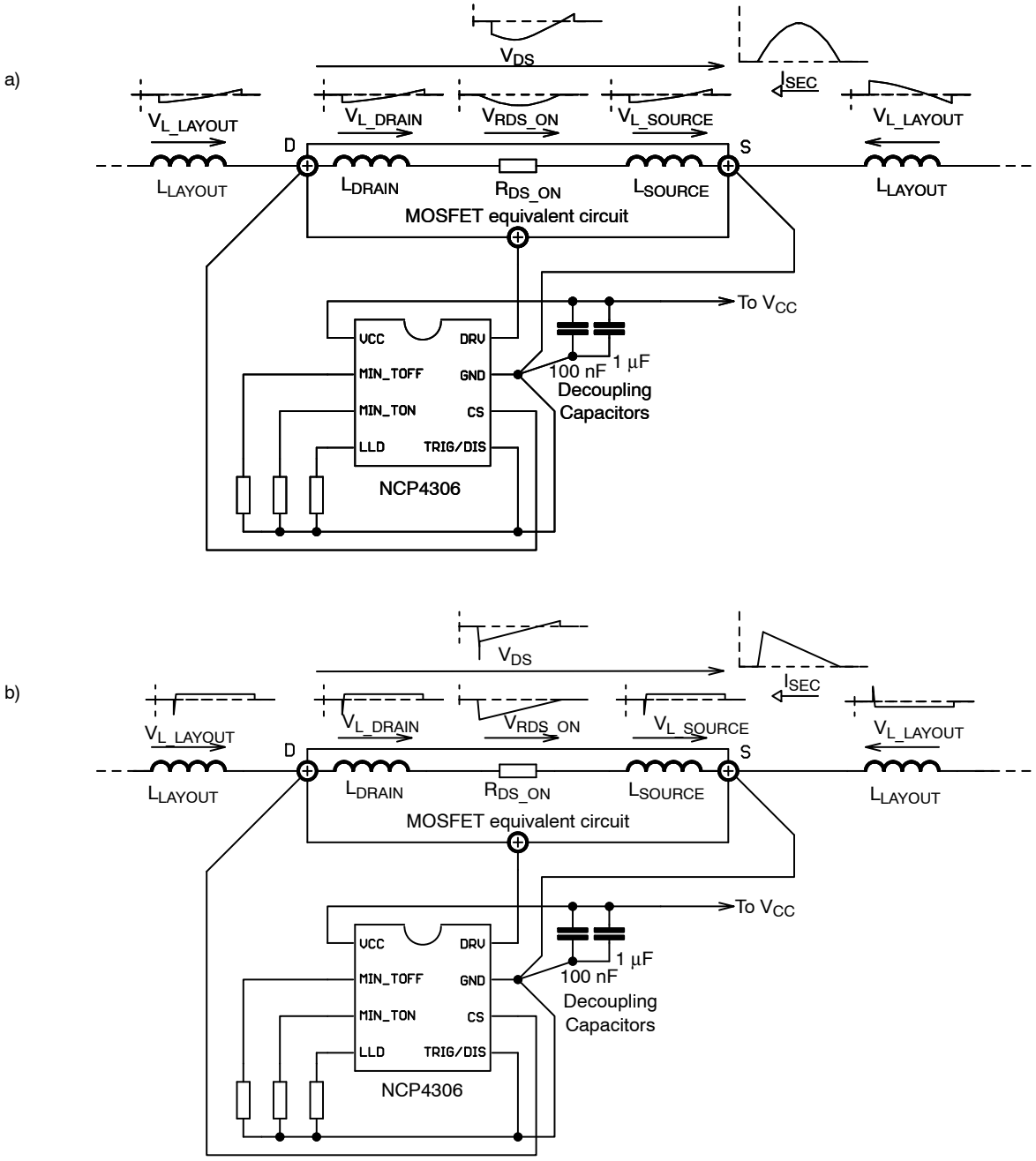


Figure 49. SR System Connection Including MOSFET and Layout Parasitic Inductances in a) LLC and b) Flyback Application

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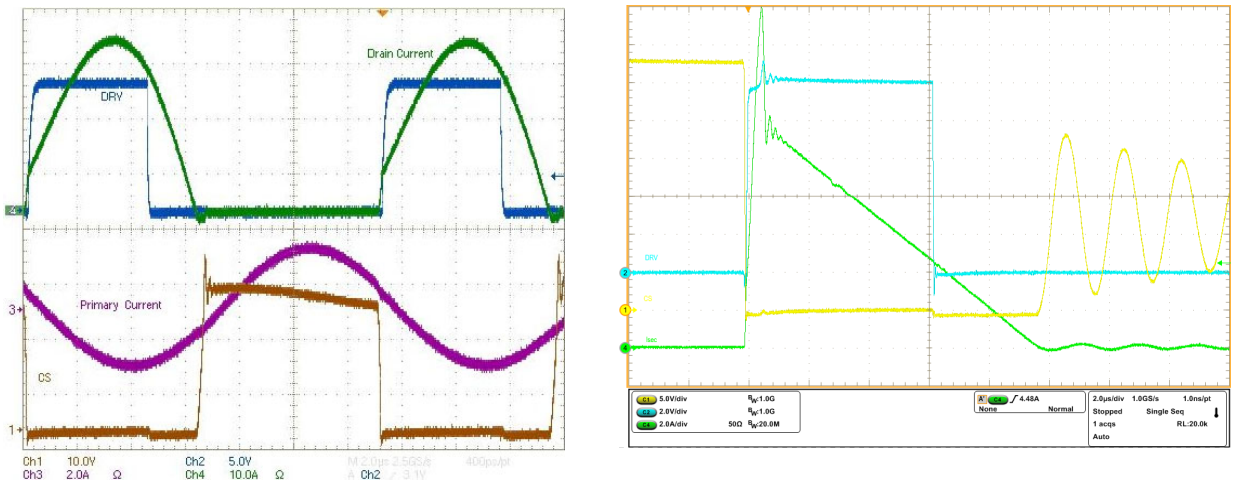


Figure 50. Waveforms from SR System Implemented in a) LLC and b) Flyback Application and Using MOSFET in TO220 Package With Long Leads – SR MOSFET channel Conduction Time is Reduced

Note that the efficiency impact caused by the error voltage due to the parasitic inductance increases with lower MOSFETs R_{DS_ON} and / or higher operating frequency.

It is thus beneficial to minimize SR MOSFET package leads length in order to maximize application efficiency. The optimum solution for applications with high secondary current Δi / Δt and high operating frequency is to use lead−less SR MOSFET i.e. SR MOSFET in SMT package. The parasitic inductance of a SMT package is negligible causing insignificant CS turn−off threshold shift and thus minimum impact to efficiency (refer to Figure 51).

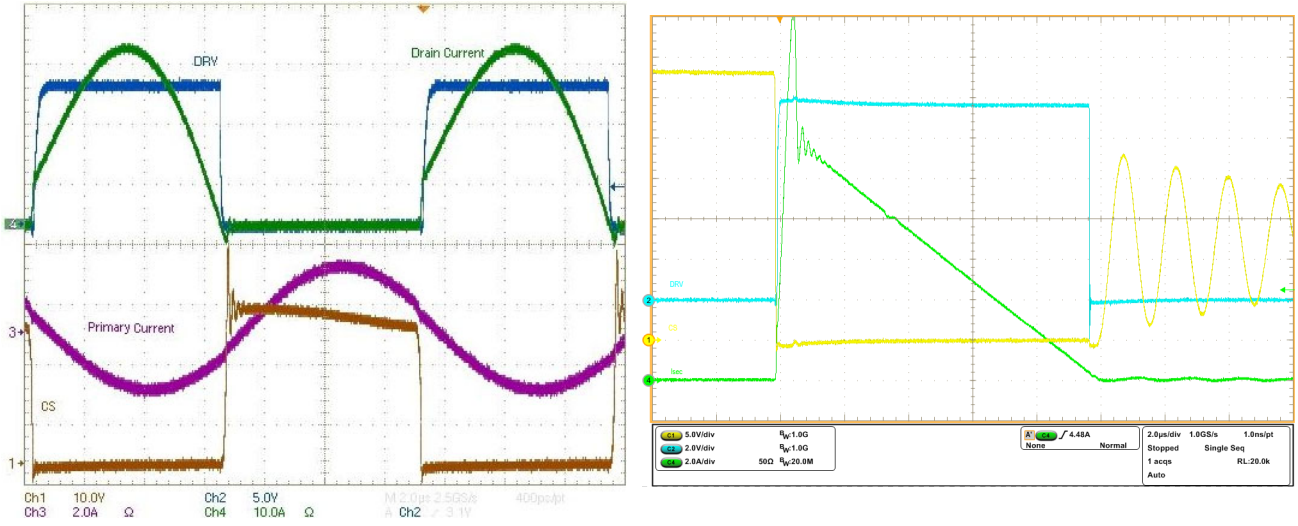


Figure 51. Waveforms from SR System Implemented in a) LLC b) Flyback Application and Using MOSFET in SMT Package with Minimized Parasitic Inductance – SR MOSFET Channel Conduction Time is Optimized

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It can be deduced from the above paragraphs on the induced error voltage and parameter tables that turn−off threshold precision is quite critical. If we consider a SR MOSFET with R_{DS_ON} of 1 mΩ, the 1 mV error voltage on the CS pin results in a 1 A turn−off current threshold difference; thus the PCB layout is very critical when implementing the SR system. Note that the CS turn−off comparator is referred to the GND pin. Any parasitic impedance (resistive or inductive – even on the magnitude of mΩ and nH values) can cause a high error voltage that is then evaluated by the CS comparator. Ideally the CS turn−off comparator should detect voltage that is caused by secondary current directly on the SR MOSFET channel resistance. In reality there will be small parasitic impedance on the CS path due to the bonding wires, leads and soldering. To assure the best efficiency results, a Kelvin connection of the SR controller to the power circuitry should be implemented. The GND pin should be connected to the SR MOSFET source soldering point and current sense pin should be connected to the SR MOSFET drain soldering point – refer to Figure 49. Using a Kelvin connection will avoid any impact of PCB layout parasitic elements on the SR controller functionality; SR MOSFET parasitic elements will still play a role in attaining an error voltage. Figure 52 and Figure 53 show examples of SR system layouts using MOSFETs in D2PAK and SO8FL packages.

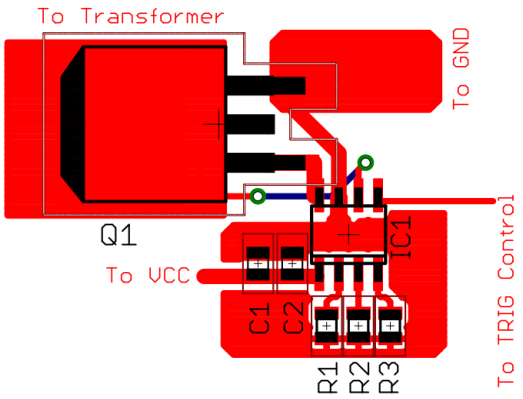


Figure 52. Recommended Layout When Using SR MOSFET in D2PAK Package

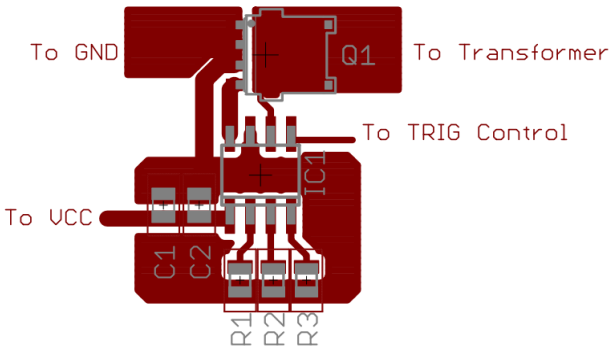


Figure 53. Recommended Layout When Using SR MOSFET in SMT Package SO8 FL

Trigger / Disable input

The NCP4306 features an ultrafast trigger input that exhibits a maximum of t_{PD_TRIG} delay from its activation to the start of SR MOSFET turn−off of process. This input can be used in applications operated in deep Continues Conduction Mode (CCM) to further increase efficiency and / or to activate disable mode of the SR driver in which the consumption of the NCP4306 is reduced to maximum of I_{CC_DIS}.

NCP4306 is capable to turn−off the SR MOSFET reliably in CCM applications just based on CS pin information only, without using the trigger input. However, natural delay of the ZCD comparator and DRV turn−off delay increase overlap between primary and secondary MOSFETs switching (also known as cross conduction). If one wants to achieve absolutely maximum efficiency with deep CCM applications, then the trigger signal coming from the primary side should be applied to the trigger pin. It is good to set trigger pulse in way there is just short overlap between primary and secondary switches. Short overlap is usually advantageous than leaving end of conduction phase on body diode. Reason is body diode has usually longer recovery time and resulting overlap time (simultaneously conduction primary and secondary side switches) is longer. There are several possibilities for transferring the trigger signal from the primary to the secondary side – refer to Figure 68 and Figure 69.

The trigger signal is blanked for t_{TRIG_BLANK} after the DRV turn−on process has begun. The blanking technique is used to increase trigger input noise immunity against the parasitic ringing that is present during the turn on process due to the SMPS layout. The trigger input is supersedes the CS input except trigger blanking period. TRIG / DIS signal turns the SR MOSFET off or prohibits its turn−on when the TRIG / DIS pin is pulled above V_{TRIG_TH}.

The SR controller enters disable mode when the trigger pin is pulled−up for more than t_{DIS_TIM}. In disable mode the IC consumption is significantly reduced. To recover from disable mode and enter normal operation, the TRIG / DIS pin has to be pulled low at least for t_{DIS_END}.

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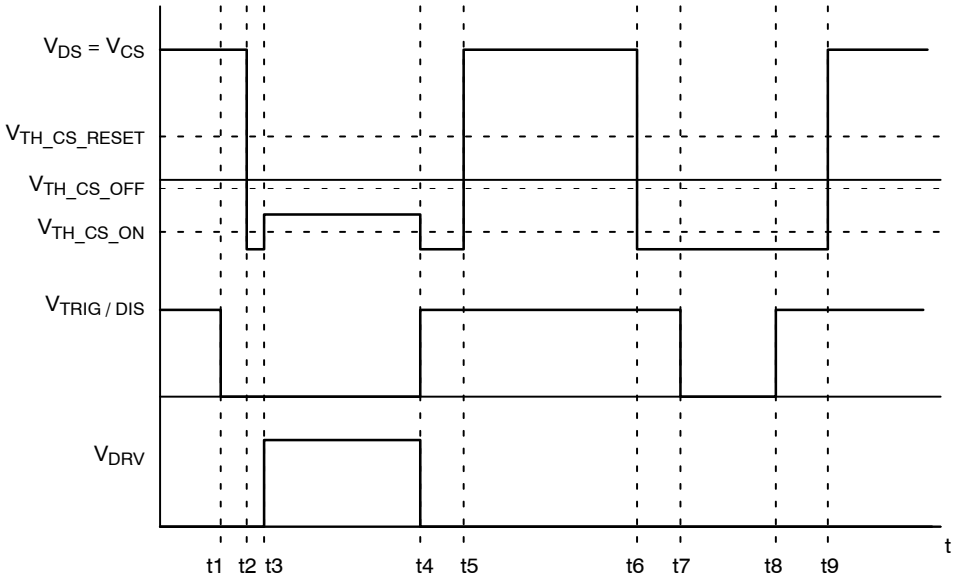


Figure 54. Trigger Input Functionality Waveforms Using the Trigger to Turn−off and Block the DRV Signal

Figure 54 shows basic TRIG / DIS input functionality. At t1 the TRIG / DIS pin is pulled low to enter into normal operation. At t2 the CS pin is dropped below the $V_{TH_CS_ON}$, signaling to the NCP4306 to start to turn the SR MOSFET on. At t3 the NCP4306 begins to drive the MOSFET. At t4, the SR MOSFET is conducting and the TRIG / DIS pin is pulled high. This high signal on the TRIG / DIS pin almost immediately turns off the drive to the SR MOSFET, turning off the MOSFET. The DRV is not turned−on in other case (t6) because the trigger pin is high in the time when CS pin signal crosses turn−on threshold. This figure clearly shows that the DRV can be asserted only on falling edge of the CS pin signal in case the trigger input is at low level (t2).

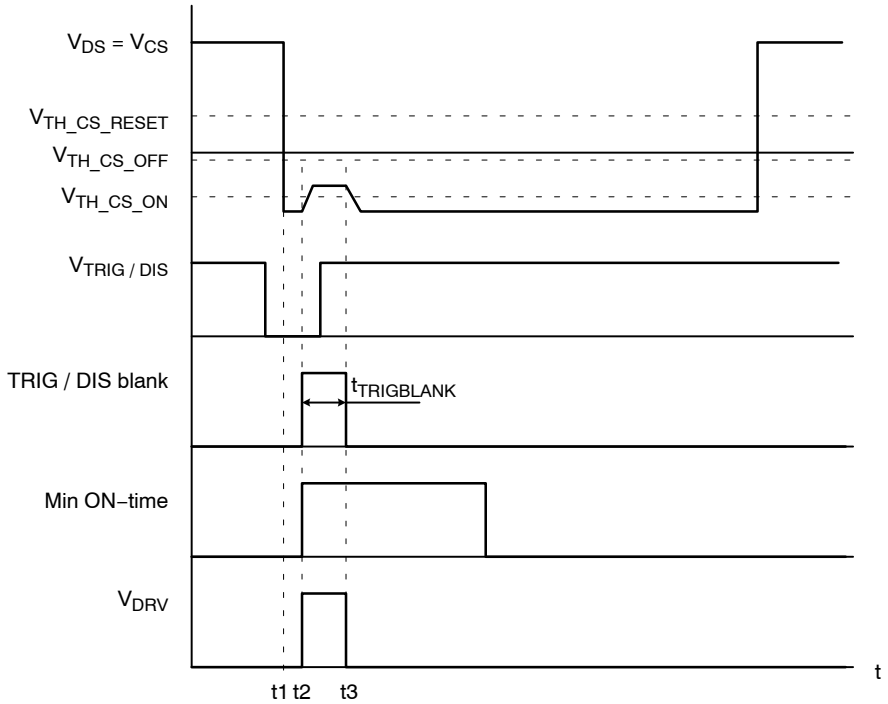


Figure 55. Trigger Input Functionality Waveforms – Trigger Blanking

In Figure 55 above, at time t1 the CS pin falls below the $V_{TH_CS_ON}$ while the Trigger is low setting in motion the DRV signal that appears at t2. At time t2 the DRV signal and Trigger blanking clock begin. TRIG / DIS signal goes high shortly after time t2. Due to the Trigger blanking clock (t_{TRIG_BLANK}) the Trigger's high signal does not affect the DRV signal until the t_{TRIG_BLANK} timer has expired. At time t3 the TRIG / DIS signal is reevaluated and the DRV

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signal is turned off. The TRIG / DIS input is blanked for t_{TRIG_BLANK} after DRV set signal to avoid undesirable behavior during SR MOSFET turn−on event. The blanking time in combination with high threshold voltage (V_{TRIG_TH}) prevent triggering on ringing and spikes that are present on the TRIG / DIS input pin during the SR MOSFET turn−on process. Controller's response to the narrow pulse on the TRIG / DIS pin is depicted in Figure 55 – this short trigger pulse enables to turn the DRV on for t_{TRIG_BLANK}. Note that this case is valid only if device not entered disable mode before.

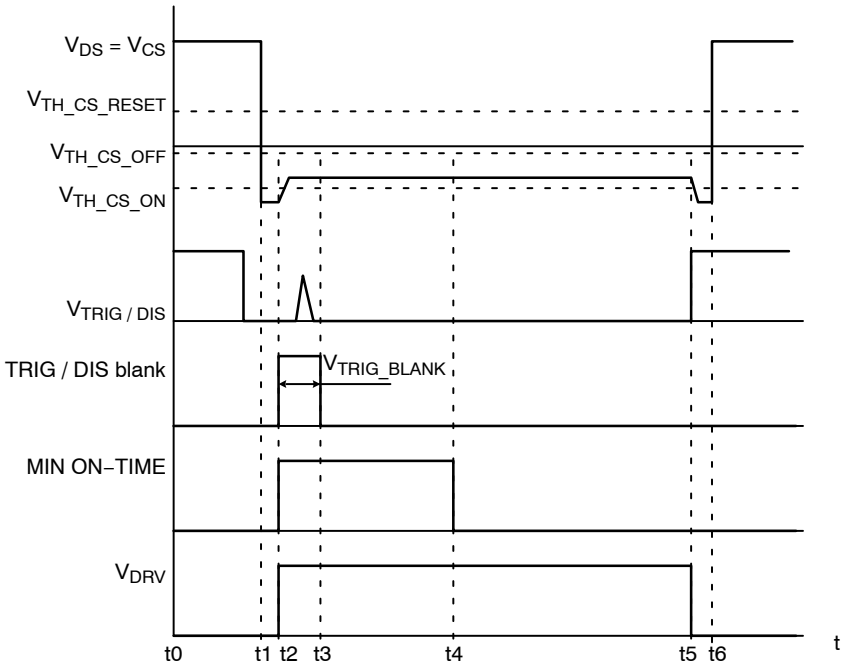


Figure 56. Trigger Input Functionality Waveforms – Trigger Blanking Acts Like a Filter

Figure 56 above shows almost the same situation as in Figure 55 with one main exception; the TRIG / DIS signal was not high after trigger blanking timer expired so the DRV signal remains high. The advantage of the trigger blanking time during DRV turn−on is evident from Figure 56 since it acts like a filter on the TRIG / DIS pin. Rising edge of the DRV signal may cause spikes on the trigger input. If it wasn't for the TRIG / DIS blanking these spikes, in combination with ultra−fast performance of the trigger logic, could turn the SR MOSFET off in an inappropriate time.

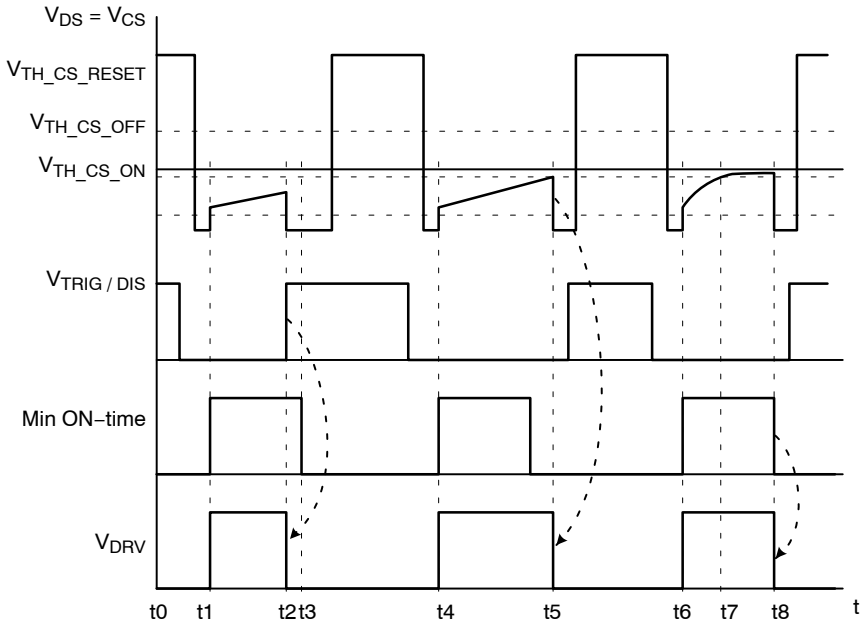


Figure 57. Trigger Input Functionality Waveforms – Trigger over Ride, CS Turn Off and Min On−time

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Figure 57 depicts all possible driver turn−off events in details when correct V_{CC} is applied. Controller driver is disabled based on TRIG / DIS input signal in time t2; the TRIG / DIS input overrides the minimum on−time period.

Driver is turned−off according to the CS (V_{DS}) signal (t5 marker) and when minimum on−time period elapsed already. TRIG / DIS signal needs to be low during this event.

If the CS (V_{DS}) voltage reaches $V_{TH_CS_OFF}$ threshold before minimum on−time period ends (t7) and the TRIG / DIS pin is low the DRV is turned−off on the falling edge of the minimum on−time period (t8 time marker in Figure 57). This demonstrates the fact that the Trigger over rides the minimum on−time. Minimum on−time has higher priority than the CS signal.

In Figure 58 the TRIG / DIS input is low the whole time and the DRV pulses are purely a function of the CS signal and the minimum on−time. The first DRV pulse terminated based on the CS signal and another two DRV pulses are prolonged till the minimum on−time period end despite the CS signal crosses the $V_{TH_CS_OFF}$ threshold earlier.

If a minimum on−time is too long the situation that occurs after time marker t6 Figure 58 can occur, is not correct and should be avoided. The minimum t_{ON} period should be selected shorter to overcome situation that the SR MOSFET is turned−on for too long time. The secondary current then changes direction and energy flows back to the transformer that result in reduced application efficiency and also in excessive ringing on the primary and secondary MOSFETs.

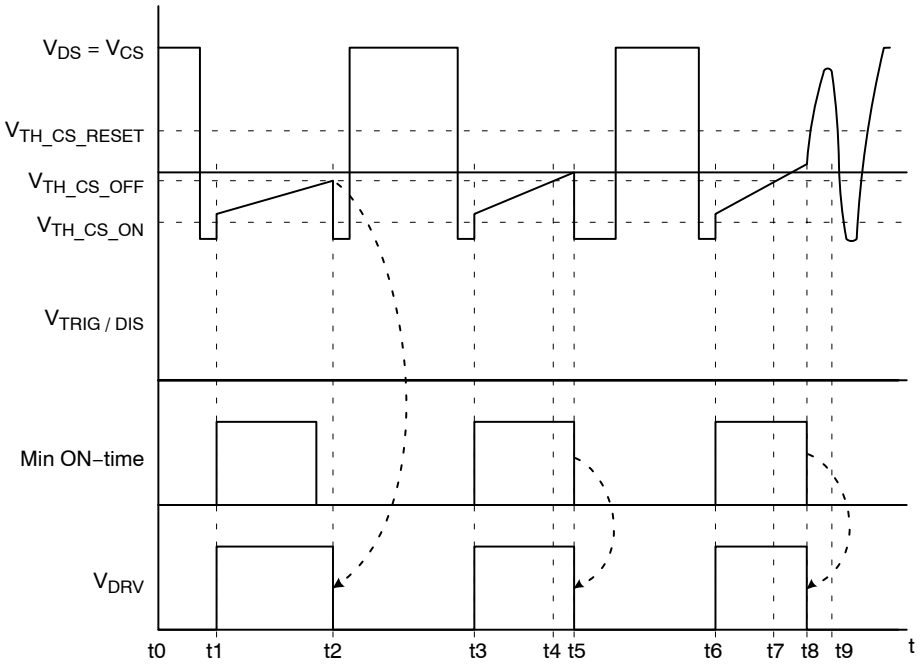


Figure 58. Minimum On−Time Priority

Figure 59 shows IC behavior in case the trigger signal features two pulses during one cycle of the V_{DS} (CS) signal. The TRIG / DIS goes low enables the DRV just before time t1 and DRV turns−on because the V_{DS} voltage drops under $V_{TH_CS_ON}$ threshold voltage. The TRIG / DIS signal disables driver at time t2. The TRIG / DIS drops down to LOW level in time t3, but IC waits for complete minimum off−time. Minimum off−time execution is blocked until CS pin voltage goes above $V_{TH_CS_RESET}$ threshold. Next cycle starts in time t6. The TRIG / DIS goes low and enables the DRV before V_{DS} drops below $V_{TH_CS_ON}$ threshold voltage thus the DRV turns−on in time t6. The TRIG / DIS signal rises up to HIGH level at time t7, consequently DRV turns−off and IC waits for high CS voltage to start minimum off−time execution.

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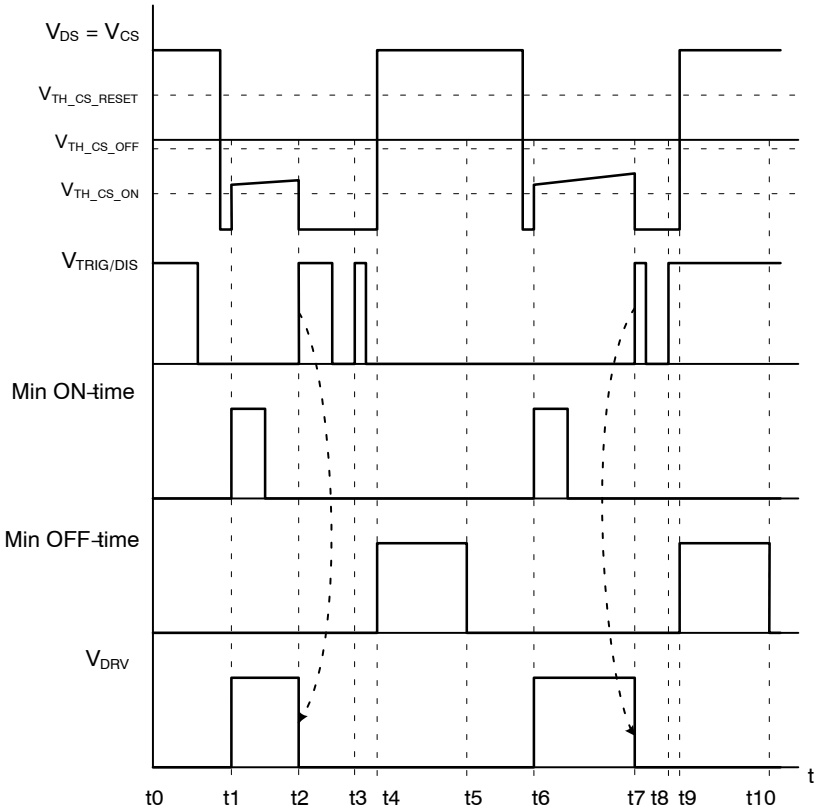


Figure 59. TRIG / DIS Input Functionality Waveforms – Two Pulses at One Cycle

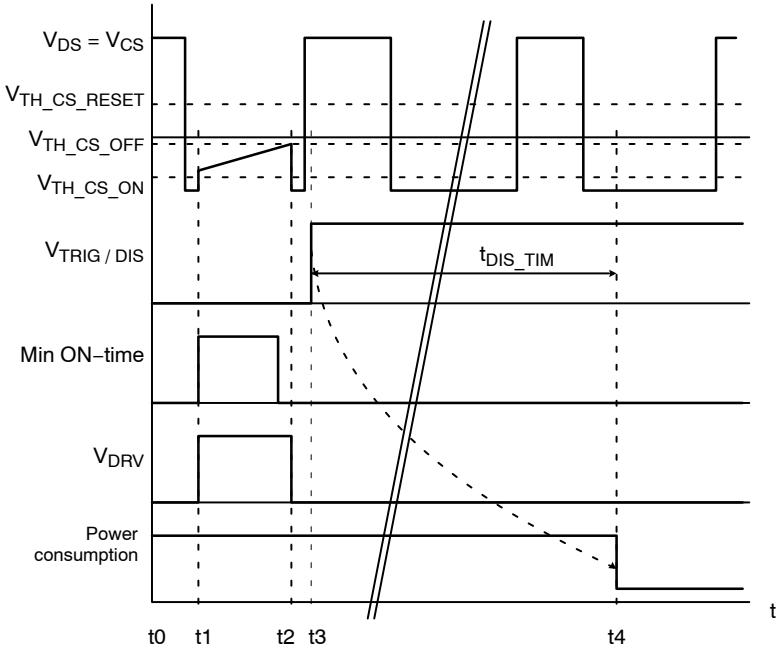


Figure 60. Trigger Input Functionality Waveforms – Disable Mode Activation

In Figure 60 above, at t2 the CS pin rises to $V_{TH_CS_OFF}$ and the SR MOSFET is turned−off. At t3 the TRIG / DIS signal is held high for more than t_{DIS_TIM}. NCP4306 enters disable mode after t_{DIS_TIM}. Driver output is disabled in disable mode. The DRV stays low (disabled) during transition to disable mode. Figure 61 shows disable mode transition 2nd case – i.e. when trigger rising edge comes during the trigger blank period. Figure 62 shows entering into disable mode and back to normal sequences.

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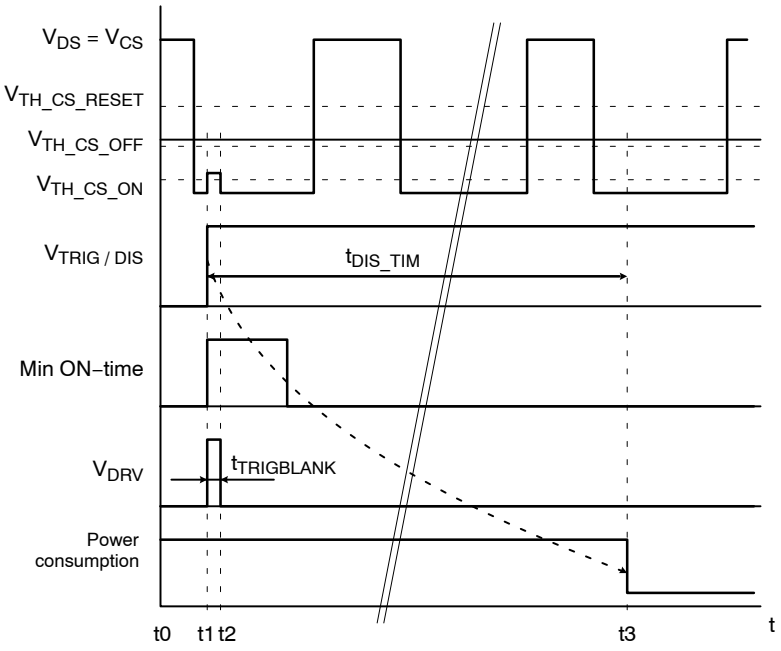


Figure 61. Trigger Input Functionality Waveforms – Disable Mode Clock Initiation

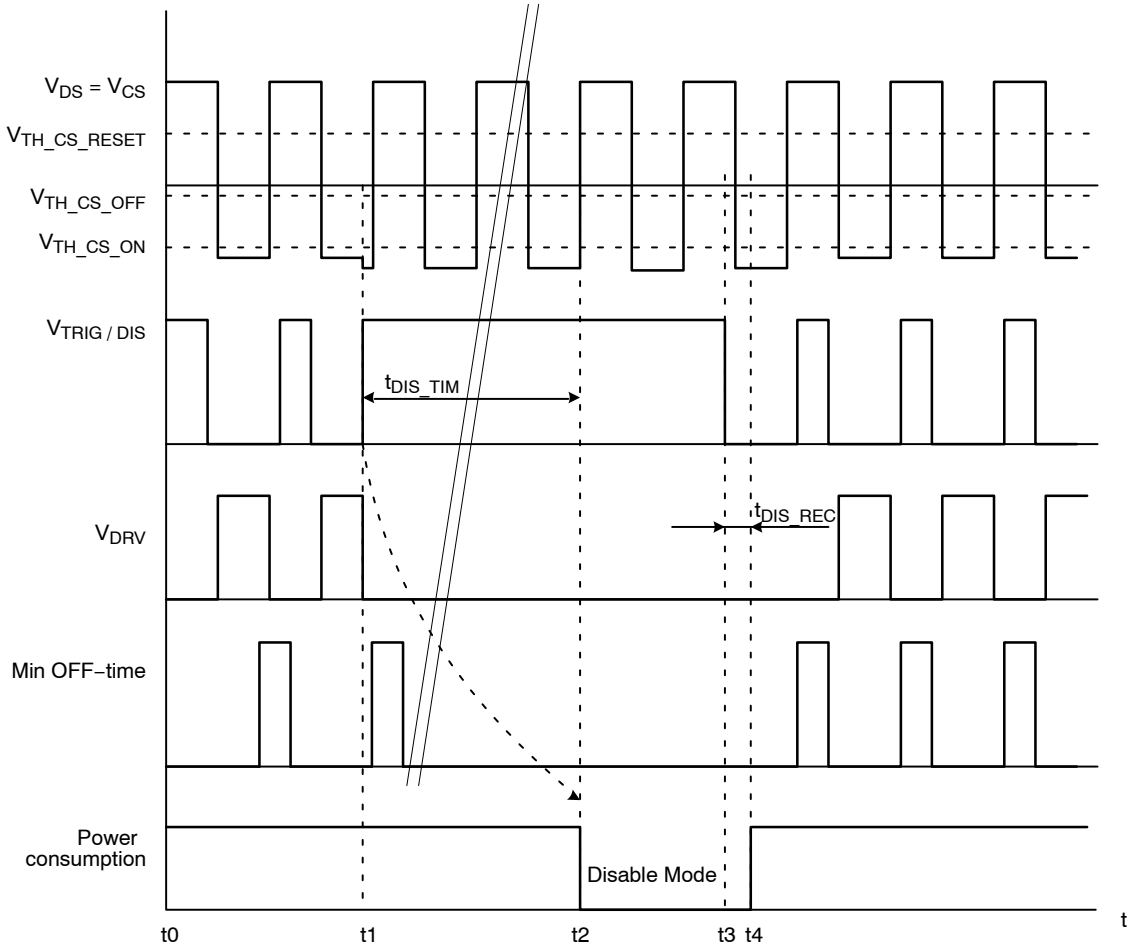


Figure 62. Trigger Input Functionality Waveforms – Disable and Normal Modes

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Figure 63 and Figure 64 shows exit from disable mode in detail. NCP4306 requires time up to t_{DIS_REC} to recover all internal circuitry to normal operation mode when recovering from disable mode. The driver is then enabled after complete t_{MIN_TOFF} period when CS (V_{DS}) voltage is over $V_{TH_CS_RESET}$ threshold. Driver turns−on in the next cycle on CS (V_{DS}) falling edge signal only (t5 − Figure 63). The DRV stays low during recovery time period. TRIG / DIS input has to be low at least for t_{DIS_END} time to end disable mode and start with recovery. Trigger can go back high after t_{DIS_END} without recovery interruption.

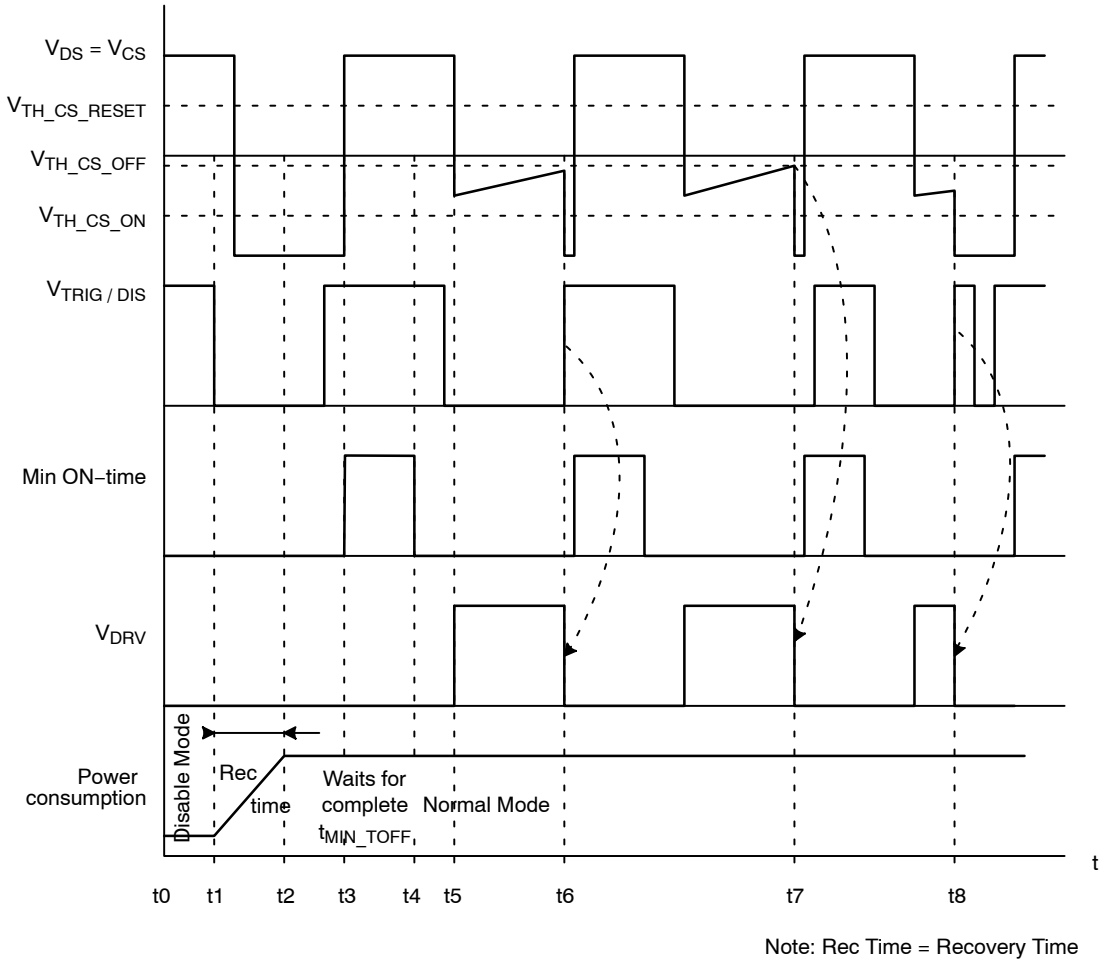


Figure 63. Trigger Input Functionality Waveforms – Exit from Disable Mode before the Falling Edge of the CS Signal

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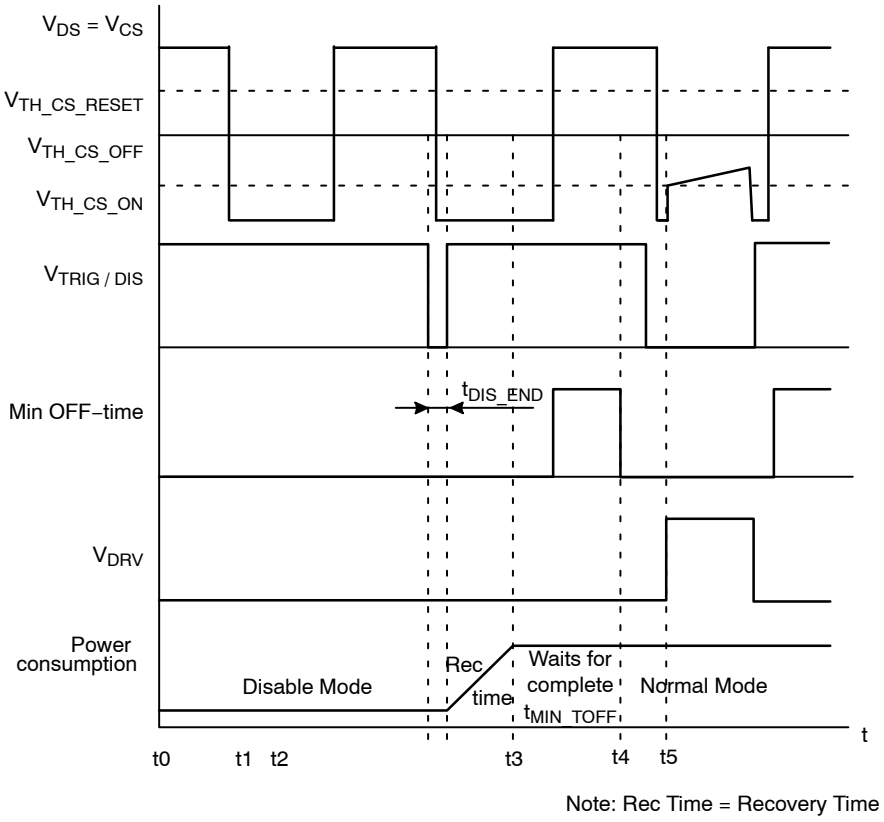


Figure 64. Trigger Input Functionality Waveforms

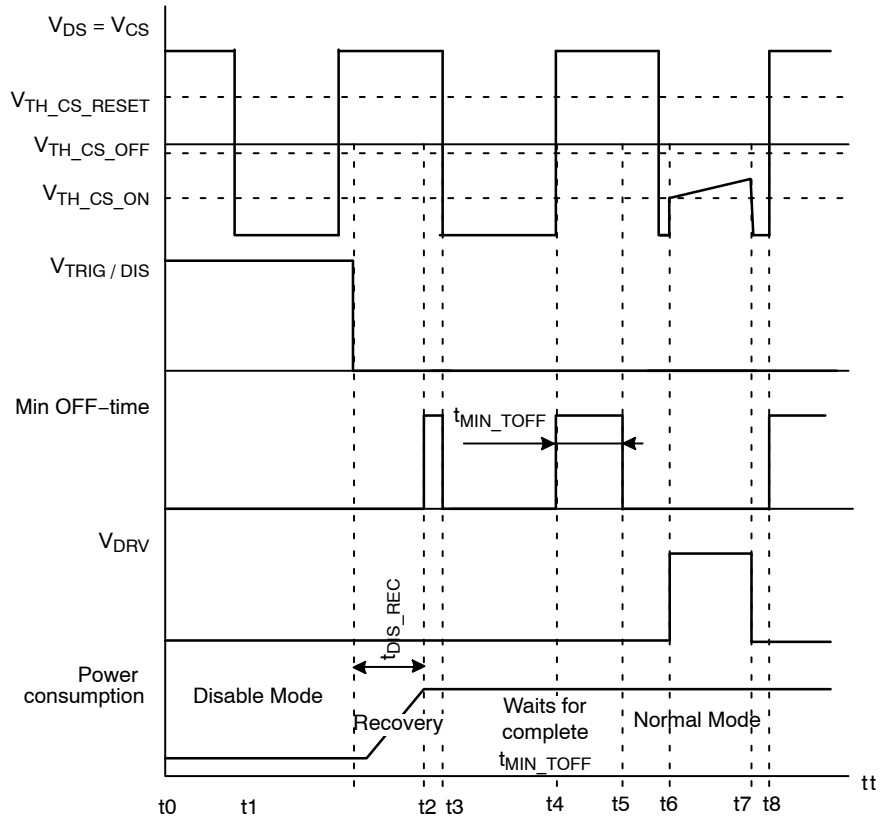


Figure 65. Trigger Input Functionality Waveforms

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Figure 65 shows detail IC behavior after disable mode is ended. The trigger pin voltage goes low at t1 and after t_{DIS_REC} IC leaves disable mode (t2). Time interval between t2 and t3 is too short for complete minimum off−time so normal mode doesn't start. V_{DS} voltage goes high again at time t4 and this event starts new minimum off−time timer execution. Next V_{DS} falling edge below $V_{TH_CS_ON}$ level activates driver.

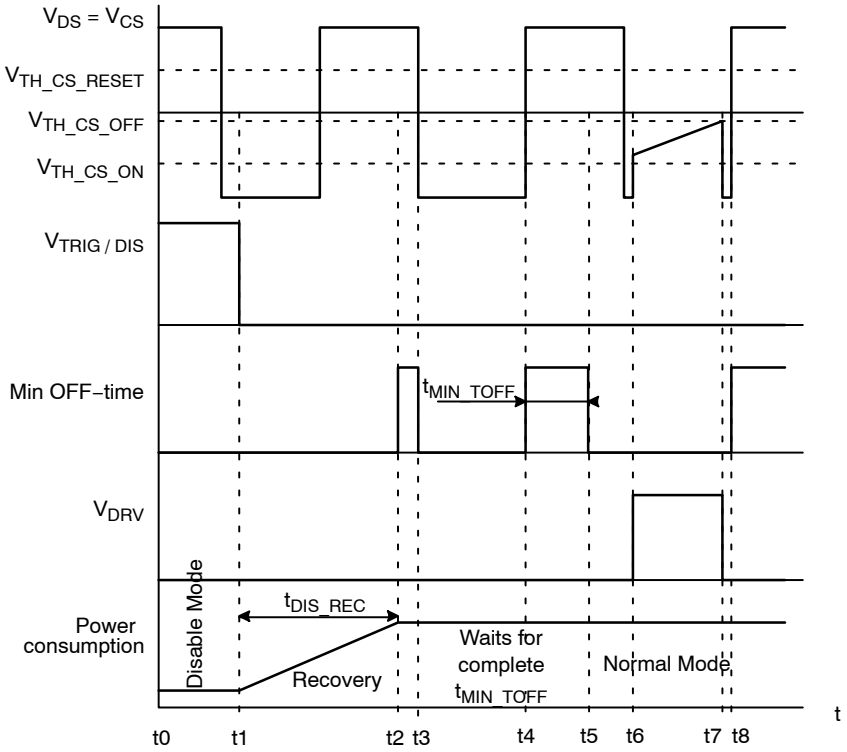


Figure 66. Trigger Input Functionality Waveforms

Different situation of leaving from disable mode is shown at Figure 66. Minimum off−time execution starts at time t2, but before time elapses V_{DS} voltage falls to negative voltage. This interrupts minimum off−time execution and the IC waits to another time when V_{DS} voltage is positive and then is again started the minimum off−time timer. The IC returns into normal mode after whole minimum off−time elapses.

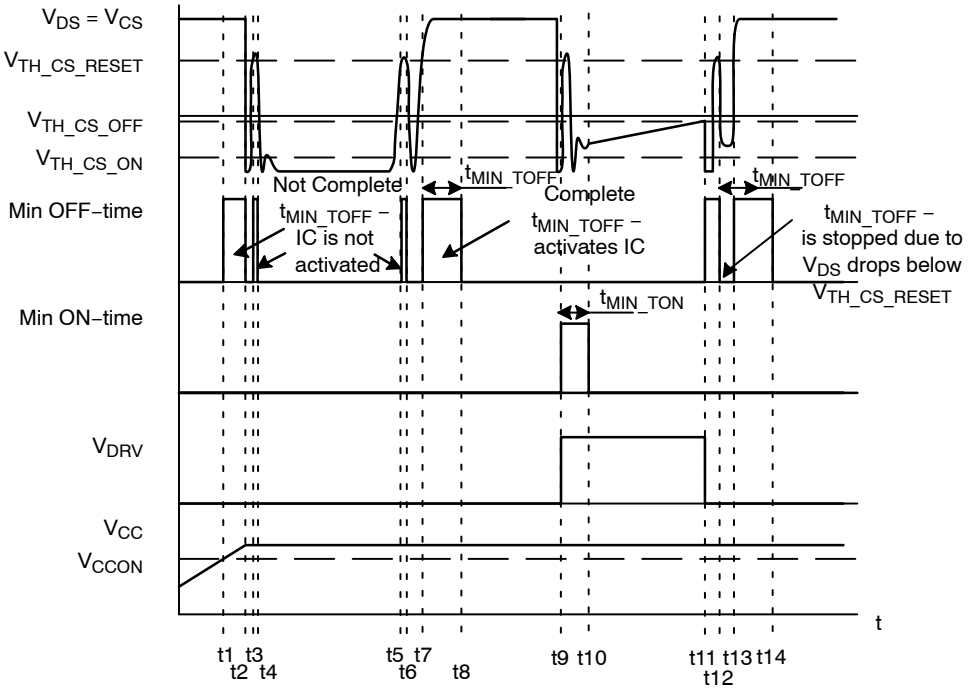


Figure 67. NCP4306 Operation after Start−Up Event

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Start−up event waveforms are shown at Figure 67. A start−up event is very similar to an exit from disable mode event. The IC waits for a complete minimum off−time event (CS pin voltage is higher than $V_{TH_CS_RESET}$) until drive pulses can continue. Figure 67 shows how the minimum off−time timer is reset when CS voltage is oscillating through $V_{TH_CS_RESET}$ level. The NCP4306 starts operation at time t1 (time t1 can be seen as a wake−up event from the disable mode through TRIG / DIS or LLD pin). Internal logic waits for one complete minimum off−time period to expire before the NCP4306 can activate the driver after a start−up or wake−up event. The minimum off−time timer starts to run at time t1, because V_{CS} is higher than $V_{TH_CS_RESET}$. The timer is then reset, before its set minimum off−time period expires, at time t2 thanks to CS voltage lower than $V_{TH_CS_RESET}$ threshold. The aforementioned reset situation can be seen again at time t3, t4, t5 and t6. A complete minimum off−time period elapses between times t7 and t8 allowing the IC to activate a driver output after time t8.

Optional primary triggering techniques for CCM flyback application are shown in Figure 68 and Figure 69. NCP4306 can operate properly without triggering in CCM, but use of triggering can reduce the commutation losses and the SR MOSFET drain voltage spike, which results in improved efficiency in CCM.

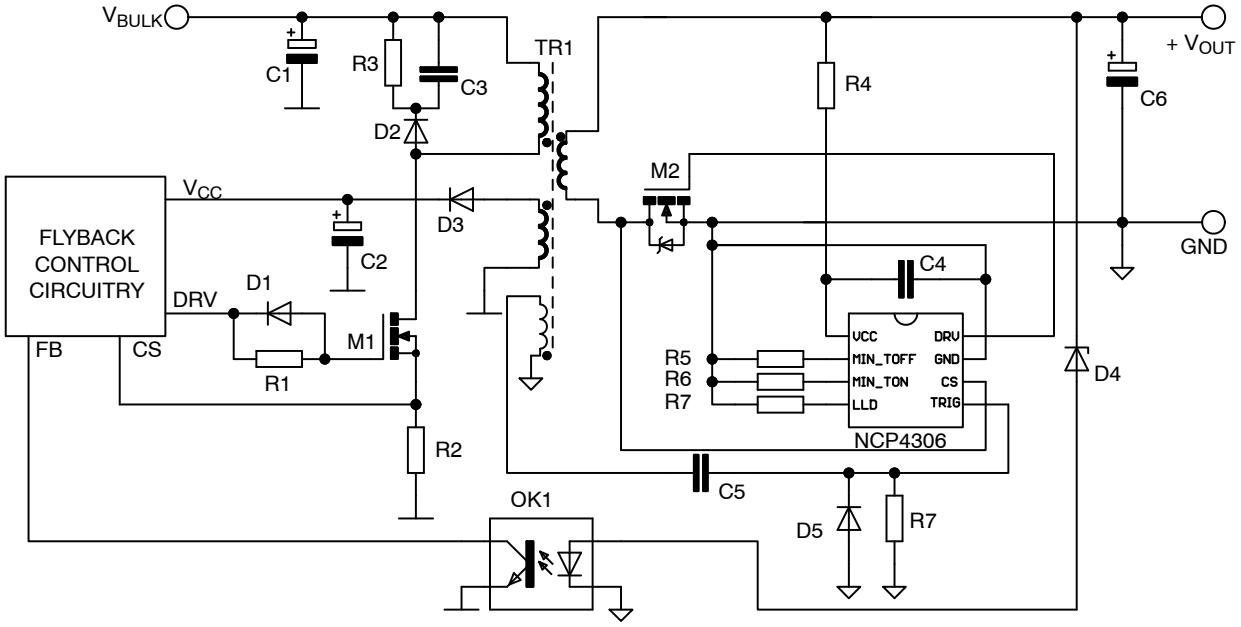


Figure 68. Optional Primary Triggering in Deep CCM Application Using Auxiliary Winding

The application shown in Figure 68 is simplest and the most cost effective solution for primary SR triggering. This method uses auxiliary winding made of triple insulated wire placed close to the primary winding section. This auxiliary winding provides information about primary turn−on event to the SR controller before the secondary winding reverses. This is possible thanks to the leakage between primary and secondary windings that creates natural delay in energy transfer. This technique provides approximately 0.5% efficiency improvement when the application is operated in deep CCM and a transformer that has a leakage of 1% of primary inductance is used.

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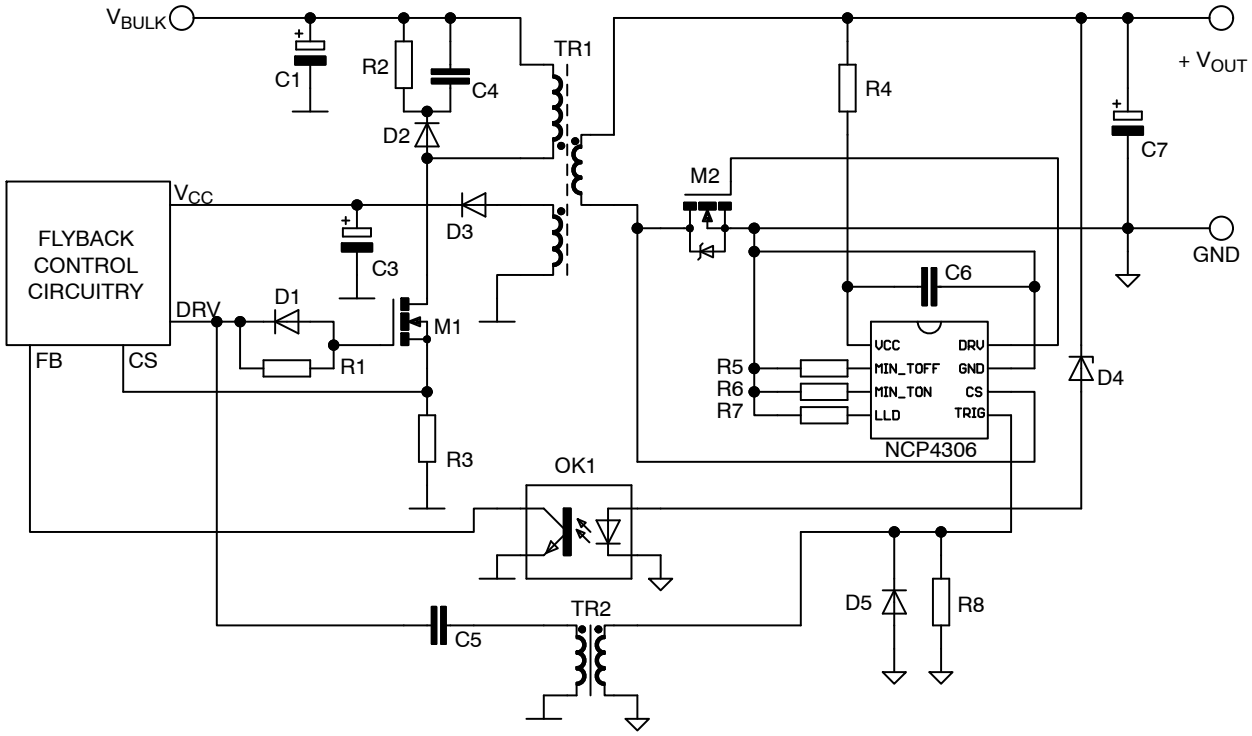


Figure 69. Optional Primary Triggering in Deep CCM Application Using Trigger Transformer

Application from Figure 69 uses an ultra−small trigger transformer to transfer primary turn−on information directly from the primary controller driver pin to the SR controller trigger input. Because the trigger input is rising edge sensitive, it is not necessary to transmit the entire primary driver pulse to the secondary. The coupling capacitor C5 is used to allow the trigger transformer's core to reset and also to prepare a needle pulse (a pulse with width shorter than 100 ns) to be transmitted to the NCP4306 TRIG / DIS input. The advantage of needle trigger pulse usage is that the required volt−second product of the pulse transformer is very low and that allows the designer to use very small and cheap magnetic. The trigger transformer can even be prepared on a small toroidal ferrite core with outer diameter of 4 mm and four turns for primary and secondary windings to assure $L_{PRIMARY} = L_{SECONDARY} > 10\ \mu H$. Proper safety insulation between primary and secondary sides can be easily assured by using triple insulated wire for one or, better, both windings.

This primary triggering technique provides approximately 0.5% efficiency improvement when the application is operated in deep CCM and transformer with leakage of 1% of primary inductance is used.

It is also possible to use capacitive coupling (use additional capacitor with safety insulation) between the primary and secondary to transmit the trigger signal. We do not recommend this technique as the parasitic capacitive currents between primary and secondary may affect the trigger signal and thus overall system functionality.

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Minimum t_{ON} and t_{OFF} adjustment

The NCP4306 offers fixed or an adjustable minimum on−time and off−time blanking periods (depends on IC version) that ease the implementation of a synchronous rectification system in any SMPS topology. These timers avoid false triggering on the CS input after the MOSFET is turned on or off.

Fixed versions are defined internally and can't be modified later or changed during operation.

The adjustment of minimum t_{ON} and t_{OFF} periods are done based on an internal timing capacitance and external resistors connected to the GND pin – refer to Figure 70 for a better understanding.

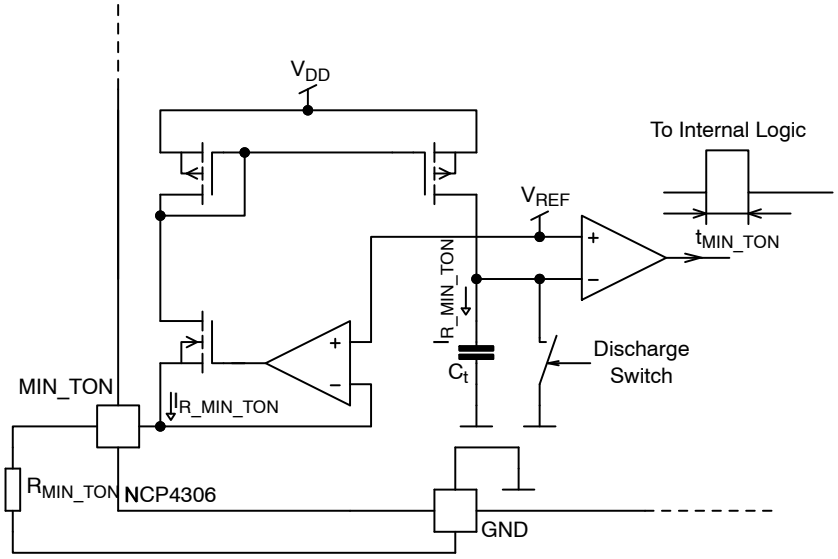


Figure 70. Internal Connection of the MIN_TON Generator (the MIN_TOFF Works in the Same Way)

Current through the MIN_TON adjust resistor can be calculated as:

$$I_{R_MIN_TON} = \frac{V_{ref}}{R_{MIN_TON}} \quad \text{(eq. 1)}$$

If the internal current mirror creates the same current through R_{MIN_TON} as used the internal timing capacitor (Ct) charging, then the minimum on−time duration can be calculated using this equation.

$$t_{MIN_ON} = V_t \times \frac{V_{ref}}{I_{R_MIN_TON}} = C_t \times \frac{V_{ref}}{\frac{V_{ref}}{R_{MIN_TON}}} = C_t \times R_{MIN_TON} \quad \text{(eq. 2)}$$

The internal capacitor size would be too large if $I_{R_MIN_TON}$ was used. The internal current mirror uses a proportional current, given by the internal current mirror ratio. Note that the internal timing comparator delay affects the accuracy of equations 7 and 8 when MIN_TON or MIN_TOFF times are selected near to their minimum possible values. Please refer to Figure 71 and Figure 72 for measured minimum on and off time charts.

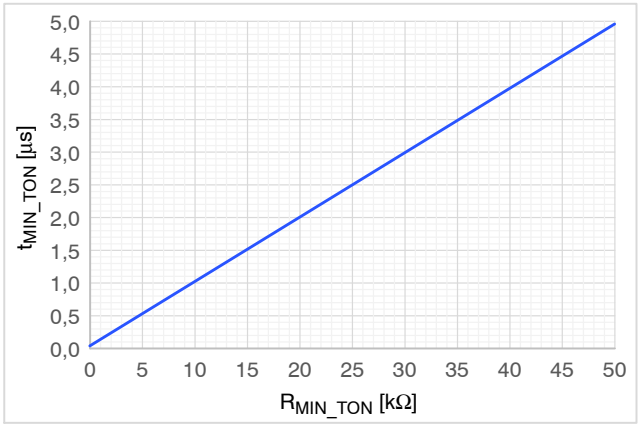


Figure 71. MIN_TON Adjust Characteristic

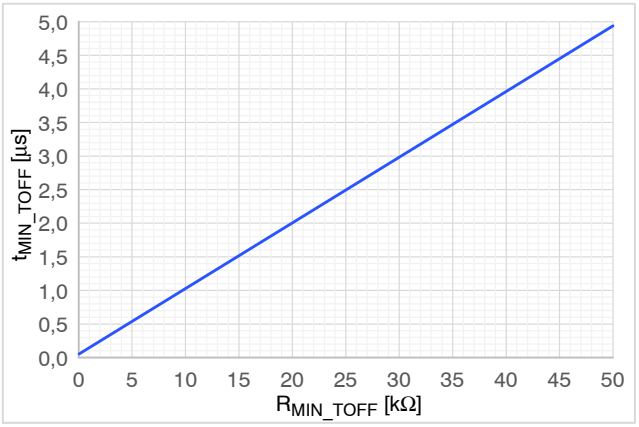


Figure 72. MIN_TOFF Adjust Characteristic

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The absolute minimum t_{ON} duration is internally clamped to 55 ns and minimum t_{OFF} duration to 70 ns in order to prevent any potential issues with the minimum t_{ON} and / or t_{OFF} input being shorted to GND.

The NCP4306 features dedicated anti−ringing protection system that is implemented with a minimum t_{OFF} blank generator. The minimum off−time one−shoot generator is restarted in the case when the CS pin voltage crosses $V_{TH_CS_RESET}$ threshold and MIN_TOFF period is active. The total off−time blanking period is prolonged due to the ringing in the application (refer to Figure 47).

Some applications may require adaptive minimum on and off time blanking periods. It is possible to modulate blanking periods by using an external NPN transistor – refer to Figure 73. The modulation signal can be derived based on the load current, feedback regulator voltage or other application parameter.

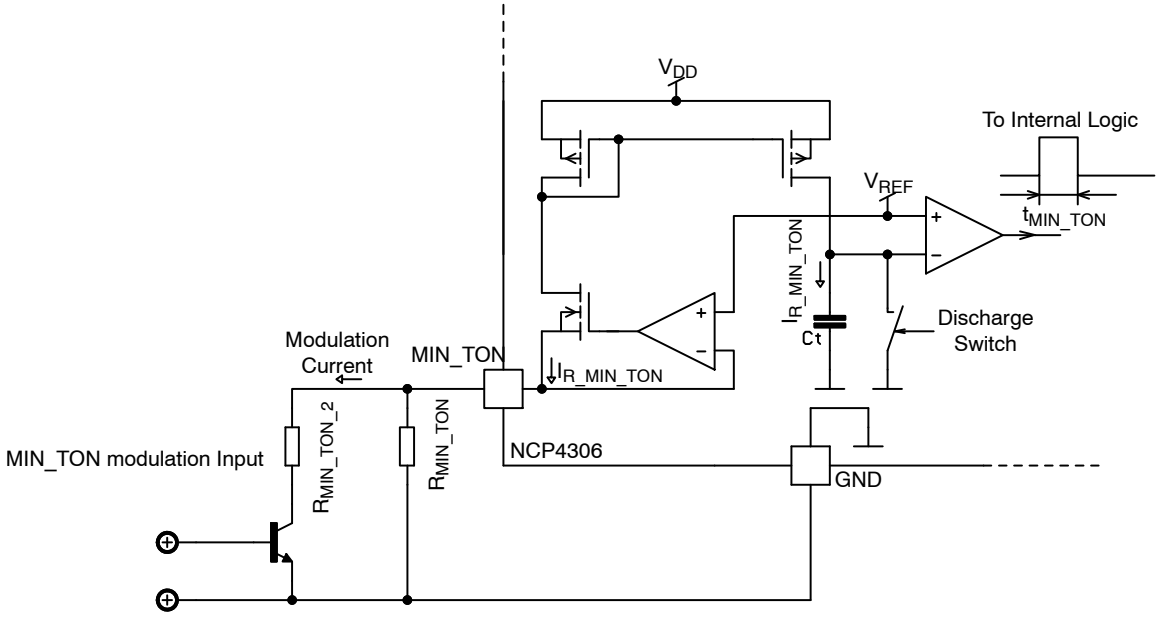


Figure 73. Possible Connection for MIN_TON and MIN_TOFF Modulation

dV / dt Detection – Flyback feature

The NCP4306 includes optional feature for flyback type converters, which operates with shorter primary on−time than ringing period after demagnetization phase during medium / high loads. These applications are for example USB−PD or Quick Charge adapters. Difficulty with this situation is that minimum off−time doesn't elapse before primary side switch is turned on and off again so SR controller doesn't turn on SR mosfet. Whole secondary side current flows through body diode that makes power loss. Figure 74 shows situation without dV / dt detection. Here can be seen that without detection next conduction cycle may be not taken through activated SR transistor. Reason is not elapsed minimum off−time blanking interval.

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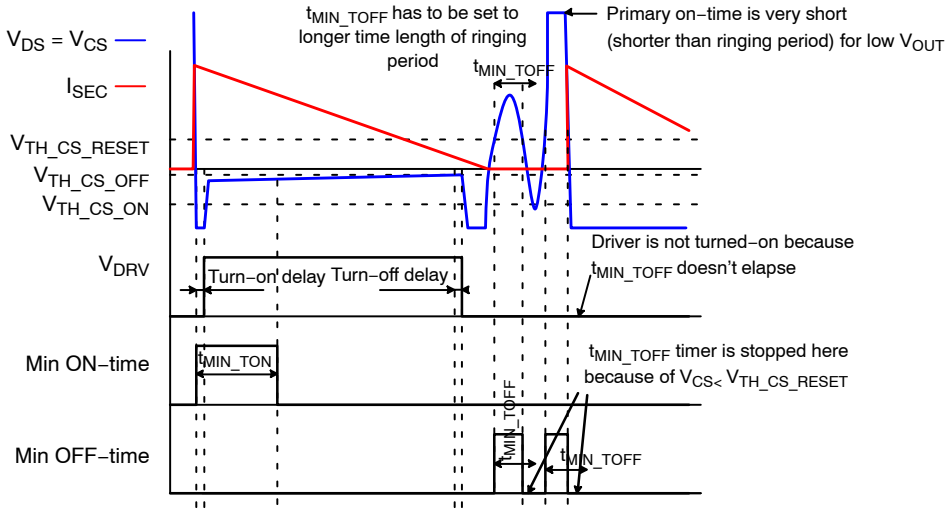


Figure 74. Situation without dV / dt Detection Feature

Figure 75 shows how system with activated dV / dt detection behaves. Min_toff blanking interval is also reset during voltage drops at CS pin, but if high negative dV / dt occurs at CS pin, min_toff interval is shorted and SR controller is ready to detect CS voltage lower than $V_{CS_TH_ON}$ and turn SR transistor on. Negative dV / dt at CS pin after primary switch is turned off is high in compare to slope that comes during ringing after demagnetization. Thanks to this we can safely detect end of primary on−time from ringing.

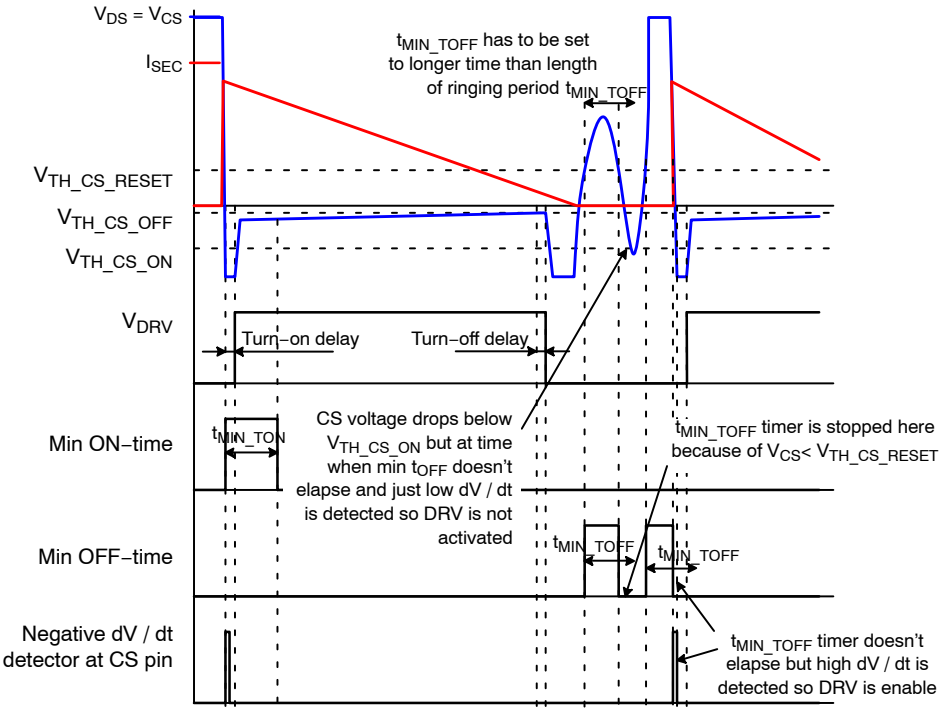


Figure 75. Situation with Enabled dV / dt Detection

Exception Timer – LLC feature

Exception timer is special feature for LLC type SMPS. It is mainly targeted to operation under light / medium load, where secondary side SMPS current shape is not sine, but it contains part of capacitive peak optionally with no current part followed by distorted sine. Examples of current shape is shown in Figure 76. This figure shows different current shapes at different loading. Lower loading makes shape more distorted from ideal sine.

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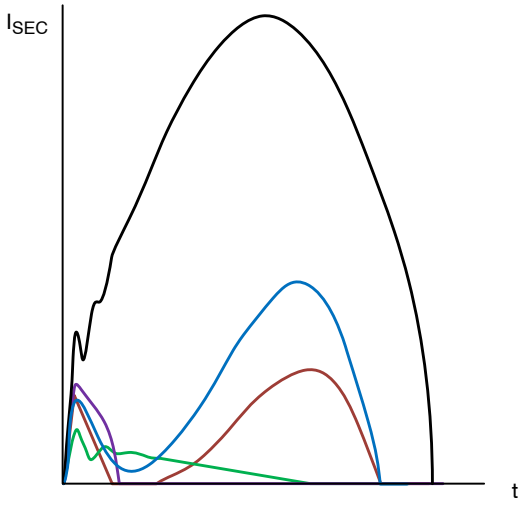


Figure 76. Current Shapes in LLC Examples

Problematic shapes may cause prematurely SR transistor turn−off, because CS voltage may get to zero or to positive voltage (due to low current or high dI / dt and parasitic inductance). Sensed voltage drop can be seen in Figure 77. This situation is valid for SR mosfet with R_{DSON} = 1 mΩ and with package (SMT) parasitic inductance L_{PACPAR} = 0.5 nH. There can be seen that SR transistor should be turned off in time between 0.4 to 1.5 μs, because CS voltage is above $V_{TH_CS_OFF}$ threshold. Turn−off process can be masked by min_ton blanking interval, but in this case is needed to set it at least to 1.5 μs that can make issue during very light load where current flows just short time and long min_ton may cause reverse current from output capacitors back to transformer and may change soft switching condition to hard switching at primary side.

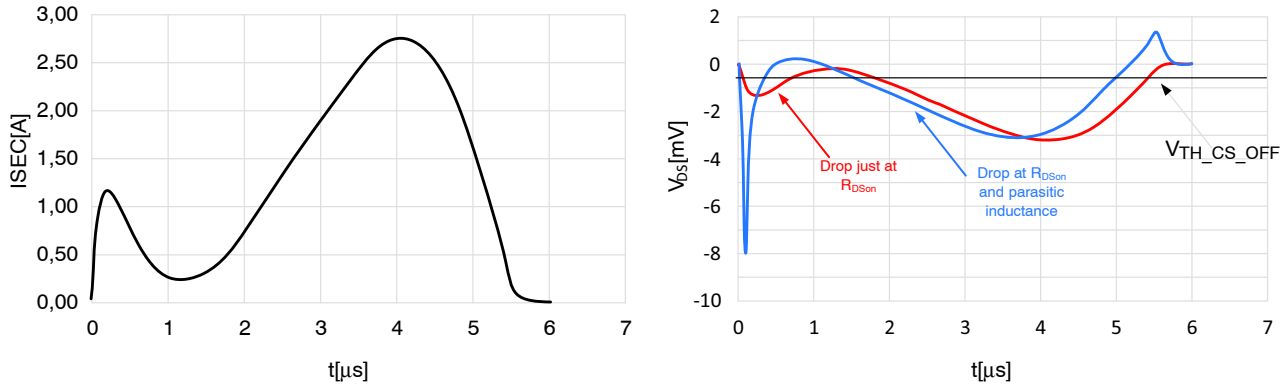


Figure 77. Sensed Voltage Drop at SR Transistor in LLC during Light / Medium Load

To early SR transistor turn−off is not issue just from efficiency point of view, but also from system stability point of view. When load is decreased, feedback loop asks primary side for lower power that changes secondary side current shape and SR driver can be turned off shortly after min_toff elapses. This causes lower efficiency transfer to secondary side and output voltage starts to decrease. Feedback loop asks for more power, secondary current shape changes and SR driver starts to conduct whole period again that improves energy transfer efficiency and output voltage starts to increase. This has to be again regulated by feedback loop and everything starts from begin and make SMPS oscillations that can be accompany with audible noise.

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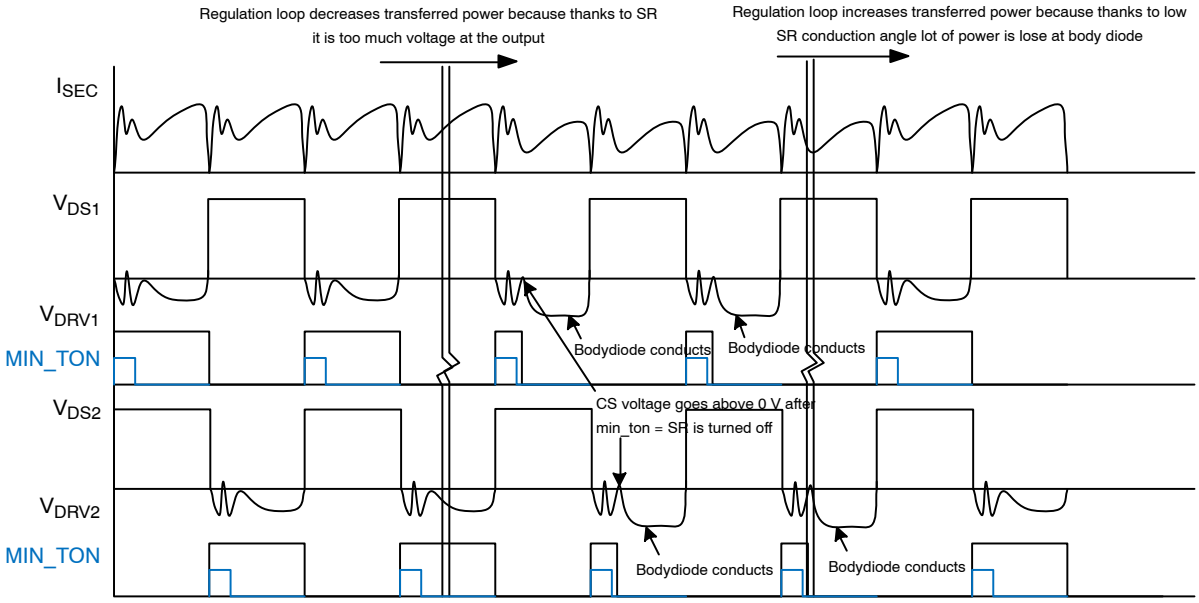


Figure 78. LLC System Oscillation due to Short SR Transistor Conduction

Operation of new feature is shown in Figure 79. Current shape makes drop at SR transistor with 1 mΩ and 0.5 nH shown as V_{DS} that is sensed at CS pin and on and off comparators decide about SR operation based on this voltage. Driver is turned on and exception timer is started when V_{CS} drops below $V_{CS_TH_ON}$. During minimum on−time blanking interval off comparator is not active. CS pin voltage is above $V_{TH_CS_OFF}$ after minimum on−time elapses so driver is turned−off and because exception timer doesn't elapse, min_ton blanking interval is started. During this time on comparator output is blanked. Reason is to avoid quick driver turning on and off that would just increase consumption. When min_ton blanking interval elapses CS voltage is again below $V_{TH_CS_ON}$ and exception timer is not elapsed, driver can be turned on again simultaneously with minimum on−time interval. Driver is turned off again almost at the end of conduction phase, but this is correct turn off. Min−ton blanking interval doesn't start, because exception timer elapsed before so SR controller waits for $V_{CS} > V_{CS_TH_RESET}$ to start minimum off time blanking timer.

Exception timer length is given as multiple of minimum on time interval. It should be not set to longer time than

$$t_{EXC} < \frac{1}{3 \times f_{SWMAX}} \quad \text{(eq. 3)}$$

where f_{SWMAX} is maximum LLC switching frequency.

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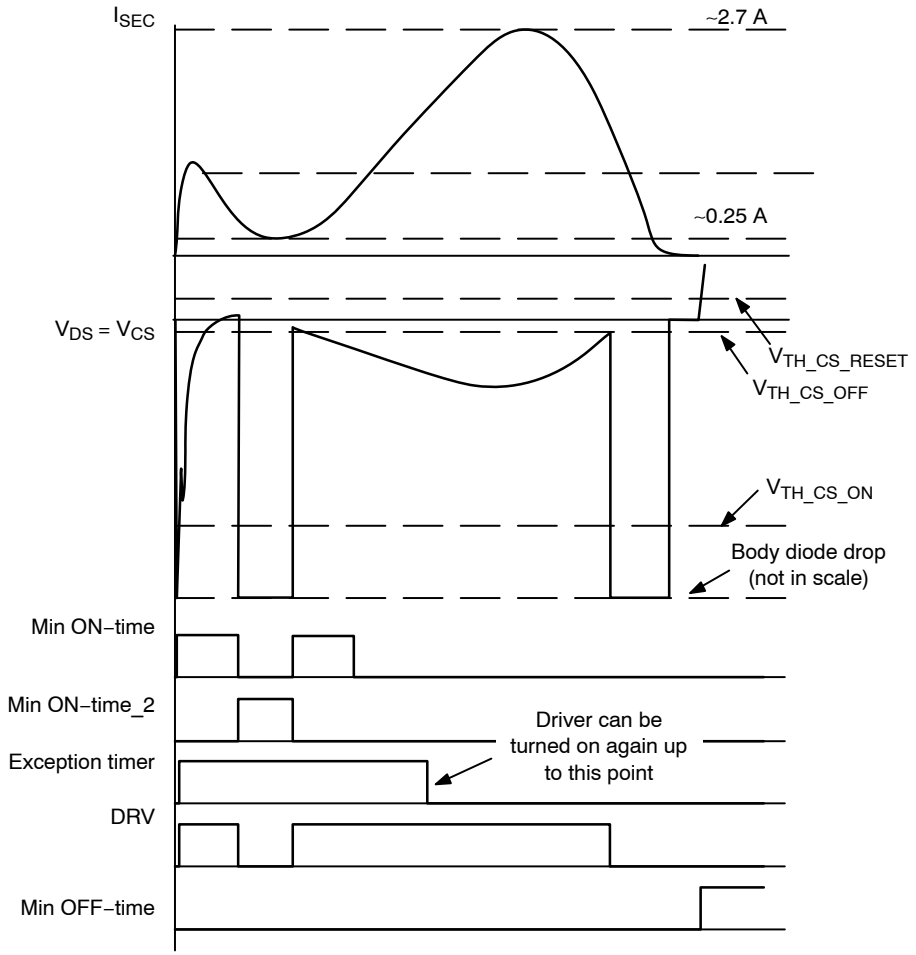


Figure 79. Exception Timer Operation

Light Load Detection

Light load detection feature is feature which task is to decrease SR controller consumption during time when SR transistor switching is not needed. This is usually during no load and light load condition when static SR controller consumption starts to play role. Goal is to disable controller during no switching time to eliminate static consumption and turn−on SR transistor as soon as possible when switching comes.

Internal simplified block diagram is shown in Figure 80. Main parts of this system are comparator at CS input that informs about CS voltage lower than zero (body diode or SR transistor conducting), LLD timer with set able nominal time and possibility to reduce it to one half and finally D flip flop with Disable signal output. Nominal time can be set by resistor at LLD pin connected to ground or internally during production. Recommended resistor values are shown in Table 6. In case of very noisy system, capacitor in parallel to LLD resistor may be used. Capacitor value impacts start−up time, because capacitor has to be charged above disable threshold by internal LLD current source.

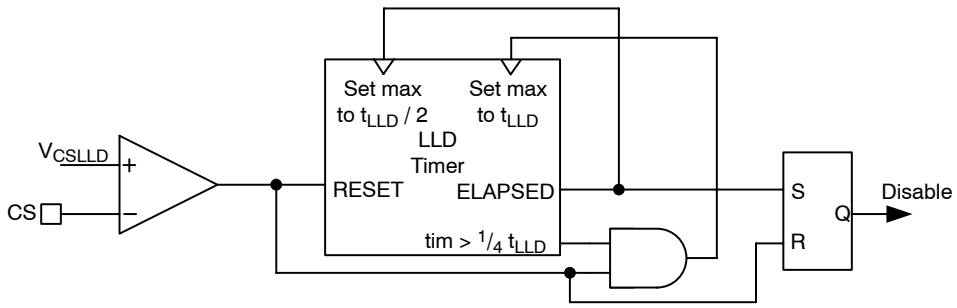


Figure 80. LLD Internal Block Diagram

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Table 6. PIN FUNCTION DESCRIPTION

LLD setting t_{LLD} [μs]	IC disabled	70	130	280	540	1075	LLD disabled
R_{LLD} [kΩ]	<12	27	43	68	91	120	>470*

*floating pin allowed, small cap for noise robustness improvement recommended

Logic function is also described by bubble diagram in Figure 81. LLD timer is running every time when CS pin voltage is positive (body diode and or transistor not conducting). If conduction doesn't come sooner than LLD timer elapses, DISABLE flag is set (IC is sent into low consumption mode), LLD timer length is changed to t_{LLD} / 2 (this adds some hysteresis in system and helps keeping overall system stable) and timer is also reset. SR controller waits for falling edge at CS pin (begin of new conduction cycle). When CS goes negative, disable mode is deactivated and IC starts to wake up (takes $t_{LLD_DIS_REC}$, system wake up is controlled same as exit from disable mode by TRIG / DIS pin). End of conduction phase (CS voltage goes positive) starts LLD timer. If next conduction phase comes shortly after first (pulses in skip burst) so shortly than t_{LLD} / 4 just LLD timer is reset. LLD timer length is set back to t_{LLD} only when new conduction phase comes after previous in time between t_{LLD} / 4 to t_{LLD} / 2. This situation happens when load is slowly increased and skip bursts come more often.

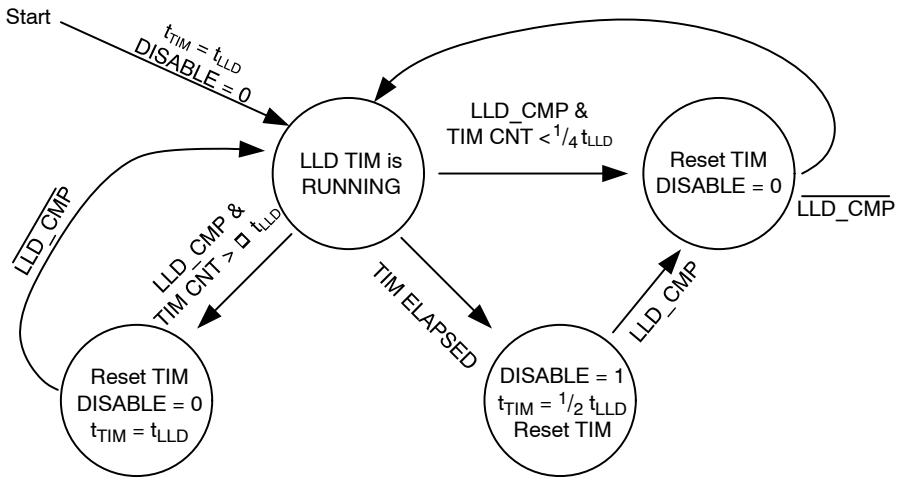


Figure 81. LLD Operation Bubble Diagram

Example of LLD operation with flyback convertor can be seen in Figure 82. SMPS works under heavy load from point 0 to 1 where switching pulses comes regularly at high frequency that resets LLD timer soon after begin of counting. Load is significantly decreased to light load at point 1 so primary controller turns to skip mode. LLD timer elapses during skip so controller enters disable mode with very low consumption and change LLD timer maximum to t_{LLD} / 2. Switching pulse in skip comes at time 3, this resets LLD timer and starts IC wake−up. Controller is waked up fully before point 4 and turns−on SR transistor. There is again no switching from 4 to 6 and thanks to it, LLD timer elapses at point 5 and controller enters disable mode again. Disable mode is ended at time 6, because new cycle comes. SR controller wakes−up and next pulse in skip burst is conducted via SR transistor. Time between 7 and 8 is delay between skip burst. Time is still less than t_{LLD} / 4, LLD timer interval is not changed. Pulse at time 8 is fully conducted via SR transistor, because controller was not in disable mode before pulse came. No switching period between 9 and 11 is longer than t_{LLD} / 2 that changes LLD timer setting to t_{LLD}. This is because shorter delay between skip burst means higher load. Pulses are transferred via SR transistor at time 11 and 12, because disable mode was not activated. Load is being decreased again between time 12 to 15 so at time 15 SR controller enters disable mode and LLD timer time is reduced again to t_{LLD} / 2. Second pulse in skip burst is again transferred via turned on SR transistor. Disable mode is activated after t_{LLD} / 2 at time 18. Load is sharply changed at time 19 that means LLD timer is reset each pulse and timers time is kept at t_{LLD} / 2. Load is removed at time 20 and disable is activated at time 21. Suitable LLD timer setting for flyback type of SMPS is 540 or 1075 μs (for special type 280 μs).

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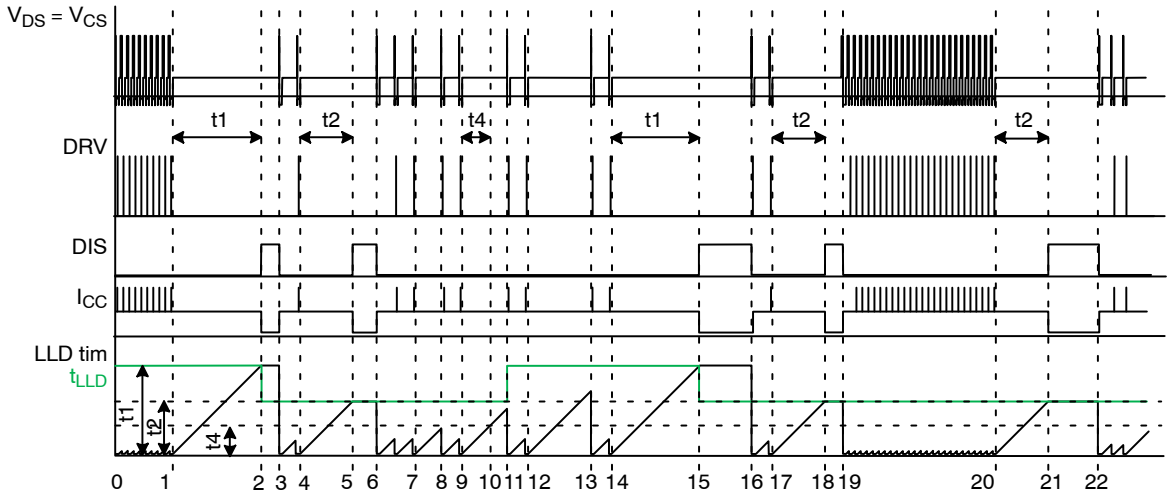


Figure 82. LLD Operation with Flyback SMPS

Example of LLD operation with LLC convertor can be seen in Figure 83. SMPS works under heavy load from point 0 to 3. Both LLD timers are reset each cycle before LLD timer reaches t_{LLD} / 4 and disable mode is not activated. SMPS load decreases at point 3 and goes into skip. LLD timers elapse during no switching time and change LLD timer time to t_{LLD} / 2. When skip burst comes at time 6 channel 2 starts to wake up, channel 1 starts to wake up at time 7. Both channels are ready to conduct via SR transistor at time 8 respectively 9. Skip burst ends at time 12, LLD timers elapse at time 13 and 14 (reached t_{LLD} / 2) and SR controllers enter disable mode. Controllers wake up at time 15 and 16 same as was in time 6 and 7. SMPS goes into skip in time 21, but load is connected soon and SMPS starts to operate under higher load from time 22. LLD timers reach time higher than t_{LLD} / 4 but lower than t_{LLD} / 2 so LLD timers maximum is set to t_{LLD}. LLD timer setting for LLC may be set to lower times.

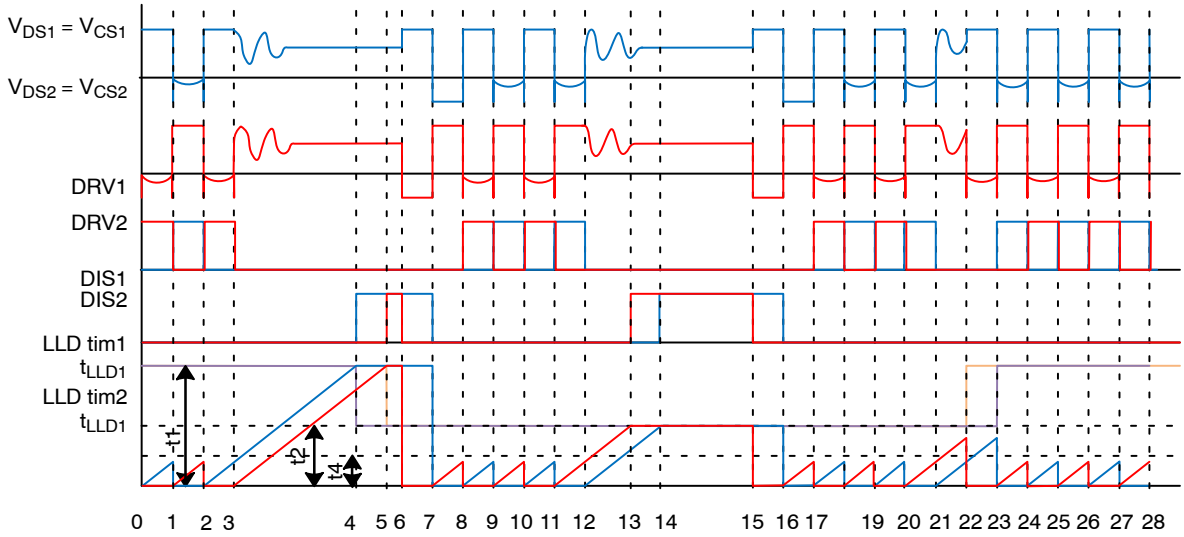


Figure 83. LLD Operation with LLC SMPS

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Operation flow

Followed bubble diagram at Figure 84 shows overall operation flow. Black bubbles are fundamental parts of system. States for dV / dt feature are colored by blue color and states for LLC feature (exception timer) are in red. LLC and dV / dt features are never activated both at same time. Operation starts in bubble start where system comes when VCC is higher than UVLO level and / or disable mode is activated (by LLD or TRIG / DIS pin).

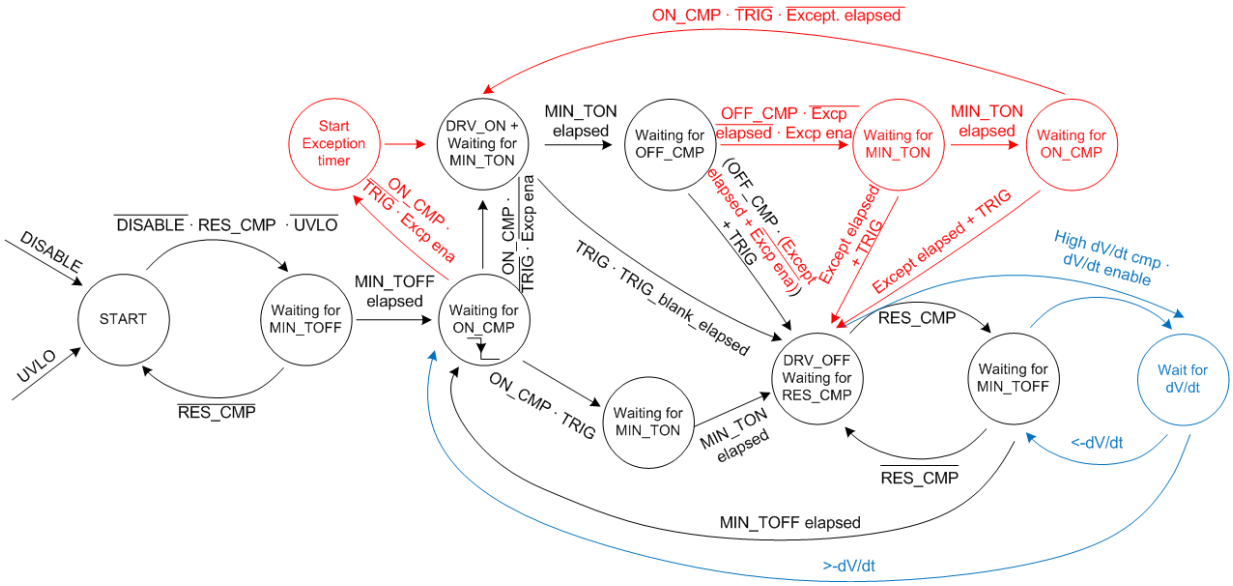


Figure 84. Overall Operation Bubble Diagram

Power dissipation calculation

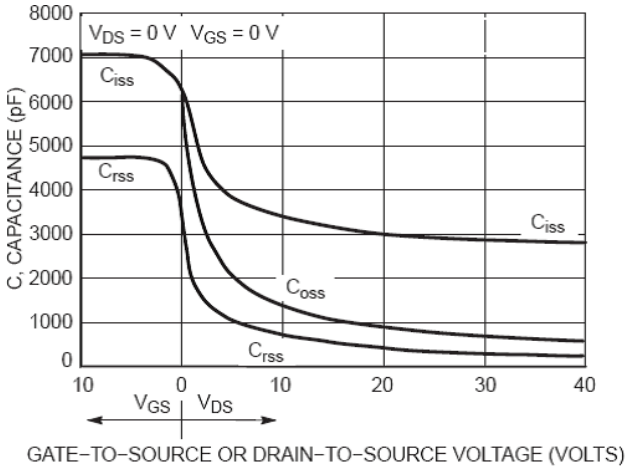
It is important to consider the power dissipation in the MOSFET driver of a SR system. If no external gate resistor is used and the internal gate resistance of the MOSFET is very low, nearly all energy losses related to gate charge are dissipated in the driver. Thus it is necessary to check the SR driver power losses in the target application to avoid over temperature and to optimize efficiency.

In SR systems the body diode of the SR MOSFET starts conducting before SR MOSFET is turned−on, because there is some delay from $V_{TH_CS_ON}$ detect to turn−on the driver. On the other hand, the SR MOSFET turn off process always starts before the drain to source voltage rises up significantly. Therefore, the MOSFET switch always operates under Zero Voltage Switching (ZVS) conditions when in a synchronous rectification system.

The following steps show how to approximately calculate the power dissipation and DIE temperature of the NCP4306 controller. Note that real results can vary due to the effects of the PCB layout on the thermal resistance.

Step 1 – MOSFET gate to source capacitance:

During ZVS operation the gate to drain capacitance does not have a Miller effect like in hard switching systems because the drain to source voltage does not change (or its change is negligible).



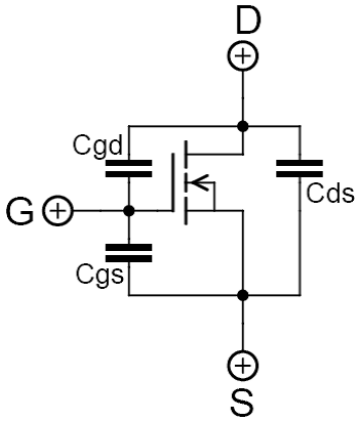


Figure 85. Typical MOSFET Capacitances Dependency on VDS and VGS Voltages

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$$C_{iss} = C_{gs} + C_{gd} \quad \text{(eq. 4)}$$

$$C_{rss} = C_{gd} \quad \text{(eq. 5)}$$

$$C_{oss} = C_{ds} + C_{gd} \quad \text{(eq. 6)}$$

Therefore, the input capacitance of a MOSFET operating in ZVS mode is given by the parallel combination of the gate to source and gate to drain capacitances (i.e. C_{iss} capacitance for given gate to source voltage). The total gate charge, Q_{g_total}, of most MOSFETs on the market is defined for hard switching conditions. In order to accurately calculate the driving losses in a SR system, it is necessary to determine the gate charge of the MOSFET for operation specifically in a ZVS system. Some manufacturers define this parameter as Q_{g_ZVS}. Unfortunately, most datasheets do not provide this data. If the C_{iss} (or Q_{g_ZVS}) parameter is not available then it will need to be measured. Please note that the input capacitance is not linear (as shown Figure 85) and it needs to be characterized for a given gate voltage clamp level.

Step 2 – Gate drive losses calculation:

Gate drive losses are affected by the gate driver clamp voltage. Gate driver clamp voltage selection depends on the type of MOSFET used (threshold voltage versus channel resistance). The total power losses (driving loses and conduction losses) should be considered when selecting the gate driver clamp voltage. Most of today's MOSFETs for SR systems feature low R_{DS_ON} for 5 V V_{GS} voltage. The NCP4306 offers both a 5 V gate clamp and a 10 V gate clamp for those MOSFET that require higher gate to source voltage.

The total driving loss can be calculated using the selected gate driver clamp voltage and the input capacitance of the MOSFET:

$$P_{DRV_total} = V_{CC} \times V_{CLAMP} \times C_{g_ZVS} \times f_{SW} \quad \text{(eq. 7)}$$

Where:

V_{CC} is the NCP4306 supply voltage

V_{CLAMP} is the driver clamp voltage

C_{g_ZVS} is the gate to source capacitance of the MOSFET in ZVS mode

f_{sw} is the switching frequency of the target application

The total driving power loss won't only be dissipated in the IC, but also in external resistances like the external gate resistor (if used) and the MOSFET internal gate resistance (Figure 86). Because NCP4306 features a clamped driver, it's high side portion can be modeled as a regular driver switch with equivalent resistance and a series voltage source. The low side driver switch resistance does not drop immediately at turn−off, thus it is necessary to use an equivalent value ($R_{DRV_SIN_EQK}$) for calculations. This method simplifies power losses calculations and still provides acceptable accuracy. Internal driver power dissipation can then be calculated using equation 8:

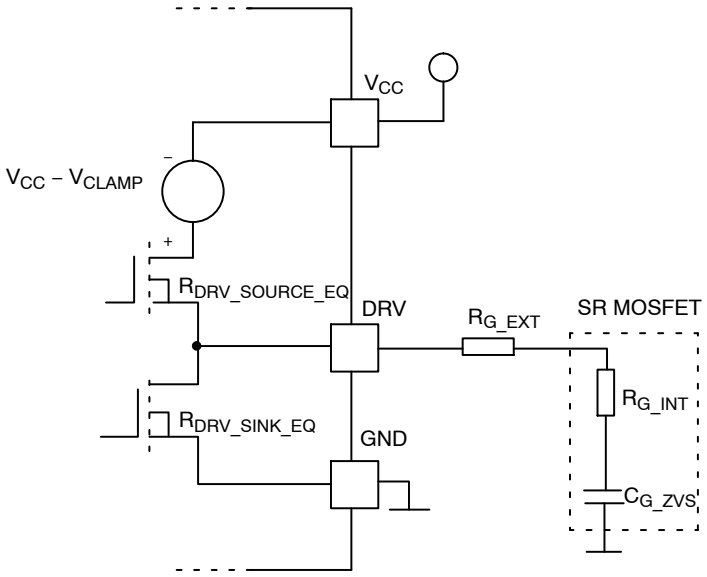


Figure 86. Equivalent Schematic of Gate Drive Circuitry

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$$P_{DRV_IC} = \frac{1}{2} \times C_{g_ZVS} \times V_{CLAMP}^{2} \times f_{SW} \times \left(\frac{R_{DRV_SINK_EQ}}{R_{DRV_SINK_EQ} + R_{G_EXT} + R_{g_int}} \right) + C_{g_ZVS} \times V_{CLAMP} \times f_{SW} \times (V_{CC} + V_{CLAMP})$$
$$+ \frac{1}{2} \times C_{g_ZVS} \times V_{CLAMP}^{2} \times f_{SW} \times \left(\frac{R_{DRV_SOURCE_EQ}}{R_{DRV_SOURCE_EQ} + R_{G_EXT} + R_{g_int}} \right) \quad \text{(eq. 8)}$$

Where:

$R_{DRV_SINK_EQ}$ is the NCP4306 driver low side switch equivalent resistance (1.6 Ω)

$R_{DRV_SOURCE_EQ}$ is the NCP4306 driver high side switch equivalent resistance (7 Ω)

R_{G_EXT} is the external gate resistor (if used)

R_{g_int} is the internal gate resistance of the MOSFET

Step 3 – IC consumption calculation:

In this step, power dissipation related to the internal IC consumption is calculated. This power loss is given by the I_{CC} current and the IC supply voltage. The I_{CC} current depends on switching frequency and also on the selected min t_{ON} and t_{OFF} periods because there is current flowing out from the MIN_TON and MIN_TOFF pins. The most accurate method for calculating these losses is to measure the I_{CC} current when C_{LOAD} = 0 nF and the IC is switching at the target frequency with given min_t_{ON} and min_t_{OFF} adjust resistors. IC consumption losses can be calculated as:

$$P_{CC} = V_{CC} \times I_{CC} \quad \text{(eq. 9)}$$

Step 4 – IC die temperature arise calculation:

The die temperature can be calculated now that the total internal power losses have been determined (driver losses plus internal IC consumption losses). The package thermal resistance is specified in the maximum ratings table for a 35 μm thin copper layer with 1 in2 copper area.

The die temperature is calculated as:

$$T_{DIE} = (P_{DRV_IC} + P_{CC)} \times R_{\theta J-A} + T_A \quad \text{(eq. 10)}$$

Where:

P_{DRV_IC} is the IC driver internal power dissipation

P_{CC} is the IC control internal power dissipation

R_{J-A} is the thermal resistance from junction to ambient

T_A is the ambient temperature

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OPN coding table

NCP4306 OPN is built from prefix of NCP4306 and postfix that consist of seven letters. Meaning of these letters are shown in table 7.

Table 7. OPN CODING TABLE

NCP4306xxxxxxx			
Postfix Index	**Parameter**	**Postfix**	**Parameter**
1	Pinout	A	MIN_TON, MIN_TOFF, LLD, TRIG / DIS – 8 pins
		B	MIN_TON, LLD
		C	MIN_TOFF, LLD
		D	MIN_TON, MIN_TOFF
		E	MIN_TOFF, TRIG / DIS
		F	MIN_TON, TRIG / DIS
		G	TRIG / DIS, LLD
		H	None
2	DRV	A	DRV CLMP = 10 V
		B	DRV CLMP = 5 V
3	dV / dt + exception	A	None
		D	Flyback (dV / dt) – 100 V / μs
		H	LLC exception – multiplier 4
4	MIN_TON	A	130 ns
		B	220 ns
		C	310 ns
		D	400 ns
		E	500 ns
		F	600 ns
		G	700 ns
		H	800 ns
		I	1000 ns
		J	1200 ns
		K	1400 ns
		L	1700 ns
		M	2000 ns
		Z	External
5	MIN_TOFF	A	0.9 μs
		B	1.0 μs
		C	1.1 μs
		D	1.2 μs
		E	1.4 μs
		F	1.6 μs
		G	1.8 μs
		H	2.0 μs
		I	2.2 μs
		J	2.4 μs
		K	2.6 μs
		L	2.9 μs
		M	3.2 μs
		N	3.5 μs
		O	3.9 μs
		Z	External

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Table 7. OPN CODING TABLE (continued)

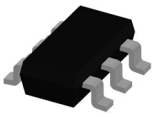
NCP4306xxxxxxx			
Postfix Index	**Parameter**	**Postfix**	**Parameter**
6	LLD	A	68 µs
		B	130 µs
		C	280 µs
		D	540 µs
		E	1075 µs
		F	Disabled
		Z	External
7	Reserved	A	–

REVISION HISTORY

Revision	Description of Changes	Date
9	Added two new OPNs to order table.	2/3/2026

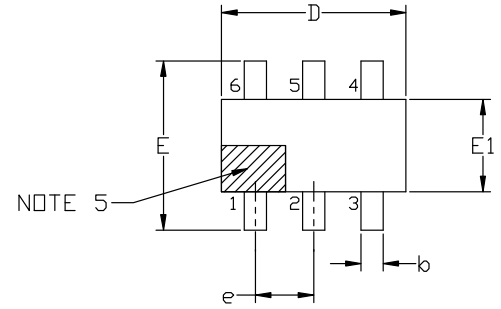
* Please note that this document has been previously updated prior to the inclusion of this revision history table and that the changes tracked only reflect what has occurred on the noted approval dates.

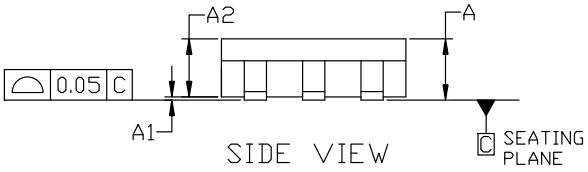
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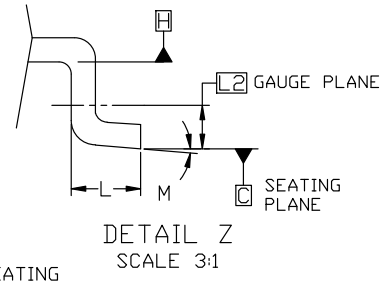


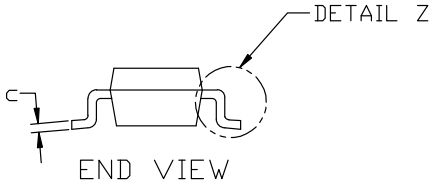
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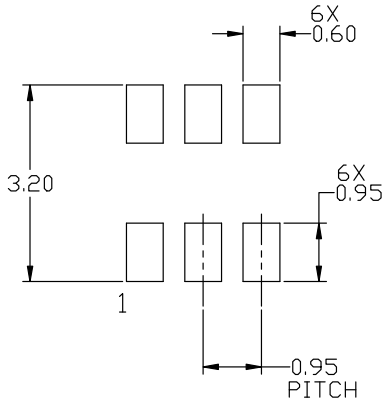






NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN 1 INDICATOR MUST BE LOCATED IN THE INDICATED ZONE

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
A2	0.80	0.90	1.00
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb-Free strategy and soldering details, please download th e ON Semiconductor Soldering and Mounting Techniques Reference manual, SOLDERRM/D.

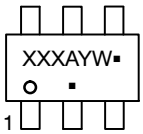
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TSOP−6 3.00x1.50x0.90, 0.95P
CASE 318G
ISSUE W

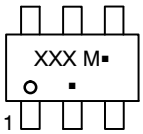
DATE 26 FEB 2024

GENERIC MARKING DIAGRAM*



IC

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package



STANDARD

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 2:
PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. BASE 2
6. COLLECTOR 2

STYLE 3:
PIN 1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out

STYLE 4:
PIN 1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD

STYLE 5:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 6:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 7:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. N/C
5. COLLECTOR
6. EMITTER

STYLE 8:
PIN 1. Vbus
2. D(in)
3. D(in)+
4. D(out)+
5. D(out)
6. GND

STYLE 9:
PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE

STYLE 10:
PIN 1. D(OUT)+
2. GND
3. D(OUT)−
4. D(IN)−
5. VBUS
6. D(IN)+

STYLE 11:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1/GATE 2

STYLE 12:
PIN 1. I/O
2. GROUND
3. I/O
4. I/O
5. VCC
6. I/O

STYLE 13:
PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1

STYLE 14:
PIN 1. ANODE
2. SOURCE
3. GATE
4. CATHODE/DRAIN
5. CATHODE/DRAIN
6. CATHODE/DRAIN

STYLE 15:
PIN 1. ANODE
2. SOURCE
3. GATE
4. DRAIN
5. N/C
6. CATHODE

STYLE 16:
PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE

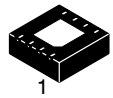
STYLE 17:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR

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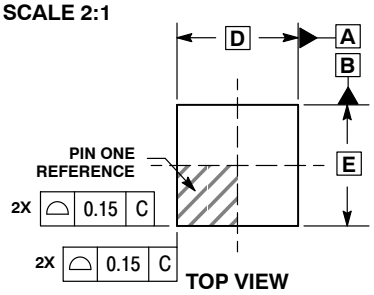
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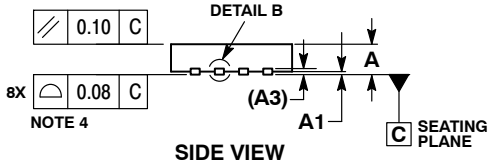
DFN8, 4x4
CASE 488AF
ISSUE C

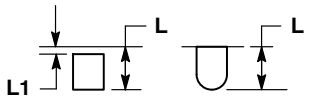
DATE 15 JAN 2009

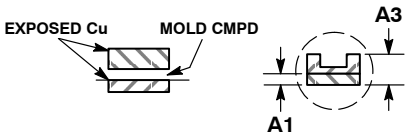


SCALE 2:1



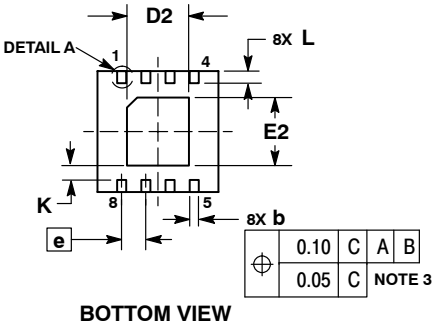




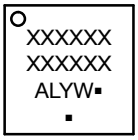


NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. DETAILS A AND B SHOW OPTIONAL CONSTRUCTIONS FOR TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	4.00 BSC	
D2	1.91	2.21
E	4.00 BSC	
E2	2.09	2.39
e	0.80 BSC	
K	0.20	---
L	0.30	0.50
L1	---	0.15



GENERIC MARKING DIAGRAM*

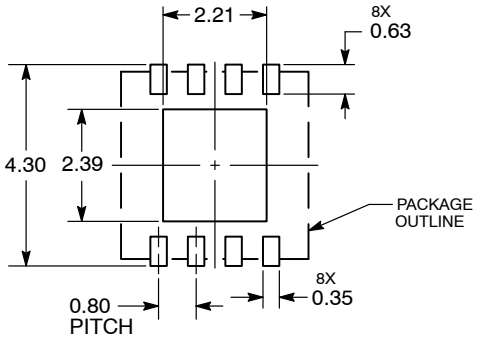


XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

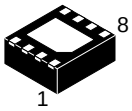
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DESCRIPTION:	**DFN8, 4X4, 0.8P**	**PAGE 1 OF 1**

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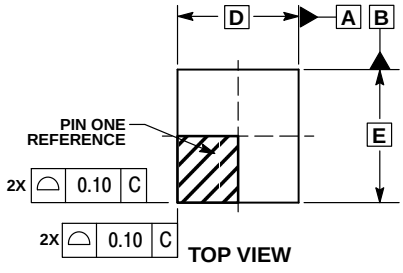
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DFN8, 2.0x2.2, 0.5P
CASE 506BP
ISSUE A

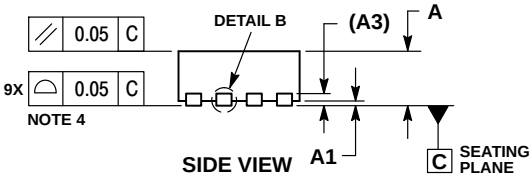
DATE 13 JAN 2010



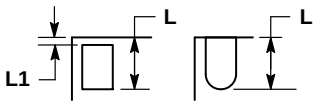
SCALE 4:1



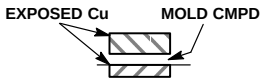
TOP VIEW



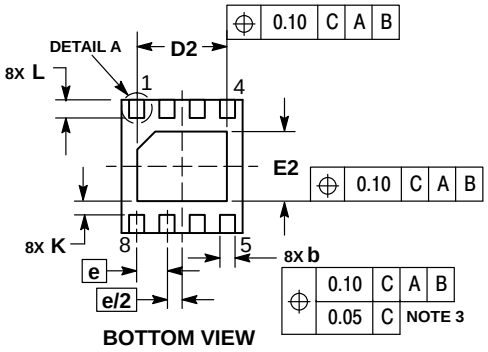
SIDE VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS



DETAIL B
ALTERNATE CONSTRUCTIONS

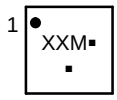


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	TYP	MAX
A	0.80	---	1.00
A1	0.00	---	0.05
A3		0.20 REF	
b	0.20	---	0.30
D		2.00 BSC	
D2	1.43	---	1.53
E		2.20 BSC	
E2	1.05	---	1.25
e		0.50 BSC	
K	0.20	0.22	0.30
L	0.25	---	0.35
L1	---	---	0.15

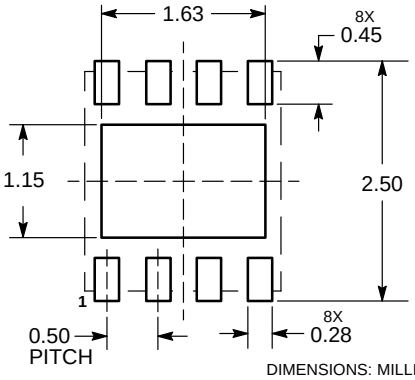
GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Device

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**DFN8, 2.0X2.2, 0.5P**		**PAGE 1 OF 1**

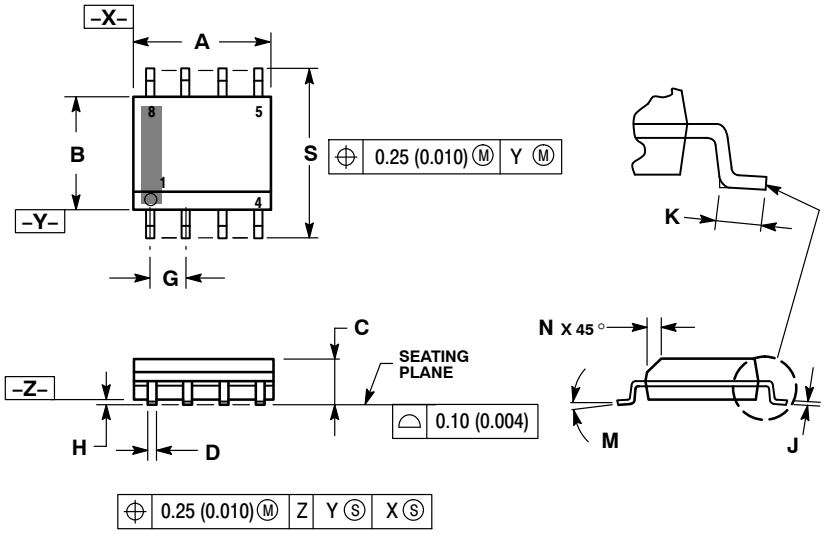
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SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

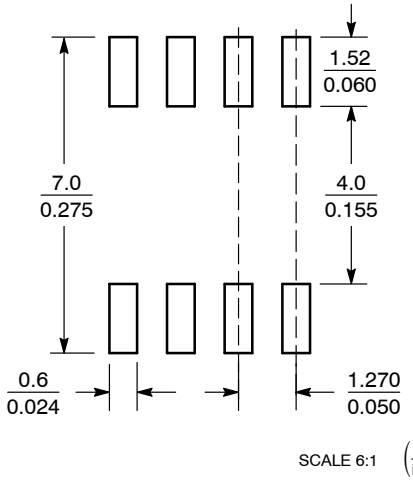
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

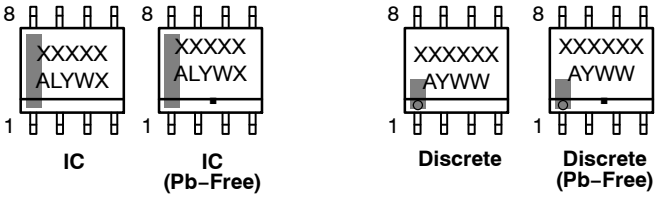
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

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SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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