MOSFET – Power, Single, N-Channel

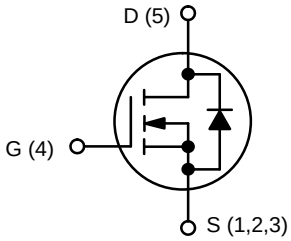
60 V, 1.2 mΩ, 287 A

NTMFS5C604NL

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
60 V	1.2 mΩ @ 10 V	287 A
	1.7 mΩ @ 4.5 V	

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- These Devices are Pb-Free and are RoHS Compliant



N-CHANNEL MOSFET

MAXIMUM RATINGS (T_J = 25 °C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	60	V
Gate-to-Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	T_C = 25 °C	I_D	287	A
		T_C = 100 °C		203	
Power Dissipation $R_{\theta JC}$ (Note 1)		T_C = 25 °C	P_D	200	W
		T_C = 100 °C		100	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	T_A = 25 °C	I_D	40	A
		T_A = 100 °C		28	
Power Dissipation $R_{\theta JA}$ (Notes 1 & 2)		T_A = 25 °C	P_D	3.9	W
		T_A = 100 °C		1.9	
Pulsed Drain Current	T_A = 25 °C, t_p = 10 μs		I_{DM}	900	A
Operating Junction and Storage Temperature			T_J, T_{stg}	−55 to +175	°C
Source Current (Body Diode)			I_S	203	A
Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)}$ = 22 A)			E_{AS}	776	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

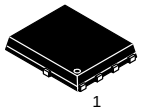
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

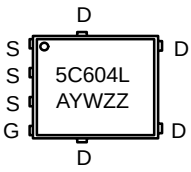
Parameter	Symbol	Value	Unit
Junction-to-Case − Steady State	$R_{\theta JC}$	0.75	°C/W
Junction-to-Ambient − Steady State (Note 2)	$R_{\theta JA}$	39	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm^2, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

MARKING DIAGRAM



DFN5 (SO-8FL)
CASE 506EZ



5C604L = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

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ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				22.9		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 60 V	T_J = 25 °C			10	μA
			T_J = 125 °C			250	
Gate-to-Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 20 V				100	nA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		1.2		2.0	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				−5.9		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 50 A		0.93	1.2	mΩ
		V_{GS} = 4.5 V	I_D = 50 A		1.25	1.7	
Forward Transconductance	g_{FS}	V_{DS} = 15 V, I_D = 50 A			180		S
Gate Resistance	R_G	T_A = 25 °C				3.4	Ω
CHARGES AND CAPACITANCES							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 25 V			8900		pF
Output Capacitance	C_{OSS}				3750		
Reverse Transfer Capacitance	C_{RSS}				40		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 30 V; I_D = 50 A			52		nC
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 30 V; I_D = 50 A			120		
Threshold Gate Charge	$Q_{G(TH)}$	V_{GS} = 4.5 V, V_{DS} = 30 V; I_D = 50 A			6.4		
Gate-to-Source Charge	Q_{GS}				21.4		
Gate-to-Drain Charge	Q_{GD}				12.7		
Plateau Voltage	V_{GP}				2.8		V
SWITCHING CHARACTERISTICS (Note 5)							
Turn-On Delay Time	$t_{d(ON)}$	V_{GS} = 4.5 V, V_{DS} = 30 V, I_D = 50 A, R_G = 2.5 Ω			32.9		ns
Rise Time	t_r				29.9		
Turn-Off Delay Time	$t_{d(OFF)}$				60.3		
Fall Time	t_f				25.2		
DRAIN-SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 50 A	T_J = 25 °C		0.78	1.2	V
			T_J = 125 °C		0.64		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dIS/dt = 100 A/μs, I_S = 50 A			98		ns
Charge Time	t_a				45		
Discharge Time	t_b				53		
Reverse Recovery Charge	Q_{RR}				190		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

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TYPICAL CHARACTERISTICS

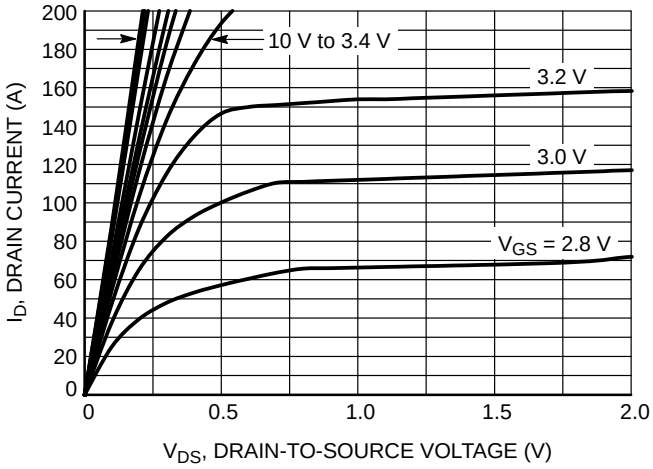


Figure 1. On-Region Characteristics

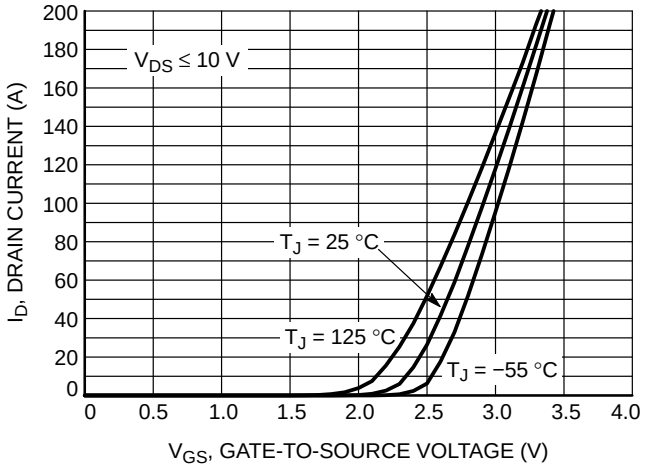


Figure 2. Transfer Characteristics

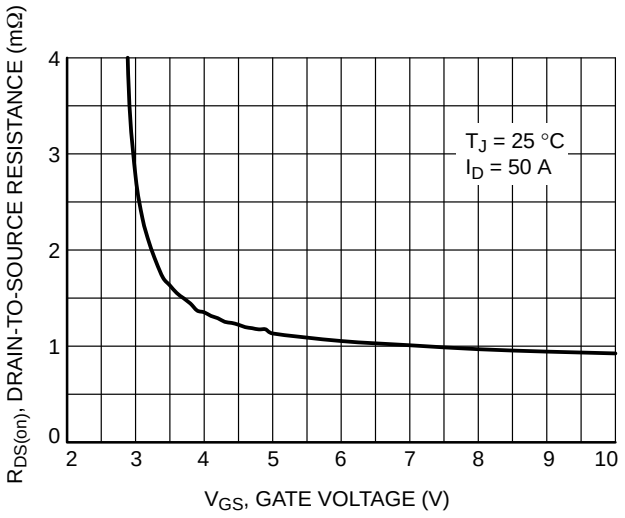


Figure 3. On-Resistance vs. Gate-to-Source Voltage

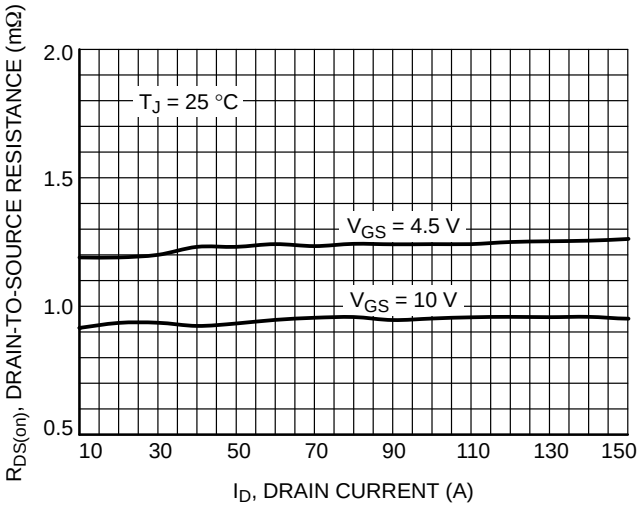


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

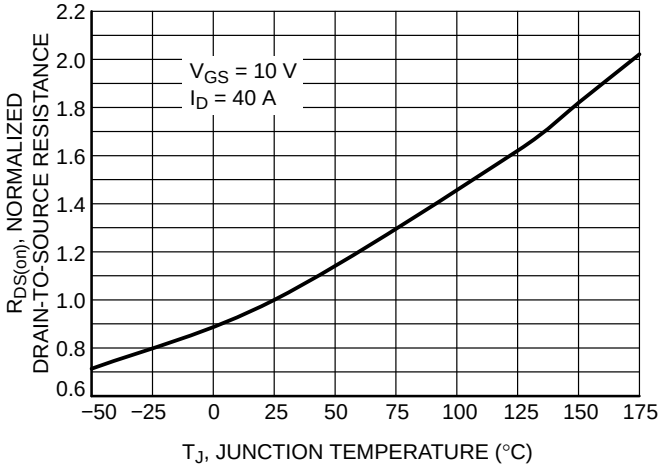


Figure 5. On-Resistance Variation with Temperature

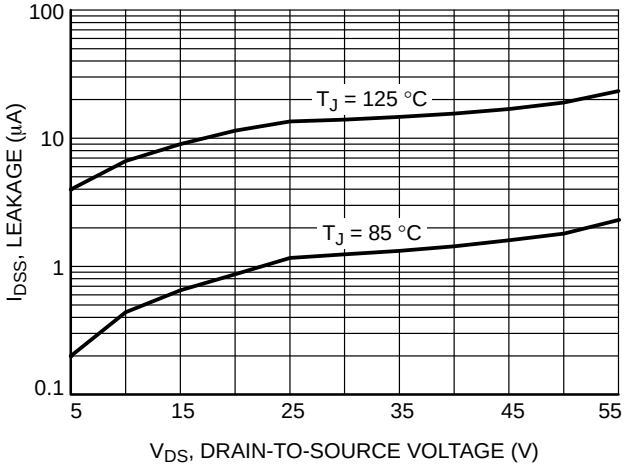


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS

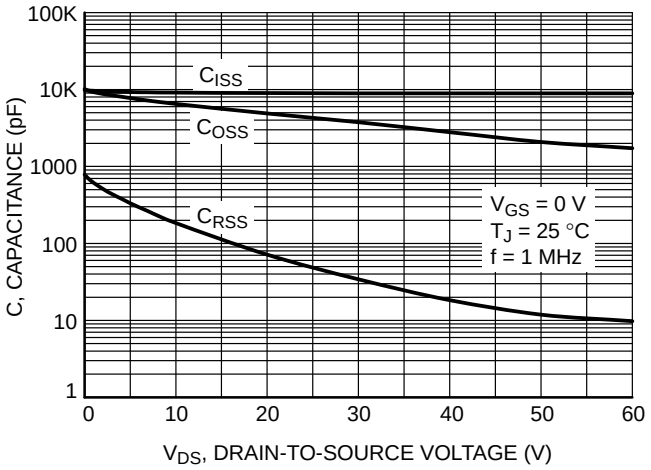


Figure 7. Capacitance Variation

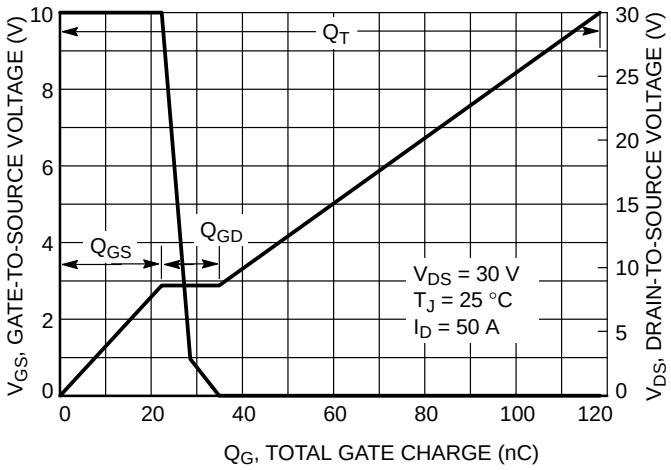


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

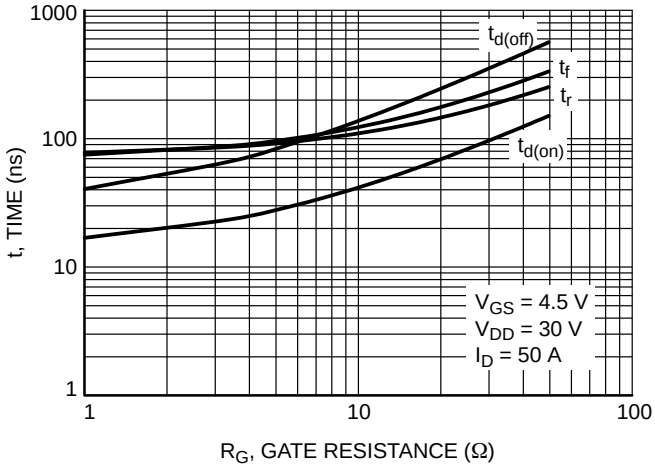


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

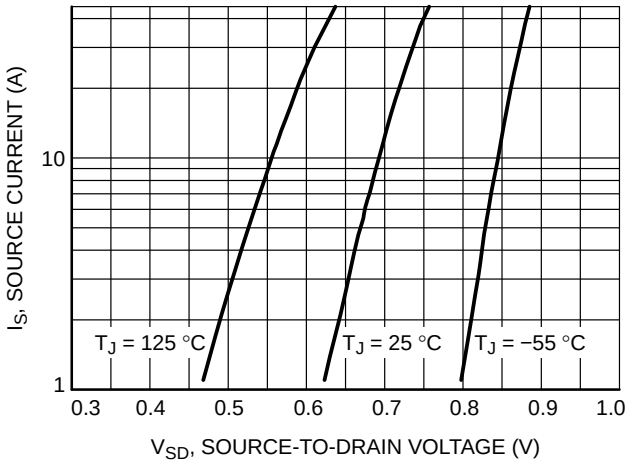


Figure 10. Diode Forward Voltage vs. Current

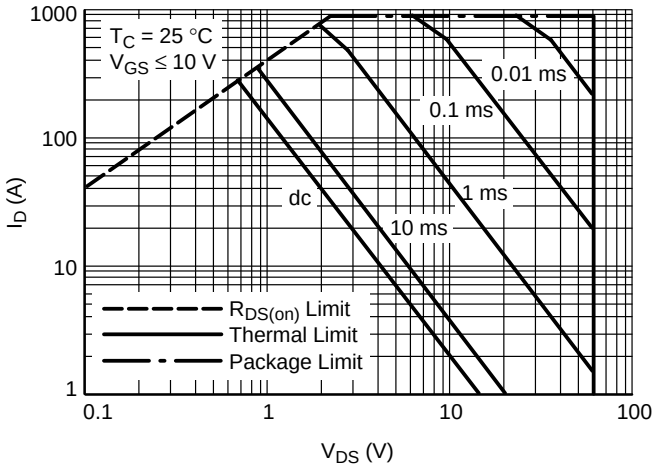


Figure 11. Safe Operating Area

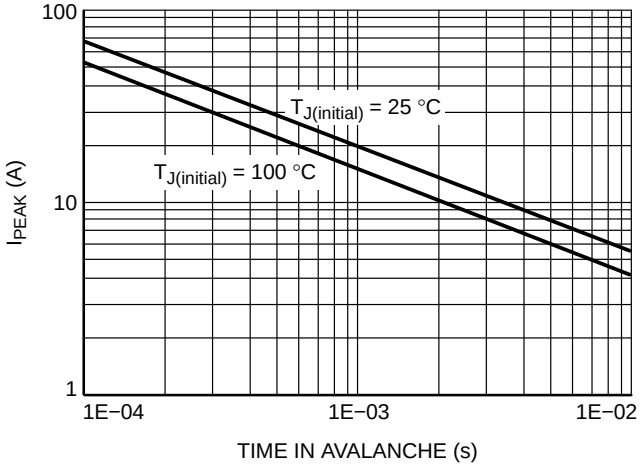


Figure 12. I_{PEAK} vs. Time in Avalanche

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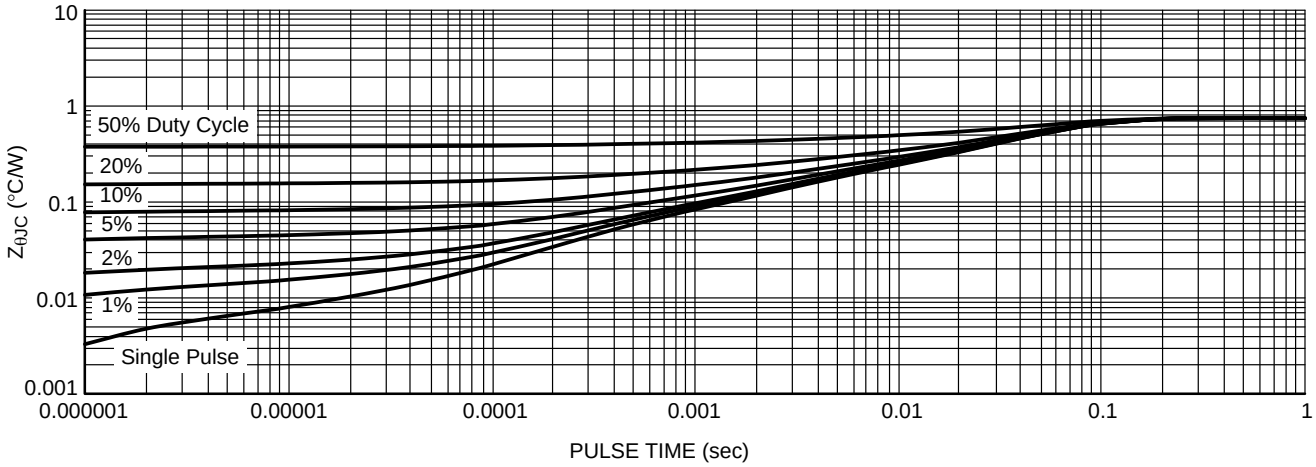


Figure 13. Thermal Characteristics

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NTMFS5C604NLT1G	5C604L	DFN5 (Pb-Free)	1500 / Tape & Reel
NTMFS5C604NLT3G	5C604L	DFN5 (Pb-Free)	5000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

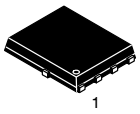
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REVISION HISTORY

Revision	Description of Changes	Date
9	Rebranded the document to **onsemi** format.	1/20/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

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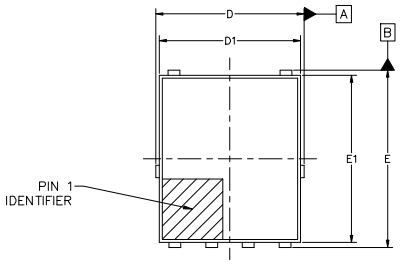


SCALE 2:1

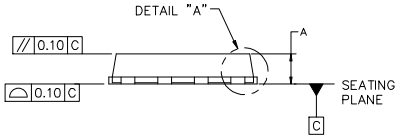
DFN5, 4.90 x 5.90 x 1.00, 1.27P
CASE 506EZ
ISSUE B

DATE 16 SEP 2024

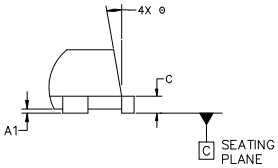
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.



TOP VIEW

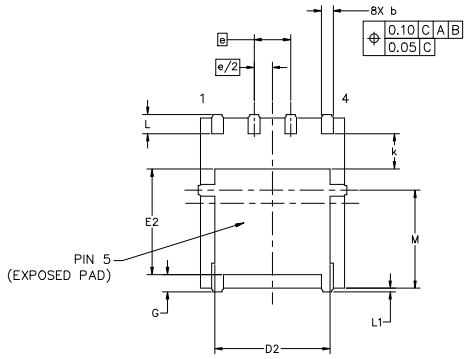


SIDE VIEW



DETAIL "A"
SCALED 2:1

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.80	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
k	1.10	1.20	1.40
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0°	---	12°



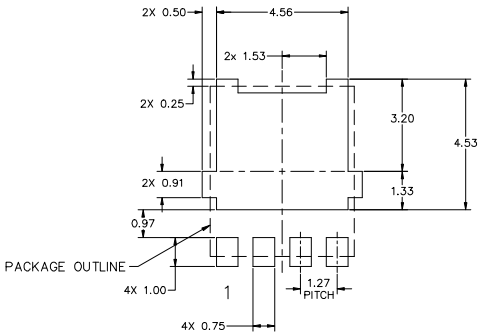
BOTTOM VIEW

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb−Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**DFN5, 4.90 x 5.90 x 1.00, 1.27P**		**PAGE 1 OF 1**

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