Voltage Detector Series with Programmable Delay

NCP302, NCP303

The NCP302 and NCP303 series are second generation ultra−low current voltage detectors that contain a programmable time delay generator. These devices are specifically designed for use as reset controllers in portable microprocessor based systems where extended battery life is paramount.

Each series features a highly accurate undervoltage detector with hysteresis and an externally programmable time delay generator. This combination of features prevents erratic system reset operation.

The NCP302 series consists of complementary output devices that are available with either an active high or active low reset. The NCP303 series has an open drain N−Channel output with an active low reset output.

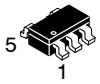
Features

- Quiescent Current of 0.5 μA Typical
- High Accuracy Undervoltage Threshold of 2.0%
- Externally Programmable Time Delay Generator
- Wide Operating Voltage Range of 0.8 V to 10 V
- Complementary or Open Drain Output
- Active Low or Active High Reset
- Specified Over the −40°C to +125°C Temperature Range (Except for Voltage Options from 0.9 to 1.1 V)
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

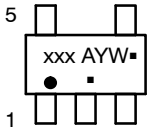
Typical Applications

- Microprocessor Reset Controller
- Low Battery Detection
- Power Fail Indicator
- Battery Backup Detection

MARKING DIAGRAM



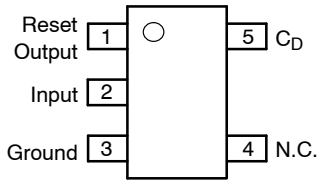
TSOP−5/ SOT23−5 CASE 483



xxx	= Specific Device Code
A	= Assembly Location
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



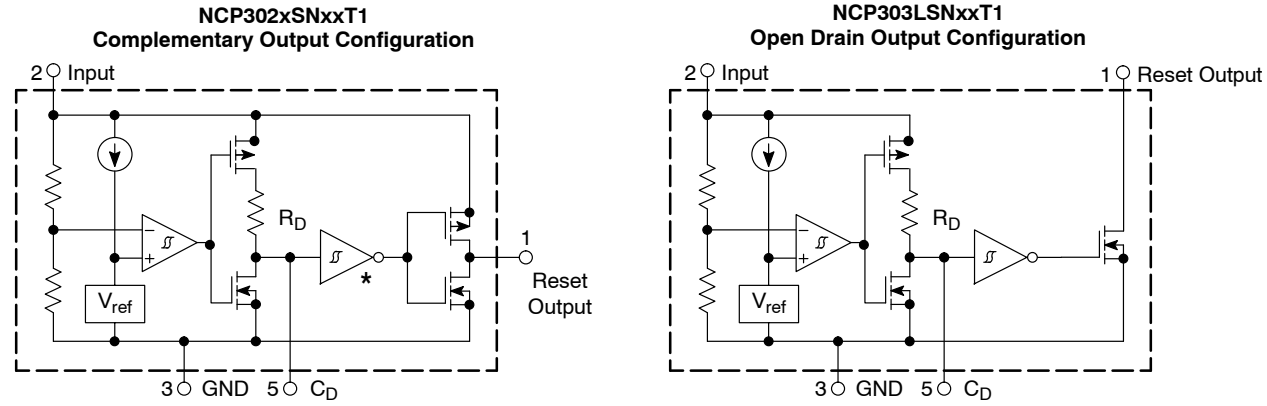
(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the ordering information section on page 22 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 23.

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* Inverter for active low devices.
Buffer for active high devices.

This device contains 28 active transistors.

Figure 1. Representative Block Diagrams

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Power Supply Voltage (Pin 2)	V_{in}	12	V
Delay Capacitor Pin Voltage (Pin 5)	V_{CD}	−0.3 to V_{in} + 0.3	V
Output Voltage (Pin 1) Complementary, NCP302 N−Channel Open Drain, NCP303	V_{OUT}	 −0.3 to V_{in} + 0.3 −0.3 to 12	V
Output Current (Pin 1) (Note 2)	I_{OUT}	70	mA
Thermal Resistance Junction−to−Air	$R_{\theta JA}$	250	°C/W
Maximum Junction Temperature	T_J	+150	°C
Operating Ambient Temperature Range All Voltage Options: 0.9 V to 1.1 V All Voltage Options: 1.2 V to 4.9 V	 T_A T_A	 −40 to +85 −40 to +125	 °C °C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Moisture Sensitivity Level	MSL	1	
Latchup Performance (Note 3) Positive Negative	$I_{LATCHUP}$	 200 200	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series contains ESD protection and exceeds the following tests:
   Human Body Model 2000 V per MIL−STD−883, Method 3015.
   Machine Model Method 200 V.
2. The maximum package power dissipation limit must not be exceeded.

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

3. Maximum ratings per JEDEC standard JESD78.

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ELECTRICAL CHARACTERISTICS (For all values T_A = −40°C to +125°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
NCP302/3 − 0.9 (T_A = 25°C for voltage options from 0.9 to 1.1 V)					
Detector Threshold (Pin 2, V_{in} Decreasing)	V_{DET-}	0.882	0.900	0.918	V
Detector Threshold Hysteresis (Pin 2, V_{in} Increasing)	V_{HYS}	0.027	0.045	0.063	V
Supply Current (Pin 2) (V_{in} = 0.8 V) (V_{in} = 2.9 V)	I_{in}	 – –	 0.20 0.45	 0.6 1.2	µA
Maximum Operating Voltage (Pin 2)	$V_{in(max)}$	–	–	10	V
Minimum Operating Voltage (Pin 2) (T_A = −40°C to 85°C)	$V_{in(min)}$	– –	0.55 0.65	0.70 0.80	V
Reset Output Current (Pin 1, Active Low 'L' Suffix Devices) Nch Sink Current, NCP302, NCP303 (V_{OUT} = 0.05V, V_{in} = 0.70V) (V_{OUT} = 0.50V, V_{in} = 0.85V) Pch Source Current, NCP302 (V_{OUT} = 2.4V, V_{in} = 4.5V)	I_{OUT}	 0.01 0.05 1.0	 0.05 0.50 6.0	 – – –	mA
Reset Output Current (Pin 1, Active High 'H' Suffix Devices) Nch Sink Current, NCP302, NCP303 (V_{OUT} = 0.5 V, V_{in} = 1.5 V) Pch Source Current, NCP302 (V_{OUT} = 0.4 V, V_{in} = 0.7 V) (V_{OUT} = GND, V_{in} = 0.8 V)	I_{OUT}	 1.05 0.011 0.014	 2.5 0.04 0.08	 – – –	mA
C_D Delay Pin Threshold Voltage (Pin 5) (V_{in} = 0.99 V)	V_{TCD}	0.50	0.67	0.84	V
Delay Capacitor Pin Sink Current (Pin 5) (V_{in} = 0.7 V, V_{CD} = 0.1V) (V_{in} = 0.85 V, V_{CD} = 0.5V)	I_{CD}	 2.0 10	 120 300	 – –	µA
Delay Pullup Resistance (Pin 5)	R_D	0.5	1.0	2.0	MΩ
NCP302/3 − 1.8					
Detector Threshold (Pin 2, V_{in} Decreasing) (T_A = 25°C) (T_A = −40°C to 125°C)	V_{DET-}	1.764 1.746	1.800 –	1.836 1.854	V
Detector Threshold Hysteresis (Pin 2, V_{in} Increasing)	V_{HYS}	0.054	0.090	0.126	V
Supply Current (Pin 2) (V_{in} = 1.7 V) (V_{in} = 3.8 V)	I_{in}	 – –	 0.23 0.48	 0.7 1.3	µA
Maximum Operating Voltage (Pin 2)	$V_{in(max)}$	–	–	10	V
Minimum Operating Voltage (Pin 2) (T_A = 25°C) (T_A = −40°C to 125°C)	$V_{in(min)}$	– –	0.55 0.65	0.70 0.80	V
Reset Output Current (Pin 1, Active Low 'L' Suffix Devices) Nch Sink Current, NCP302, NCP303 (V_{OUT} = 0.05V, V_{in} = 0.70V) (V_{OUT} = 0.50V, V_{in} = 1.5V) Pch Source Current, NCP302 (V_{OUT} = 2.4V, V_{in} = 4.5V)	I_{OUT}	 0.01 1.0 1.0	 0.05 2.0 6.0	 – – –	mA
Reset Output Current (Pin 1, Active High 'H' Suffix Devices) Nch Sink Current, NCP302, NCP303 (V_{OUT} = 0.5 V, V_{in} = 5.0 V) Pch Source Current, NCP302 (V_{OUT} = 0.4 V, V_{in} = 0.7 V) (V_{OUT} = GND, V_{in} = 1.5 V)	I_{OUT}	 6.3 0.011 0.525	 11 0.04 0.6	 – – –	mA
C_D Delay Pin Threshold Voltage (Pin 5) (V_{in} = 1.98 V)	V_{TCD}	0.99	1.34	1.68	V

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ELECTRICAL CHARACTERISTICS (continued) (For all values T_A = −40°C to +125°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
NCP302/3 – 1.8					
Delay Capacitor Pin Sink Current (Pin 5) (V_{in} = 0.7 V, V_{CD} = 0.1V) (V_{in} = 1.5 V, V_{CD} = 0.5V)	I_{CD}	 2.0 200	 120 1600	 – –	µA
Delay Pullup Resistance (Pin 5)	R_D	0.5	1.0	2.0	MΩ
NCP302/3 – 2.0					
Detector Threshold (Pin 2, V_{in} Decreasing) (T_A = 25°C) (T_A = −40°C to 125°C)	V_{DET-}	1.96 1.94	2.00 –	2.04 2.06	V
Detector Threshold Hysteresis (Pin 2, V_{in} Increasing)	V_{HYS}	0.06	0.10	0.14	V
Supply Current (Pin 2) (V_{in} = 1.9 V) (V_{in} = 4.0 V)	I_{in}	 – –	 0.23 0.48	 0.8 1.3	µA
Maximum Operating Voltage (Pin 2)	$V_{in(max)}$	–	–	10	V
Minimum Operating Voltage (Pin 2) (T_A = 25°C) (T_A = −40°C to 125°C)	$V_{in(min)}$	– –	0.55 0.65	0.70 0.80	V
Reset Output Current (Pin 1, Active Low 'L' Suffix Devices) Nch Sink Current, NCP302, NCP303 (V_{OUT} = 0.05V, V_{in} = 0.70V) (V_{OUT} = 0.50V, V_{in} = 1.5V) Pch Source Current, NCP302 (V_{OUT} = 2.4V, V_{in} = 4.5V)	I_{OUT}	 0.01 1.0 1.0	 0.14 3.5 9.7	 – – –	mA
Reset Output Current (Pin 1, Active High 'H' Suffix Devices) Nch Sink Current, NCP302, NCP303 (V_{OUT} = 0.5 V, V_{in} = 5.0 V) Pch Source Current, NCP302 (V_{OUT} = 0.4 V, V_{in} = 0.7 V) (V_{OUT} = GND, V_{in} = 1.5 V)	I_{OUT}	 6.3 0.011 0.525	 11 0.04 0.6	 – – –	mA
C_D Delay Pin Threshold Voltage (Pin 5) (V_{in} = 2.2 V)	V_{TCD}	1.10	1.49	1.87	V
Delay Capacitor Pin Sink Current (Pin 5) (V_{in} = 0.7 V, V_{CD} = 0.1V) (V_{in} = 1.5 V, V_{CD} = 0.5V)	I_{CD}	 2.0 200	 250 3600	 – –	µA
Delay Pullup Resistance (Pin 5)	R_D	0.5	1.0	2.0	MΩ
NCP302/3– 2.7					
Detector Threshold (Pin 2, V_{in} Decreasing) (T_A = 25°C) (T_A = −40°C to 125°C)	V_{DET-}	2.646 2.619	2.700 –	2.754 2.781	V
Detector Threshold Hysteresis (Pin 2, V_{in} Increasing)	V_{HYS}	0.081	0.135	0.189	V
Supply Current (Pin 2) (V_{in} = 2.6 V) (V_{in} = 4.7 V)	I_{in}	 – –	 0.25 0.50	 0.8 1.3	µA
Maximum Operating Voltage (Pin 2)	$V_{in(max)}$	–	–	10	V
Minimum Operating Voltage (Pin 2) (T_A = 25°C) (T_A = −40°C to 125°C)	$V_{in(min)}$	– –	0.55 0.65	0.70 0.80	V
Reset Output Current (Pin 1, Active Low 'L' Suffix Devices) Nch Sink Current, NCP302, NCP303 (V_{OUT} = 0.05V, V_{in} = 0.70V) (V_{OUT} = 0.50V, V_{in} = 1.5V) Pch Source Current, NCP302 (V_{OUT} = 2.4V, V_{in} = 4.5V)	I_{OUT}	 0.01 1.0 1.0	 0.14 3.5 9.7	 – – –	mA
Reset Output Current (Pin 1, Active High 'H' Suffix Devices) Nch Sink Current, NCP302, NCP303 (V_{OUT} = 0.5 V, V_{in} = 5.0 V)	I_{OUT}	 6.3	 11	 –	mA

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ELECTRICAL CHARACTERISTICS (continued) (For all values T_A = −40°C to +125°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
NCP302/3– 2.7					
Pch Source Current, NCP302 (V_{OUT} = 0.4 V, V_{in} = 0.7 V) (V_{OUT} = GND, V_{in} = 1.5 V)		 0.011 0.525	 0.04 0.6	 – –	
C_D Delay Pin Threshold Voltage (Pin 5) (V_{in} = 2.97 V)	V_{TCD}	 1.49	 2.01	 2.53	V
Delay Capacitor Pin Sink Current (Pin 5) (V_{in} = 0.7 V, V_{CD} = 0.1V) (V_{in} = 1.5 V, V_{CD} = 0.5V)	I_{CD}	 2.0 200	 250 3600	 – –	μA
Delay Pullup Resistance (Pin 5)	R_D	0.5	1.0	2.0	MΩ
NCP302/3 – 3.0					
Detector Threshold (Pin 2, V_{in} Decreasing) (T_A = 25°C) (T_A = −40°C to 125°C)	V_{DET-}	2.94 2.91	3.00 –	3.06 3.09	V
Detector Threshold Hysteresis (Pin 2, V_{in} Increasing)	V_{HYS}	0.09	0.15	0.21	V
Supply Current (Pin 2) (V_{in} = 2.87 V) (V_{in} = 5.0 V)	I_{in}	 – –	 0.25 0.50	 0.9 1.3	μA
Maximum Operating Voltage (Pin 2)	$V_{in(max)}$	–	–	10	V
Minimum Operating Voltage (Pin 2) (T_A = 25°C) (T_A = −40°C to 125°C)	$V_{in(min)}$	– –	0.55 0.65	0.70 0.80	V
Reset Output Current (Pin 1, Active Low 'L' Suffix Devices) Nch Sink Current, NCP302, NCP303 (V_{OUT} = 0.05V, V_{in} = 0.70V) (V_{OUT} = 0.50V, V_{in} = 1.5V) Pch Source Current, NCP302 (V_{OUT} = 2.4V, V_{in} = 4.5V)	I_{OUT}	 0.01 1.0 1.0	 0.14 3.5 9.7	 – – –	mA
Reset Output Current (Pin 1, Active High 'H' Suffix Devices) Nch Sink Current, NCP302, NCP303 (V_{OUT} = 0.5 V, V_{in} = 5.0 V) Pch Source Current, NCP302 (V_{OUT} = 0.4 V, V_{in} = 0.7 V) (V_{OUT} = GND, V_{in} = 1.5 V)	I_{OUT}	 6.3 0.011 0.525	 11 0.04 0.6	 – – –	mA
C_D Delay Pin Threshold Voltage (Pin 5) (V_{in} = 3.3 V)	V_{TCD}	 1.65	 2.23	 2.81	V
Delay Capacitor Pin Sink Current (Pin 5) (V_{in} = 0.7 V, V_{CD} = 0.1V) (V_{in} = 1.5 V, V_{CD} = 0.5V)	I_{CD}	 2.0 200	 250 3600	 – –	μA
Delay Pullup Resistance (Pin 5)	R_D	0.5	1.0	2.0	MΩ
NCP302/3 – 4.5					
Detector Threshold (Pin 2, V_{in} Decreasing) (T_A = 25°C) (T_A = −40°C to 125°C)	V_{DET-}	4.410 4.365	4.500 –	4.590 4.635	V
Detector Threshold Hysteresis (Pin 2, V_{in} Increasing)	V_{HYS}	0.135	0.225	0.315	V
Supply Current (Pin 2) (V_{in} = 4.34 V) (V_{in} = 6.5 V)	I_{in}	 – –	 0.33 0.52	 1.0 1.4	μA
Maximum Operating Voltage (Pin 2)	$V_{in(max)}$	–	–	10	V
Minimum Operating Voltage (Pin 2) (T_A = 25°C) (T_A = −40°C to 125°C)	$V_{in(min)}$	– –	0.55 0.65	0.70 0.80	V
Reset Output Current (Pin 1, Active Low 'L' Suffix Devices) Nch Sink Current, NCP302, NCP303 (V_{OUT} = 0.05V, V_{in} = 0.70V) (V_{OUT} = 0.50V, V_{in} = 1.5V)	I_{OUT}	 0.01 1.0	 0.05 2.0	 – –	mA

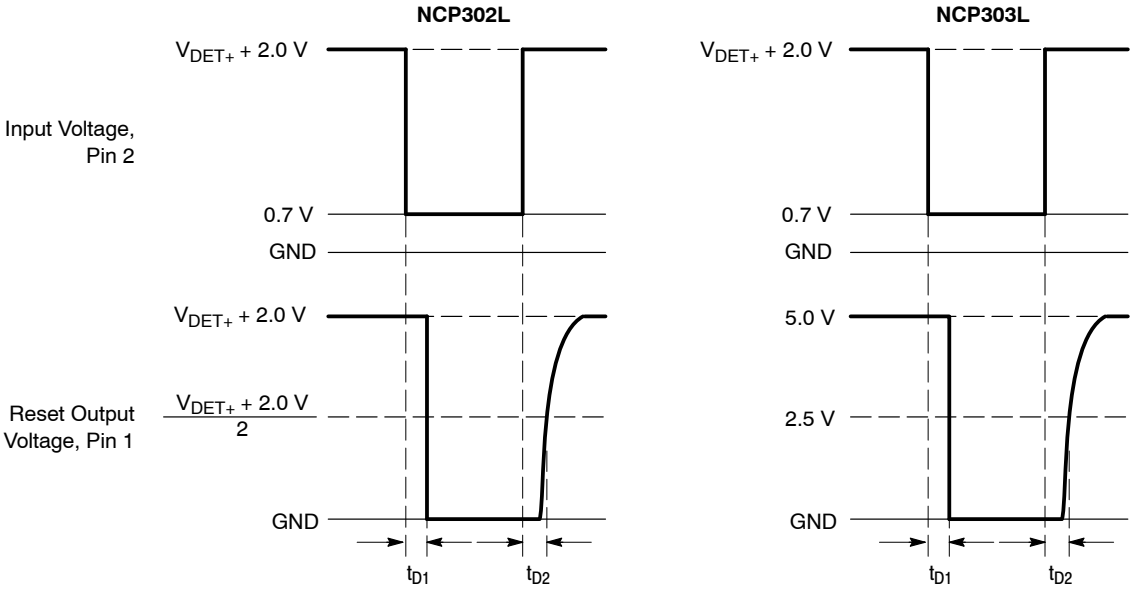
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ELECTRICAL CHARACTERISTICS (continued) (For all values T_A = −40°C to +125°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
NCP302/3 − 4.5					
Pch Source Current, NCP302 (V_{OUT} = 5.9V, V_{in} = 8.0V)		1.5	10.5	−	
Reset Output Current (Pin 1, Active High 'H' Suffix Devices)	I_{OUT}				mA
Nch Sink Current, NCP302, NCP303 (V_{OUT} = 0.5 V, V_{in} = 5.0 V)		6.3	11	−	
Pch Source Current, NCP302 (V_{OUT} = 0.4 V, V_{in} = 0.7 V) (V_{OUT} = GND, V_{in} = 1.5 V)		0.011 0.525	0.04 0.6	− −	
C_D Delay Pin Threshold Voltage (Pin 5) (V_{in} = 4.95 V)	V_{TCD}	2.25	3.04	3.83	V
Delay Capacitor Pin Sink Current (Pin 5) (V_{in} = 0.7 V, V_{CD} = 0.1V) (V_{in} = 1.5 V, V_{CD} = 0.5V)	I_{CD}	2.0 200	120 1600	− −	μA
Delay Pullup Resistance (Pin 5)	R_D	0.5	1.0	2.0	MΩ
NCP302/3 − 4.7					
Detector Threshold (Pin 2, V_{in} Decreasing) (T_A = 25°C) (T_A = −40°C to 125°C)	V_{DET-}	4.606 4.559	4.700 −	4.794 4.841	V
Detector Threshold Hysteresis (Pin 2, V_{in} Increasing)	V_{HYS}	0.141	0.235	0.329	V
Supply Current (Pin 2) (V_{in} = 4.54 V) (V_{in} = 6.7 V)	I_{in}	− −	0.34 0.53	1.0 1.4	μA
Maximum Operating Voltage (Pin 2)	$V_{in(max)}$	−	−	10	V
Minimum Operating Voltage (Pin 2) (T_A = 25°C) (T_A = −40°C to 125°C)	$V_{in(min)}$	− −	0.55 0.65	0.70 0.80	V
Reset Output Current (Pin 1, Active Low 'L' Suffix Devices)	I_{OUT}				mA
Nch Sink Current, NCP302, NCP303 (V_{OUT} = 0.05V, V_{in} = 0.70V) (V_{OUT} = 0.50V, V_{in} = 1.5V)		0.01 1.0	0.05 2.0	− −	
Pch Source Current, NCP302 (V_{OUT} = 5.9V, V_{in} = 8.0V)		1.5	10.5	−	
Reset Output Current (Pin 1, Active High 'H' Suffix Devices)	I_{OUT}				mA
Nch Sink Current, NCP302, NCP303 (V_{OUT} = 0.5 V, V_{in} = 5.0 V)		6.3	11	−	
Pch Source Current, NCP302 (V_{OUT} = 0.4 V, V_{in} = 0.7 V) (V_{OUT} = GND, V_{in} = 1.5 V)		0.011 0.525	0.04 0.6	− −	
C_D Delay Pin Threshold Voltage (Pin 5) (V_{in} = 5.17 V)	V_{TCD}	2.59	3.49	4.40	V
Delay Capacitor Pin Sink Current (Pin 5) (V_{in} = 0.7 V, V_{CD} = 0.1V) (V_{in} = 1.5 V, V_{CD} = 0.5V)	I_{CD}	2.0 200	120 1600	− −	μA
Delay Pullup Resistance (Pin 5)	R_D	0.5	1.0	2.0	MΩ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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NCP302 and NCP303 series are measured with a 10 pF capacitive load. NCP303 has an additional 470 k pullup resistor connected from the reset output to +5.0 V. The reset output voltage waveforms are shown for the active low 'L' devices. Output time delay t_{D1} and t_{D2} are dependent upon the delay capacitance. Refer to Figures 30, 31, and 32. The upper detector threshold, V_{DET+} is the sum of the lower detector threshold, V_{DET-} plus the input hysteresis, V_{HYS}.

Figure 2. Measurement Conditions for t_{D1} and t_{D2}

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Table 1. ELECTRICAL CHARACTERISTIC TABLE FOR 0.9 – 4.9 V

NCP302 Series	Detector Threshold			Detector Threshold Hysteresis			Supply Current		Nch Sink Current		Pch Source Current
							V_{in} Low	V_{in} High	V_{in} Low	V_{in} High	
	V_{DET-} (V) (Note 4)			V_{HYS} (V)			I_{in} (μA) (Note 5)	I_{in} (μA) (Note 6)	I_{OUT} (mA) (Note 7)	I_{OUT} (mA) (Note 8)	I_{OUT}(mA) (Note 9)
Part Number	Min	Typ	Max	Min	Typ	Max	Typ	Typ	Typ	Typ	Typ
NCP302LSN09T1	0.882	0.9	0.918	0.027	0.045	0.063	0.20	0.45	0.05	0.5	2.0
NCP302LSN15T1	1.470	1.5	1.530	0.045	0.075	0.105					
NCP302LSN18T1	1.764	1.8	1.836	0.054	0.090	0.126	0.23	0.48			
NCP302LSN20T1	1.960	2.0	2.040	0.060	0.100	0.140					
NCP302LSN27T1	2.646	2.7	2.754	0.081	0.135	0.189	0.25	0.50			
NCP302LSN30T1,	2.940	3.0	3.060	0.090	0.150	0.210					
NCV302LSN30T1,	2.940	3.0	3.060	0.090	0.150	0.210					
NCP302LSN33T1	3.234	3.3	3.366	0.099	0.165	0.231					
NCP302LSN38T1	3.724	3.8	3.876	0.114	0.190	0.266					
NCP302LSN40T1	3.920	4.0	4.080	0.120	0.200	0.280					3.0
NCP302LSN43T1	4.214	4.3	4.386	0.129	0.215	0.301					
NCP302LSN45T1	4.410	4.5	4.590	0.135	0.225	0.315	0.33	0.52			
NCP302LSN47T1	4.606	4.7	4.794	0.141	0.235	0.329	0.34	0.53			

4. Values shown apply at +25°C only. For voltage options greater than 1.1 V, V_{DET-} limits over operating temperature range (−40°C to +125°C) are V_{NOM} ±3%. For voltage options < 1.2 V, V_{DET-} is guaranteed only at +25°C.
5. Condition 1: 0.9 — 2.9 V, V_{in} = V_{DET-} − 0.10 V; 3.0 — 3.9 V, V_{in} = V_{DET-} − 0.13 V; 4.0 — 4.9 V, V_{in} = V_{DET-} − 0.16 V
6. Condition 2: 0.9 — 4.9 V, V_{in} = V_{DET-} + 2.0 V
7. Condition 3: 0.9 — 4.9 V, V_{in} = 0.7 V, V_{OUT} = 0.05 V, Active Low ‘L’ Suffix Devices
8. Condition 4: 0.9 — 1.0 V, V_{in} = 0.85 V, V_{OUT} = 0.5 V; 1.1 — 1.5 V, V_{in} = 1.0 V, V_{OUT} = 0.5 V; 1.6 — 4.9 V, V_{in} = 1.5 V, V_{OUT} = 0.5 V, Active Low ‘L’ Suffix Devices
9. Condition 5: 0.9 — 3.9 V, V_{in} = 4.5 V, V_{OUT} = 2.4 V; 4.0 — 4.9 V, V_{in} = 8.0 V, V_{OUT} = 5.9 V, Active Low ‘L’ Suffix Devices

Table 2. ELECTRICAL CHARACTERISTIC TABLE FOR 0.9 – 4.9 V

NCP302 Series	Detector Threshold			Detector Threshold Hysteresis			Supply Current		Nch Sink Current	Pch Source Current	
							V_{in} Low	V_{in} High		V_{in} Low	V_{in} High
	V_{DET-} (V) (Note 10)			V_{HYS} (V)			I_{in} (μA) (Note 11)	I_{in} (μA) (Note 12)	I_{OUT} (mA) (Note 13)	I_{OUT} (mA) (Note 14)	I_{OUT} (mA) (Note 15)
Part Number	Min	Typ	Max	Min	Typ	Max	Typ	Typ	Typ	Typ	Typ
NCP302HSN09T1	0.882	0.9	0.918	0.027	0.045	0.063	0.20	0.45	2.5	0.04	0.08
NCP302HSN18T1	1.764	1.8	1.836	0.054	0.090	0.126	0.23	0.48			
NCP302HSN27T1	2.646	2.7	2.754	0.081	0.135	0.189	0.25	0.50			
NCP302HSN30T1	2.940	3.0	3.060	0.090	0.150	0.210					
NCP302HSN40T1	3.920	4.0	4.080	0.120	0.200	0.280					
NCP302HSN45T1	4.410	4.5	4.590	0.135	0.225	0.315	0.33	0.52			

10. Values shown apply at +25°C only. For voltage options greater than 1.1 V, V_{DET-} limits over operating temperature range (−40°C to +125°C) are V_{NOM} ±3%. For voltage options < 1.2 V, V_{DET-} is guaranteed only at +25°C.
11. Condition 1: 0.9 — 2.9 V, V_{in} = V_{DET-} − 0.10 V; 3.0 — 3.9 V, V_{in} = V_{DET-} − 0.13 V; 4.0 — 4.9 V, V_{in} = V_{DET-} − 0.16 V
12. Condition 2: 0.9 — 4.9 V, V_{in} = V_{DET-} + 2.0 V
13. Condition 3: 0.9 — 1.4 V, V_{in} = 1.5 V, V_{OUT} = 0.5 V; 1.5 — 4.9 V, V_{in} = 5.0 V, V_{OUT} = 0.5 V, Active High ‘H’ Suffix Devices
14. Condition 4: 0.9 — 4.9 V, V_{in} = 0.7 V, V_{OUT} = 0.4 V, Active High ‘H’ Suffix Devices
15. Condition 5: 0.9 — 1.0 V, V_{in} = 0.8 V, V_{OUT} = GND; 1.1 — 1.5 V, V_{in} = 1.0 V, V_{OUT} = GND; 1.6 — 4.9 V, V_{in} = 1.5 V, V_{OUT} = GND, Active High ‘H’ Suffix Devices

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Table 3. ELECTRICAL CHARACTERISTIC TABLE FOR 0.9 – 4.9 V

NCP303 Series	Detector Threshold			Detector Threshold Hysteresis			Supply Current		Nch Sink Current	
							V_{in} Low	V_{in} High	V_{in} Low	V_{in} High
	V_{DET-} (V) (Note 16)			V_{HYS} (V)			I_{in} (μA) (Note 17)	I_{in} (μA) (Note 18)	I_{OUT} (mA) (Note 19)	I_{OUT} (mA) (Note 20)
Part Number	Min	Typ	Max	Min	Typ	Max	Typ	Typ	Typ	Typ
NCP303LSN09T1	0.882	0.9	0.918	0.027	0.045	0.063	0.20	0.45	0.05	0.5
NCP303LSN10T1	0.980	1.0	1.020	0.030	0.050	0.070				
NCP303LSN11T1	1.078	1.1	1.122	0.033	0.055	0.077				1.0
NCP303LSN13T1	1.274	1.3	1.326	0.039	0.065	0.091				
NCP303LSN14T1	1.372	1.4	1.428	0.042	0.070	0.098				
NCP303LSN15T1	1.470	1.5	1.530	0.045	0.075	0.105				
NCP303LSN16T1	1.568	1.6	1.632	0.048	0.080	0.112				2.0
NCP303LSN17T1	1.666	1.7	1.734	0.051	0.085	0.119				
NCP303LSN18T1	1.764	1.8	1.836	0.054	0.090	0.126	0.23	0.48		
NCP303LSN20T1	1.960	2.0	2.040	0.060	0.100	0.140				
NCP303LSN22T1	2.156	2.2	2.244	0.066	0.110	0.154				
NCP303LSN23T1	2.254	2.3	2.346	0.069	0.115	0.161				
NCP303LSN24T1	2.352	2.4	2.448	0.072	0.120	0.168				
NCP303LSN25T1	2.450	2.5	2.550	0.075	0.125	0.175				
NCP303LSN26T1	2.548	2.6	2.652	0.078	0.130	0.182				
NCP303LSN27T1	2.646	2.7	2.754	0.081	0.135	0.189	0.25	0.50		
NCP303LSN28T1	2.744	2.8	2.856	0.084	0.140	0.196				
NCP303LSN29T1	2.842	2.9	2.958	0.087	0.145	0.203				
NCP303LSN30T1	2.940	3.0	3.060	0.090	0.150	0.210				
NCP303LSN31T1	3.038	3.1	3.162	0.093	0.155	0.217				
NCP303LSN32T1	3.136	3.2	3.264	0.096	0.160	0.224				
NCP303LSN33T1	3.234	3.3	3.366	0.099	0.165	0.231				
NCP303LSN34T1	3.332	3.4	3.468	0.102	0.170	0.238				
NCP303LSN36T1	3.528	3.6	3.672	0.108	0.180	0.252				
NCP303LSN38T1	3.724	3.8	3.876	0.114	0.190	0.266				
NCP303LSN40T1	3.920	4.0	4.080	0.120	0.200	0.280				
NCP303LSN42T1	4.116	4.2	4.284	0.126	0.210	0.294				
NCP303LSN44T1	4.312	4.4	4.488	0.132	0.220	0.308				
NCP303LSN45T1	4.410	4.5	4.590	0.135	0.225	0.315	0.33	0.52		
NCP303LSN46T1	4.508	4.6	4.692	0.138	0.230	0.322				
NCP303LSN47T1	4.606	4.7	4.794	0.141	0.235	0.329	0.34	0.53		
NCP303LSN49T1	4.802	4.9	4.998	0.147	0.245	0.343				

16. Values shown apply at +25°C only. For voltage options greater than 1.1 V, V_{DET-} limits over operating temperature range (−40°C to +125°C) are V_{NOM} ±3%. For voltage options < 1.2 V, V_{DET-} is guaranteed only at +25°C.
17. Condition 1: 0.9 — 2.9 V, $V_{in} = V_{DET-} - 0.10$ V; 3.0 — 3.9 V, $V_{in} = V_{DET-} - 0.13$ V; 4.0 — 4.9 V, $V_{in} = V_{DET-} - 0.16$ V
18. Condition 2: 0.9 — 4.9 V, $V_{in} = V_{DET-} + 2.0$ V
19. Condition 3: 0.9 — 4.9 V, V_{in} = 0.7 V, V_{OUT} = 0.05 V, Active Low ‘L’ Suffix Devices
20. Condition 4: 0.9 — 1.0 V, V_{in} = 0.85 V, V_{OUT} = 0.5 V; 1.1 — 1.5 V, V_{in} = 1.0 V, V_{OUT} = 0.5 V; 1.6 — 4.9 V, V_{in} = 1.5 V, V_{OUT} = 0.5 V, Active Low ‘L’ Suffix Devices

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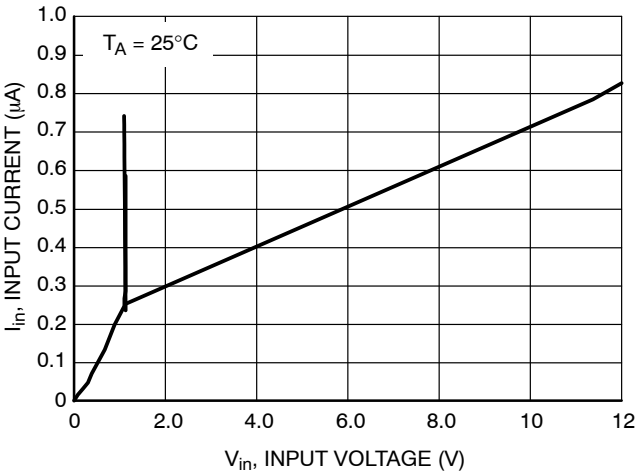


Figure 3. NCP302/3 Series 0.9 V Input Current vs. Input Voltage

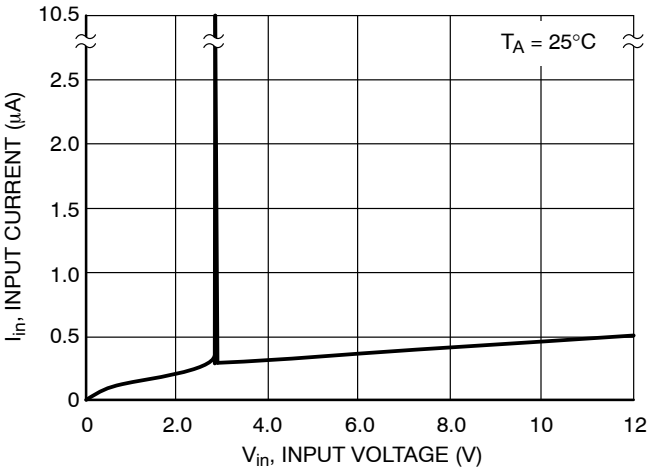


Figure 4. NCP302/3 Series 2.7 V Input Current vs. Input Voltage

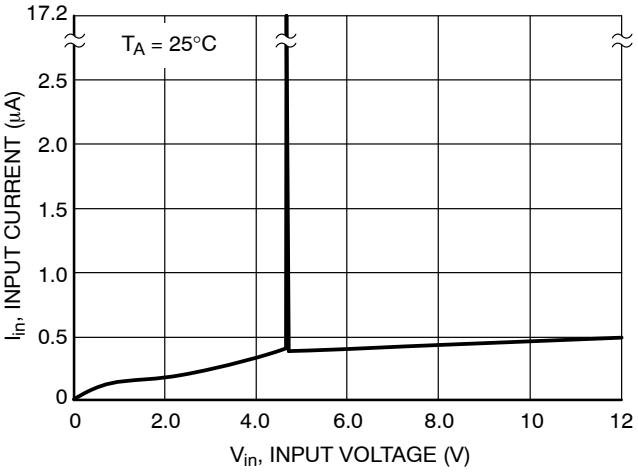


Figure 5. NCP302/3 Series 4.5 V Input Current vs. Input Voltage

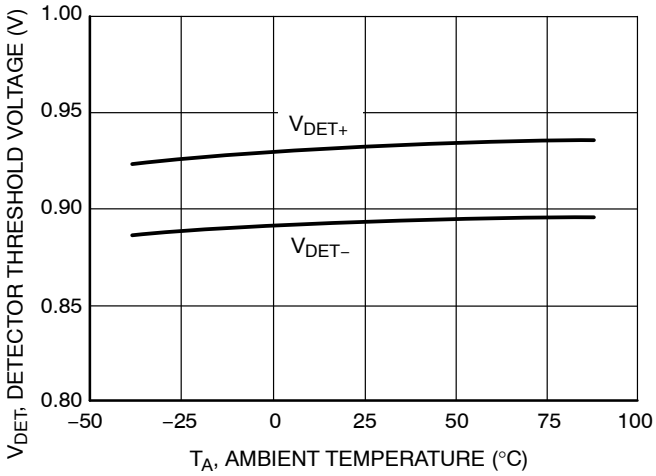


Figure 6. NCP302/3 Series 0.9 V Detector Threshold Voltage vs. Temperature

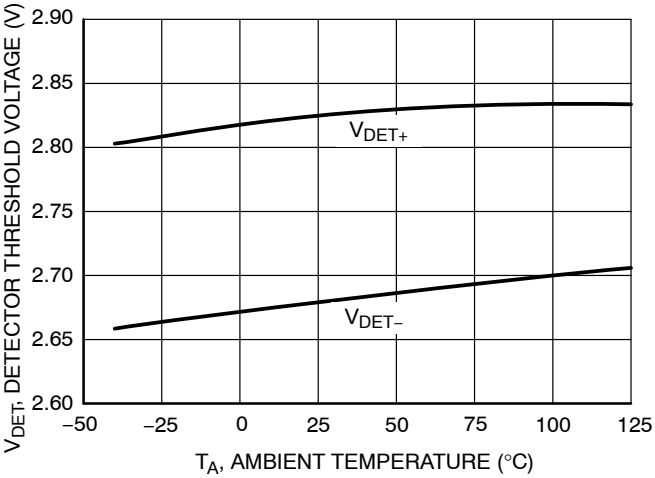


Figure 7. NCP302/3 Series 2.7 V Detector Threshold Voltage vs. Temperature

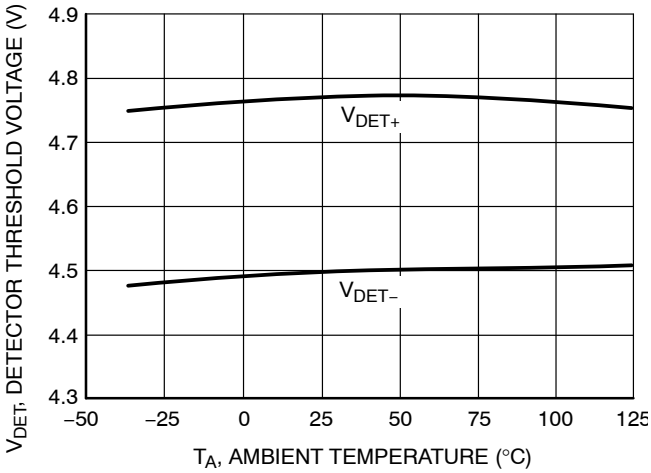


Figure 8. NCP302/3 Series 4.5 V Detector Threshold Voltage vs. Temperature

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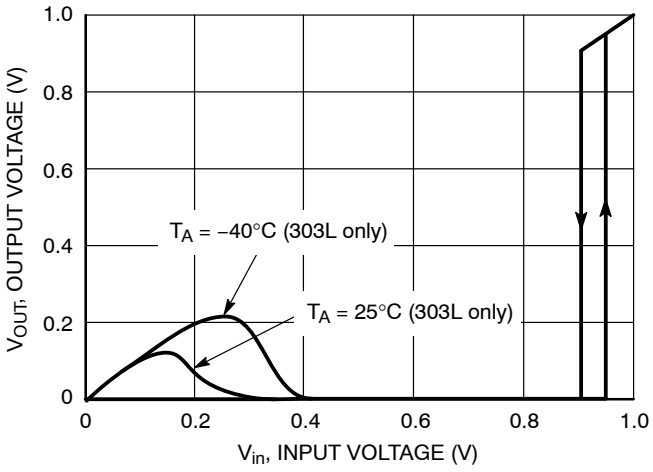


Figure 9. NCP302L/3L Series 0.9 V Reset Output Voltage vs. Input Voltage

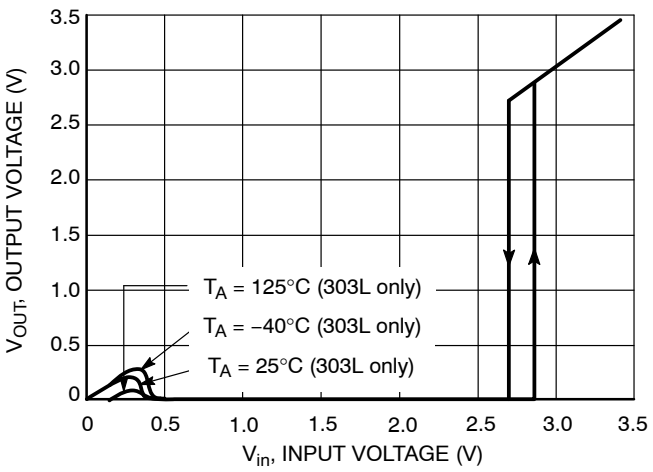


Figure 10. NCP302L/3L Series 2.7 V Reset Output Voltage vs. Input Voltage

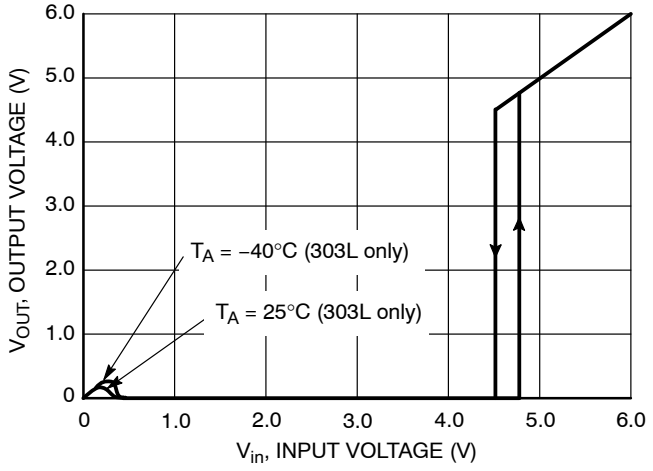


Figure 11. NCP302L/3L Series 4.5 V Reset Output Voltage vs. Input Voltage

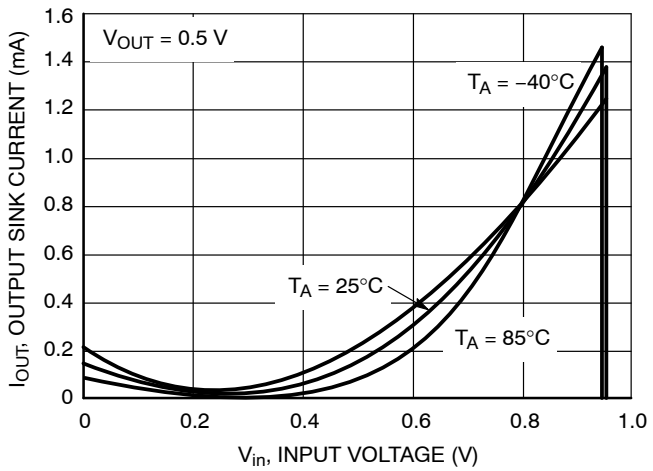


Figure 12. NCP302H/3L Series 0.9 V Reset Output Sink Current vs. Input Voltage

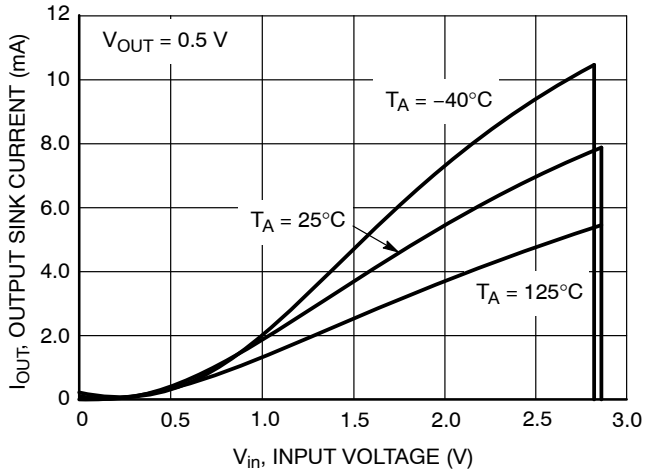


Figure 13. NCP302H/3L Series 2.7 V Reset Output Sink Current vs. Input Voltage

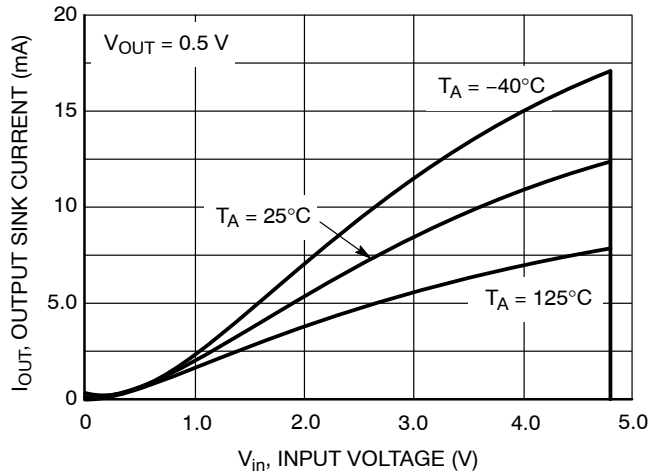


Figure 14. NCP302H/3L Series 4.5 V Reset Output Sink Current vs. Input Voltage

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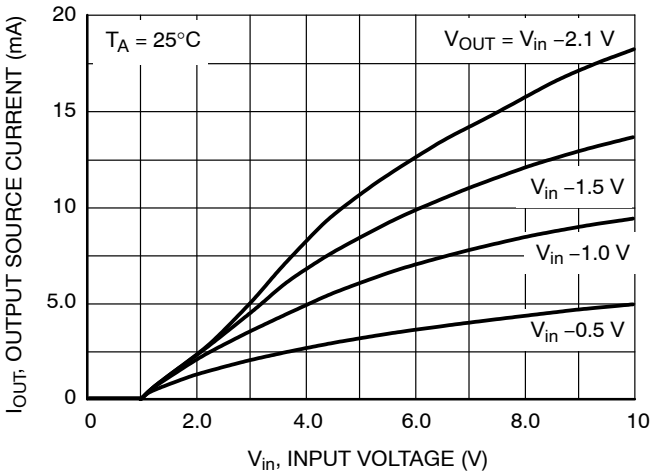


Figure 15. NCP302L Series 0.9 V Reset Output Source Current vs. Input Voltage

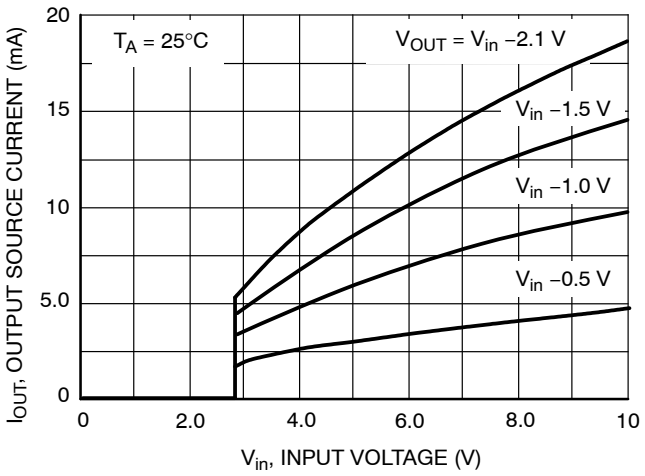


Figure 16. NCP302L Series 2.7 V Reset Output Source Current vs. Input Voltage

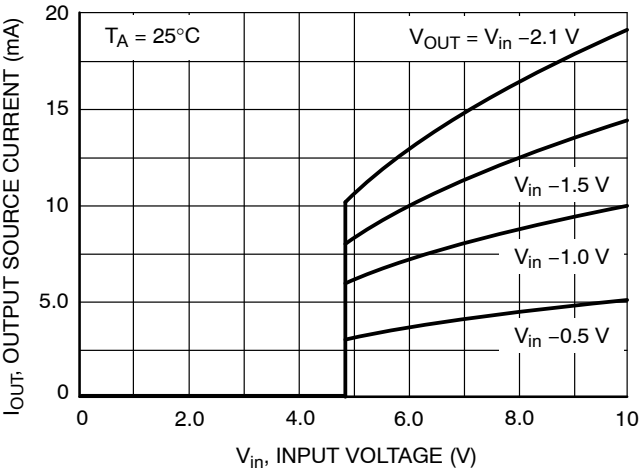


Figure 17. NCP302L Series 4.5 V Reset Output Source Current vs. Input Voltage

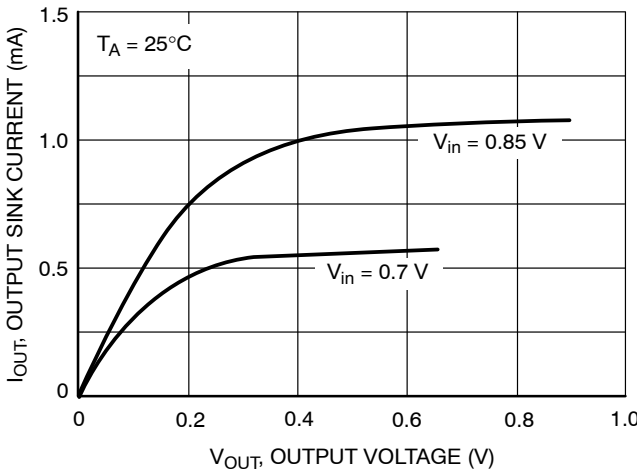


Figure 18. NCP302H/3L Series 0.9 V Reset Output Sink Current vs. Output Voltage

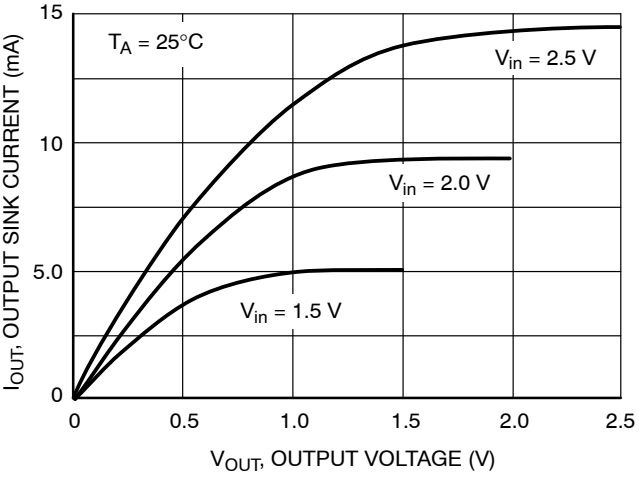


Figure 19. NCP302H/3L Series 2.7 V Reset Output Sink Current vs. Output Voltage

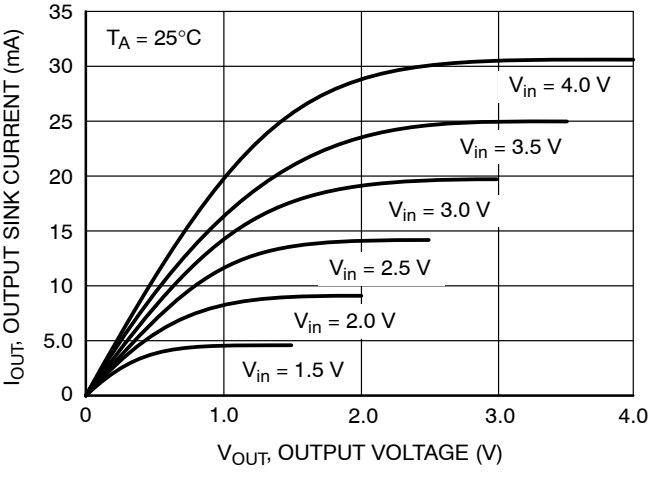


Figure 20. NCP302H/3L Series 4.5 V Reset Output Sink Current vs. Output Voltage

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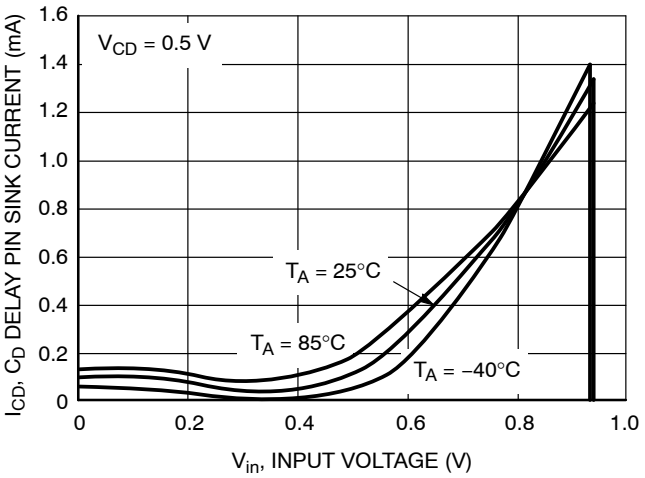


Figure 21. NCP302/3 Series 0.9 V C_D Delay Pin Sink Current vs. Input Voltage

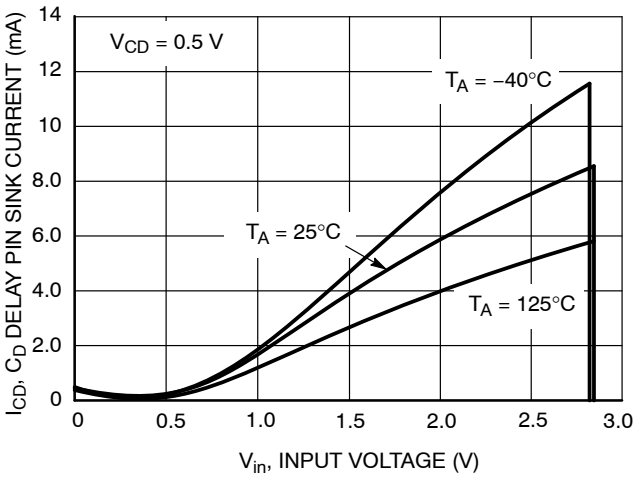


Figure 22. NCP302/3 Series 2.7 V C_D Delay Pin Sink Current vs. Input Voltage

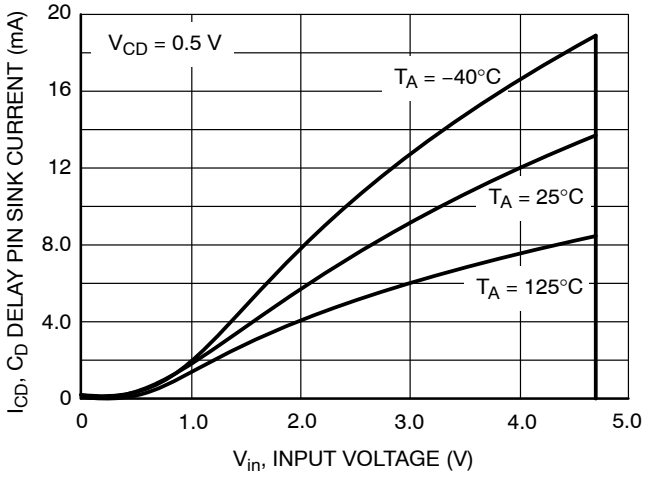


Figure 23. NCP302/3 Series 4.5 V C_D Delay Pin Sink Current vs. Input Voltage

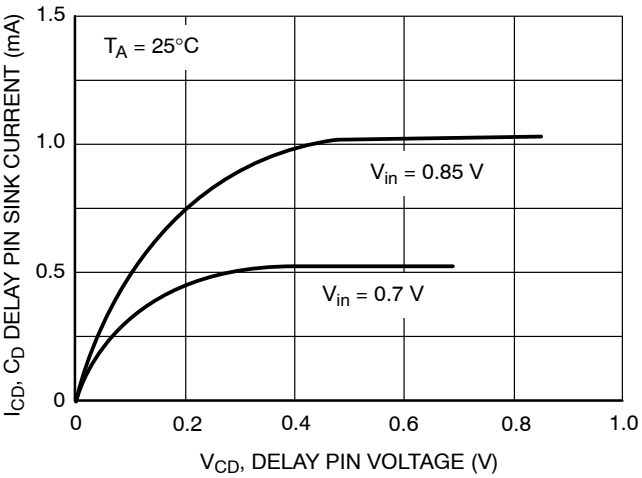


Figure 24. NCP302/3 Series 0.9 V C_D Delay Pin Sink Current vs. Voltage

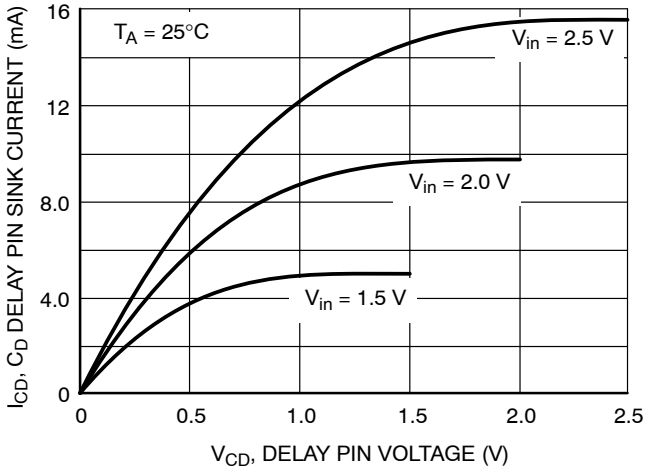


Figure 25. NCP302/3 Series 2.7 V C_D Delay Pin Sink Current vs. Voltage

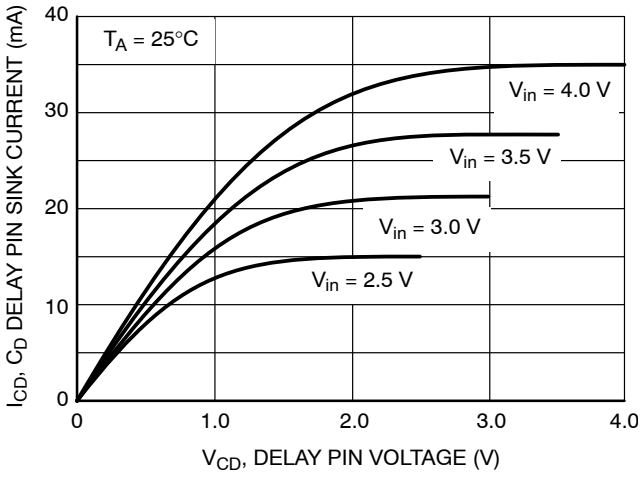


Figure 26. NCP302/3 Series 4.5 V C_D Delay Pin Sink Current vs. Voltage

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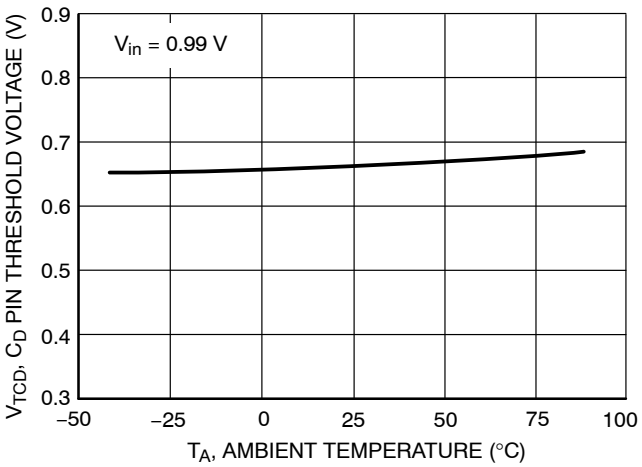


Figure 27. NCP302/3 Series 0.9 V C_D Delay Pin Threshold Voltage vs. Temperature

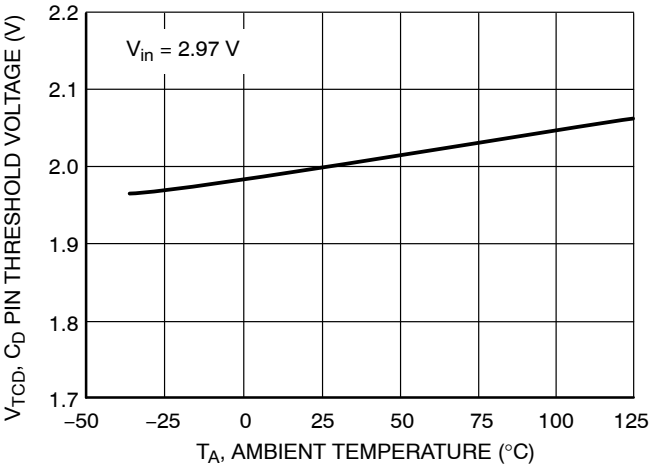


Figure 28. NCP302/3 Series 2.7 V C_D Delay Pin Threshold Voltage vs. Temperature

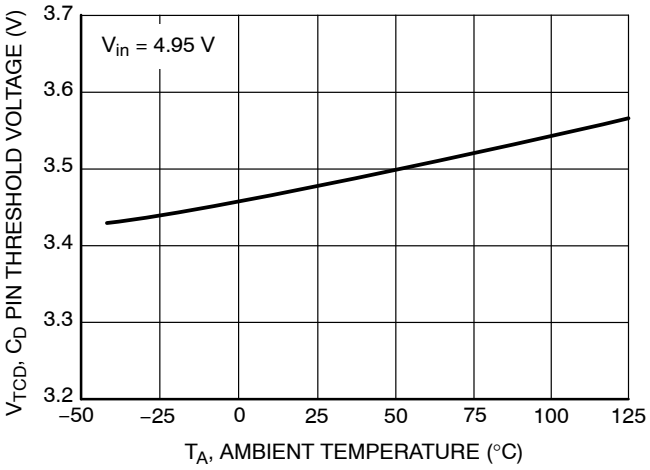


Figure 29. NCP302/3 Series 4.5 V C_D Delay Pin Threshold Voltage vs. Temperature

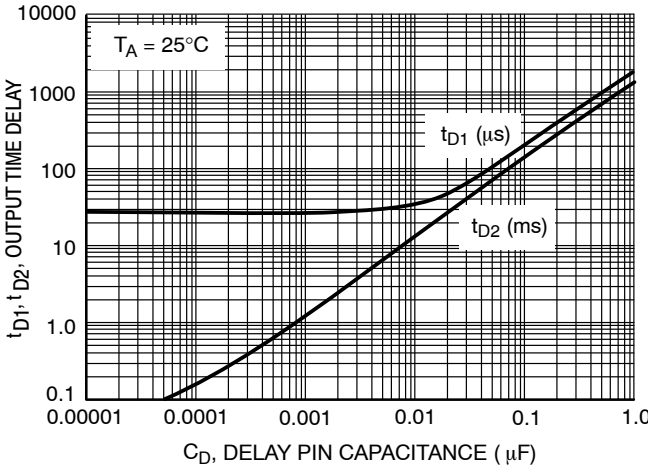


Figure 30. NCP302/3 Series 0.9 V Output Time Delay vs. Capacitance

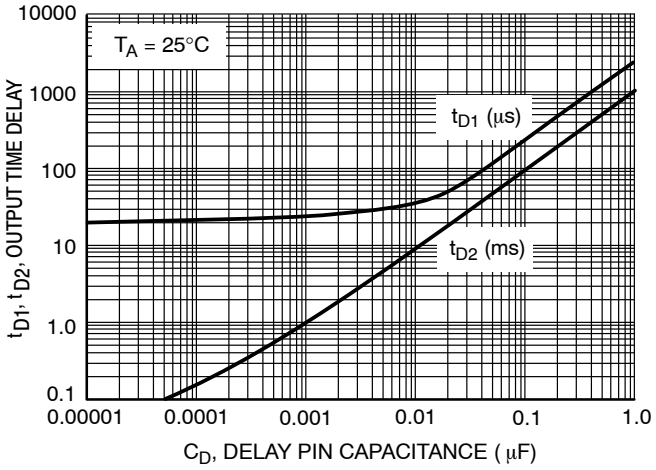


Figure 31. NCP302/3 Series 2.7 V Output Time Delay vs. Capacitance

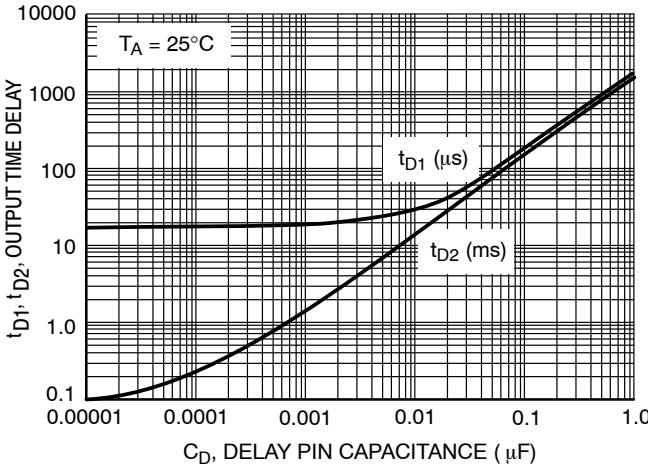


Figure 32. NCP302/3 Series 4.5 V Output Time Delay vs. Capacitance

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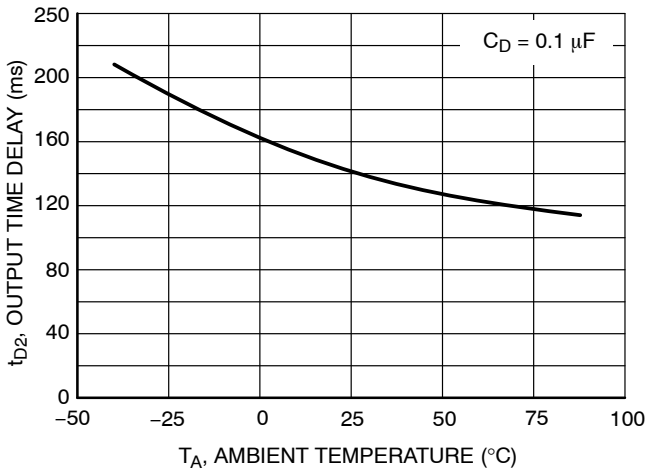


Figure 33. NCP302/3 Series 0.9 V Reset Output Time Delay vs. Temperature

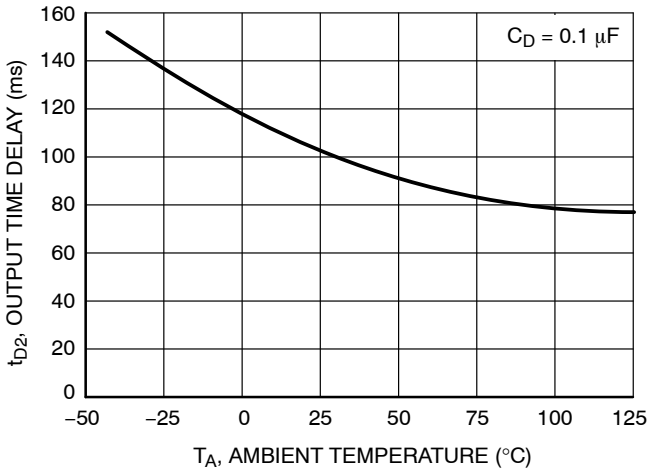


Figure 34. NCP302/3 Series 2.7 V Reset Output Time Delay vs. Temperature

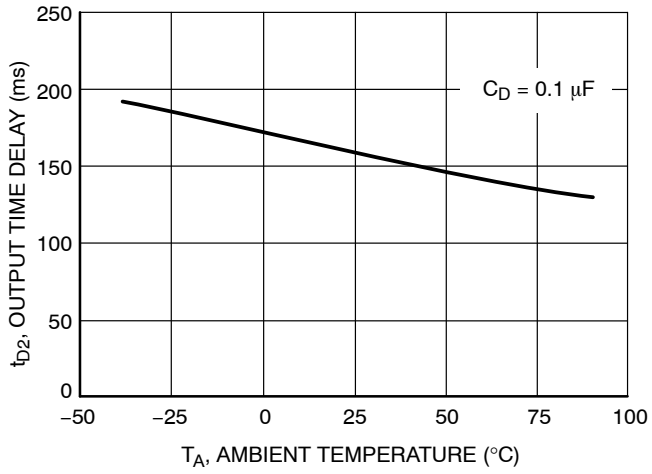


Figure 35. NCP302/3 Series 4.5 V Reset Output Time Delay vs. Temperature

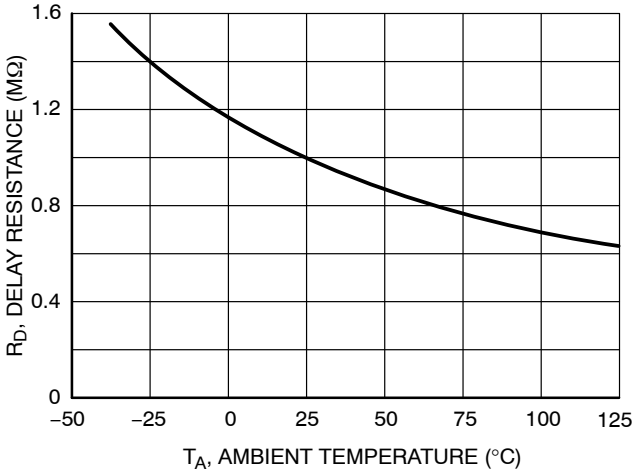


Figure 36. NCP302/3 Series Delay Resistance vs. Temperature

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OPERATING DESCRIPTION

The NCP302 and NCP303 series devices consist of a precision voltage detector that drives a time delay generator. Figures 37 and 38 show a timing diagram and a typical application. Initially consider that input voltage V_{in} is at a nominal level and it is greater than the voltage detector upper threshold (V_{DET+}). The voltage at Pin 5 and capacitor C_D will be at the same level as V_{in}, and the reset output (Pin 1) will be in the high state for active low devices, or in the low state for active high devices. If there is a power interruption and V_{in} becomes significantly deficient, it will fall below the lower detector threshold (V_{DET-}) and the external time delay capacitor C_D will be immediately discharged by an internal N−Channel MOSFET that connects to Pin 5. This sequence of events causes the Reset output to be in the low state for active low devices, or in the high state for active high devices. After completion of the power interruption, V_{in} will again return to its nominal level and become greater than the V_{DET+}. The voltage detector will turn off the N−Channel MOSFET and allow pullup resistor R_D to charge external capacitor C_D, thus creating a programmable delay for releasing the reset signal. When the voltage at Pin 5 exceeds the inverter/buffer threshold, typically 0.675 V_{in}, the reset output will revert back to its original state. The reset output time delay versus capacitance is shown in Figures 30 through 32. The voltage detector and inverter/buffer have built−in hysteresis to prevent erratic reset operation.

Although these device series are specifically designed for use as reset controllers in portable microprocessor based systems, they offer a cost−effective solution in numerous applications where precise voltage monitoring and time delay are required. Figures 38 through 46 show various application examples.

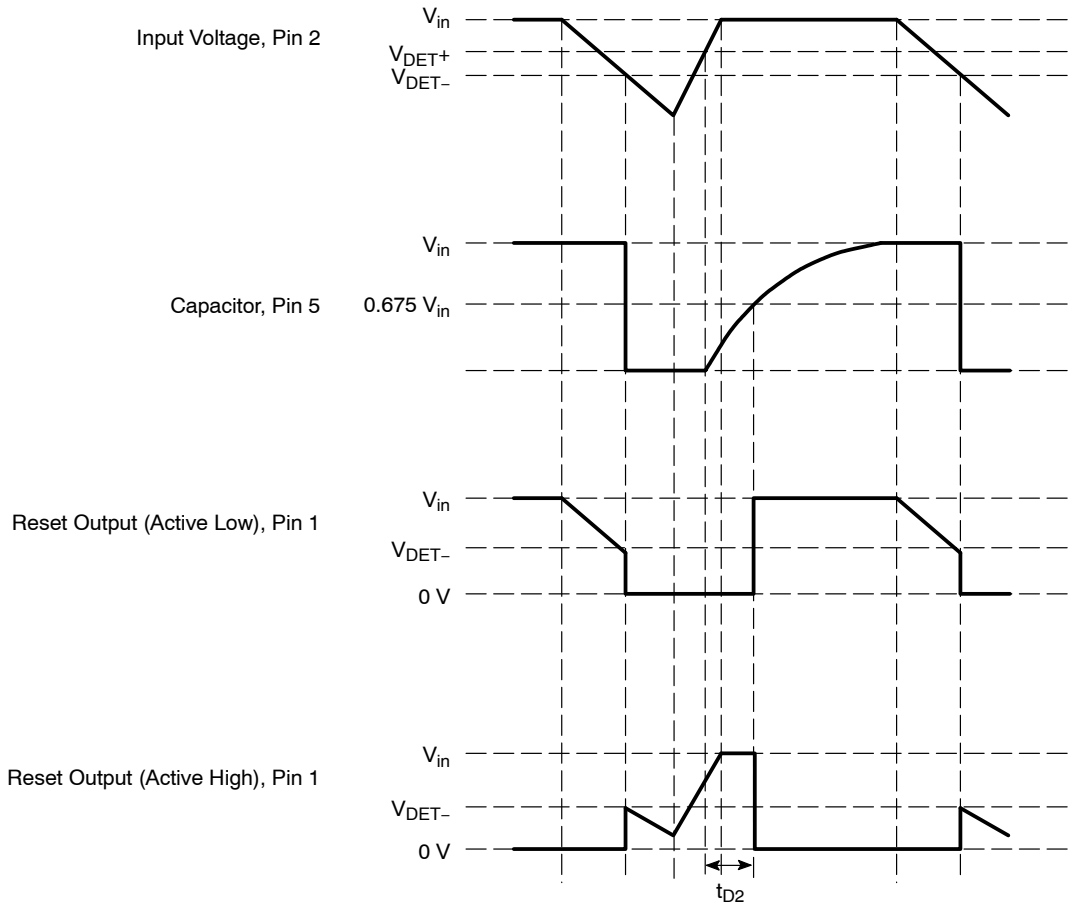


Figure 37. Timing Waveforms

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APPLICATION CIRCUIT INFORMATION

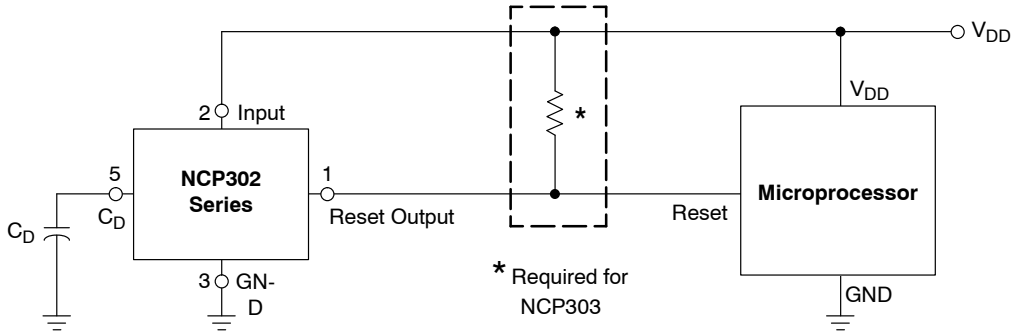


Figure 38. Microprocessor Reset Circuit

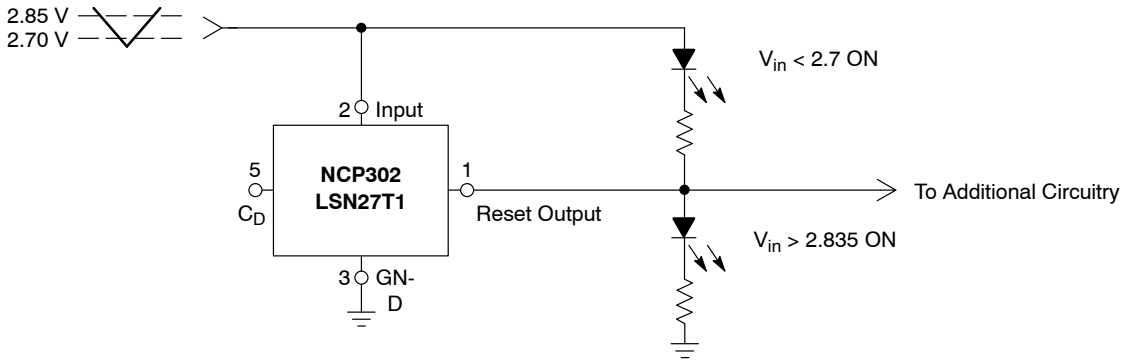


Figure 39. Battery Charge Indicator

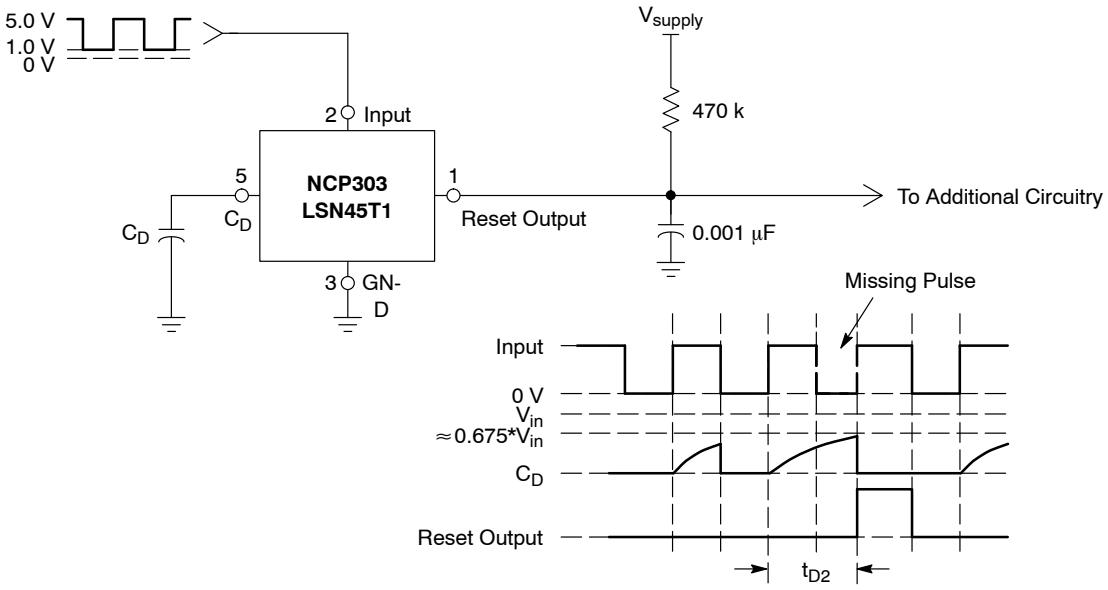


Figure 40. Missing Pulse Detector or Frequency Detector

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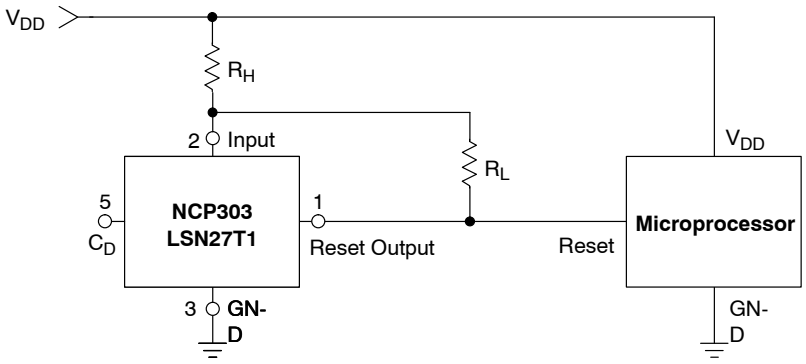


Figure 41. Microprocessor Reset Circuit with Additional Hysteresis

Comparator hysteresis can be increased with the addition of resistor R_H. The hysteresis equations have been simplified and do not account for the change of input current I_{in} as V_{in} crosses the comparator threshold. The internal resistance, R_{in} is simply calculated using I_{in} = 0.26 μA at 2.6 V.

V_{in} Decreasing:

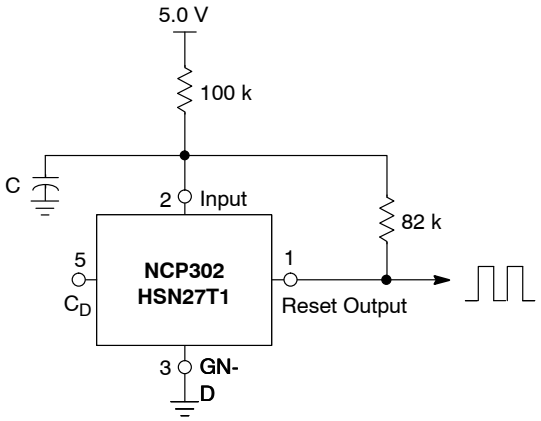
$$V_{th} = \left(\frac{R_H}{R_{in}} + 1\right)(V_{DET-})$$

V_{in} Increasing:

$$V_{th} = \left(\frac{R_H}{R_{in} \parallel R_L} + 1\right)(V_{DET-} + V_{HYS})$$

$V_{HYS} = V_{in}$ Increasing $- V_{in}$ Decreasing

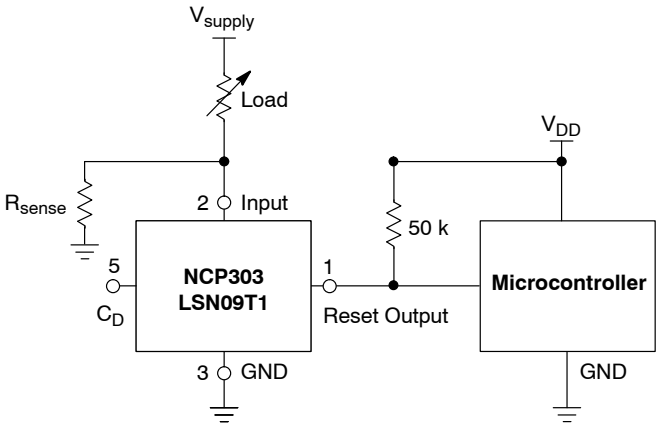
Test Data				
V_{th} Decreasing (V)	V_{th} Increasing (V)	V_{HYS} (V)	R_H (Ω)	R_L (kΩ)
2.70	2.84	0.135	0	–
2.70	2.87	0.17	100	10
2.70	2.88	0.19	100	6.8
2.70	2.91	0.21	100	4.3
2.70	2.90	0.20	220	10
2.70	2.94	0.24	220	6.8
2.70	2.98	0.28	220	4.3
2.70	2.70	0.27	470	10
2.70	3.04	0.34	470	6.8
2.70	3.15	0.35	470	4.3



Test Data		
C (μF)	f_{OSC} (kHz)	I_Q (μA)
0.01	2590	21.77
0.1	490	21.97
1.0	52	22.07

Figure 42. Simple Clock Oscillator

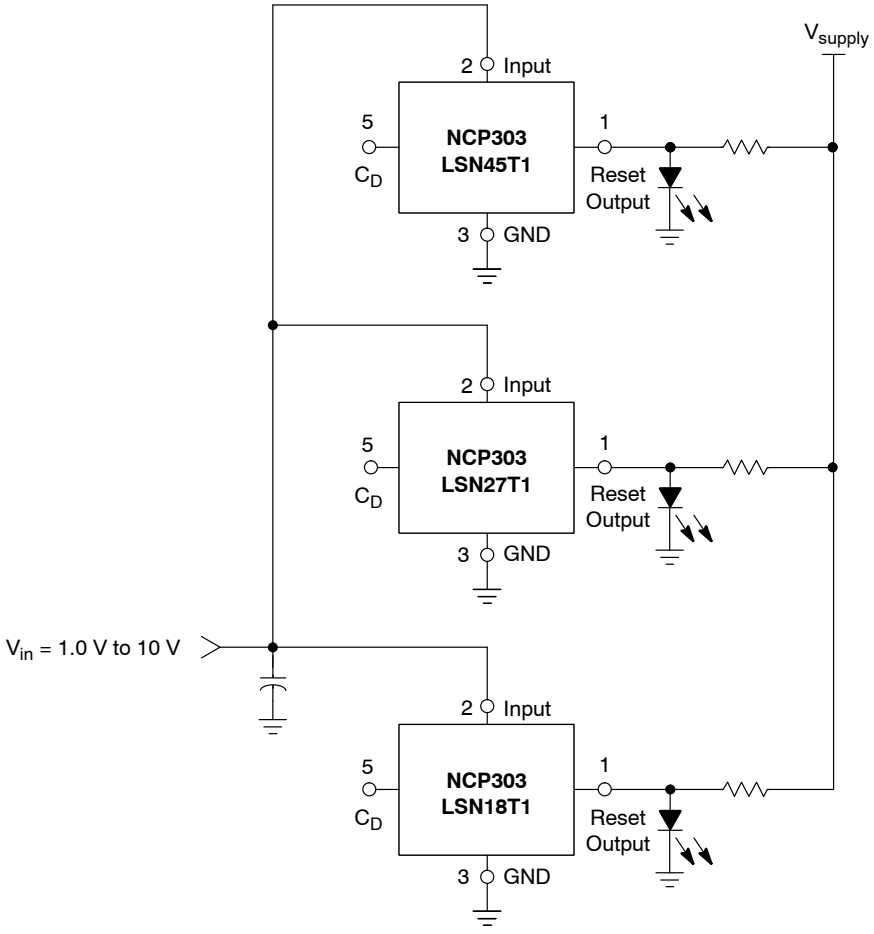
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This circuit monitors the current at the load. As current flows through the load, a voltage drop with respect to ground appears across R_{sense} where $V_{sense} = I_{load} * R_{sense}$. The following conditions apply:

If:	Then:
$I_{Load} < V_{DET-}/R_{sense}$	Reset Output = 0 V
$I_{Load} \geq (V_{DET-}+V_{HYS})/R_{sense}$	Reset Output = V_{DD}

Figure 43. Microcontroller Systems Load Sensing



A simple voltage monitor can be constructed by connecting several voltage detectors as shown above. Each LED will sequentially turn on when the respective voltage detector threshold (V_{DET-} +V_{HYS}) is exceeded. Note that detector thresholds (V_{DET-}) that range from 0.9 V to 4.9 V in 100 mV steps can be manufactured.

Figure 44. LED Bar Graph Voltage Monitor

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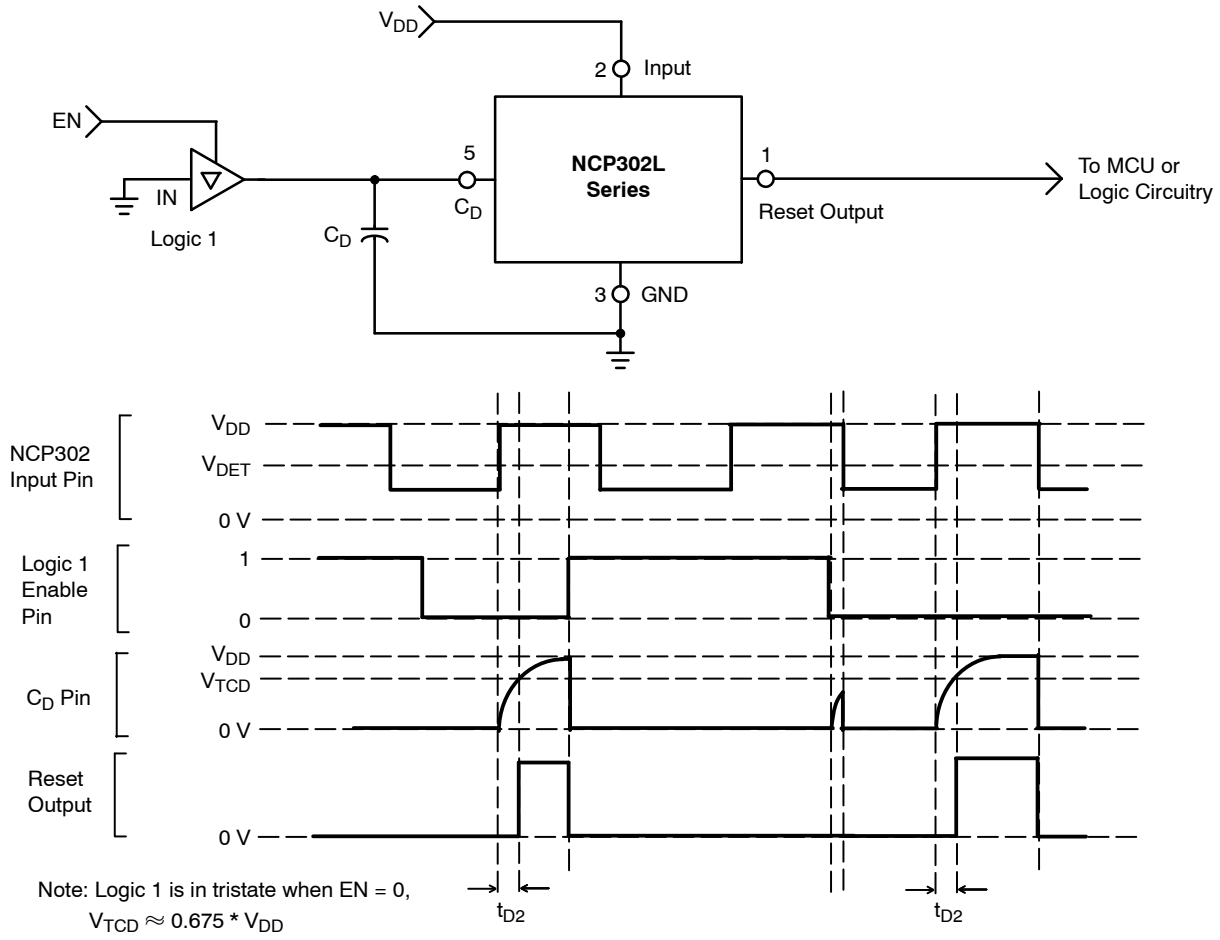


Figure 45. Undervoltage Detection with Independent Reset Signal Control

This circuit monitors V_{DD} for undervoltage. If the V_{DD} input falls below the detector threshold (V_{DET-}), then the capacitor on the C_D pin will be immediately discharged resulting in the reset output changing to its active state indicating that an undervoltage event has been detected. The addition of a logic gate (Logic 1) provides for reset output control which is independent of V_{DD}. If the output of the logic gate is tristated the undervoltage detector will behave normally. If the tristate is de−asserted, the logic gate will pull the C_D pin low resulting in the Reset Output pin changing to an active state. This independent control is useful in power supply sequencing applications when the Reset Output is tied to the enable input of an LDO or DC−DC converter.

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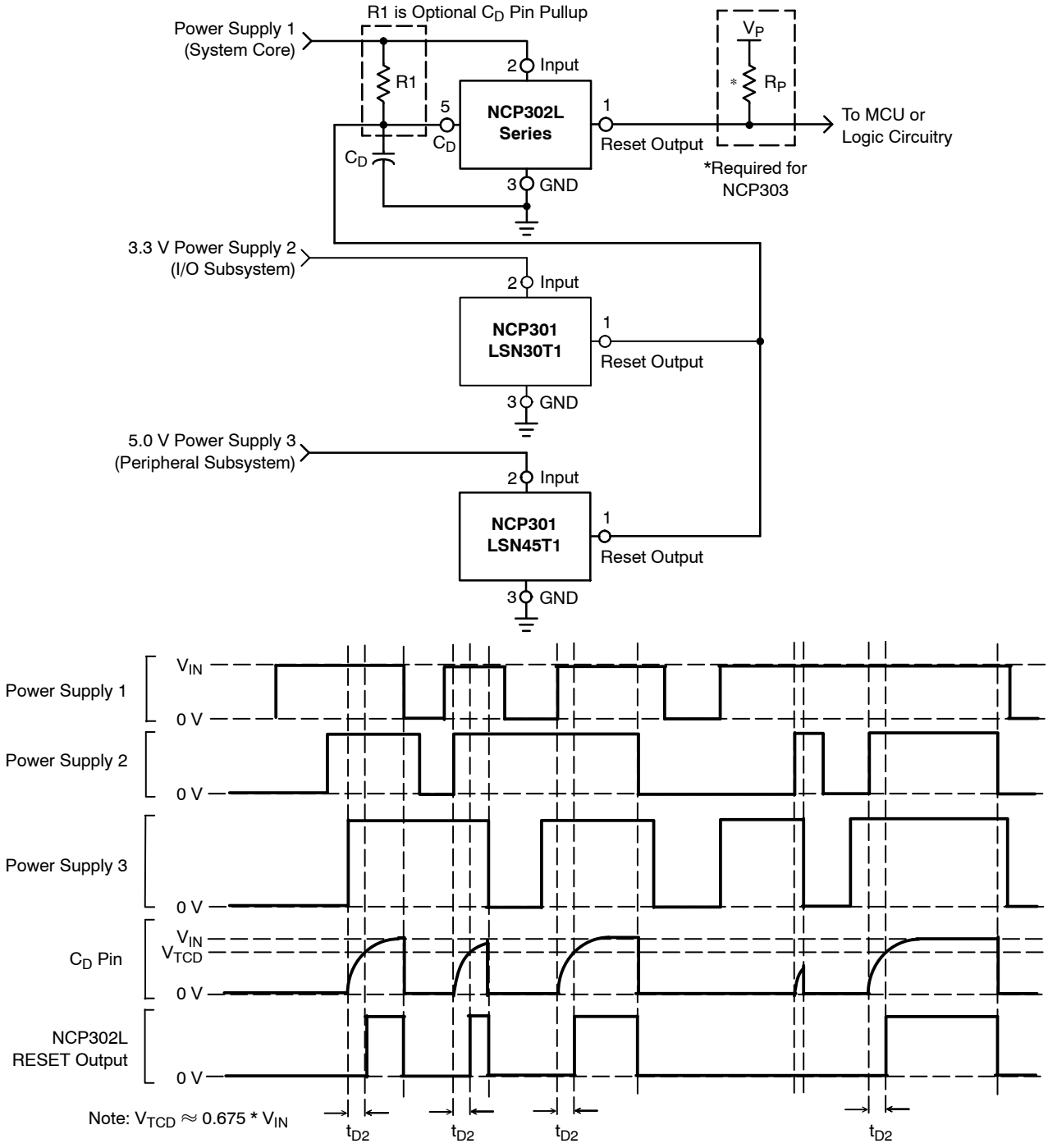


Figure 46. Multi−Rail Supply Undervoltage Monitor with Power Good

This circuit monitors multiple power supply rails for undervoltage conditions. If any of the three power supplies are in an undervoltage condition, the NCP302 reset output will be immediately set to an active low level. All three power supplies must be above their minimum voltage levels for the NCP302 reset output to generate a “Power Good” level (Reset Output = Power Supply 1 or V_P).

Optionally, R1 may be added to provide a smaller effective C_D pin pullup resistance, (R_D’), where $R_D' = R1 \parallel R_D$, with R_D (internal C_D pin pullup resistance) approximately equal to 1.0 MΩ, and R1 > 5 kΩ. If R1 << R_D, then R1 also can decrease the reset output delay time (t_{D2}) variance over the operating temperature range.

The Power Good signal time delay (t_{D2}) can be estimated by: $t_{D2} \approx R_D * C_D$, with R_D in Ohms, and C_D in Farads. If R1 is installed, then R_D’ is substituted for R_D. R_P is added only if using the NCP303 to replace the NCP302. This allows the Reset Output to be pulled up to V_P, which can be the Power Supply 1 or an independent power supply rail.

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ORDERING INFORMATION

Device	Threshold Voltage	Output Type	Reset	Marking	Package	Shipping†
NCV303LSN09T1G*	0.9	Open Drain	Active Low	AMU	TSOP−5 (Pb−Free)	3000 / Tape & Reel (7 inch Reel)
NCV303LSN10T1G*	1.0			SSM		
NCV303LSN11T1G*	1.1			ADC		
NCV303LSN16T1G*	1.6			SRV		
NCV303LSN20T1G*	2.0			SRW		
NCV303LSN24T1G*	2.4			SRY		
NCV303LSN25T1G*	2.5			AHA		
NCV303LSN27T1G*	2.7			CAP		
NCV303LSN29T1G*	2.9			SSK		
NCV303LSN30T1G*	3.0			SSA		
NCV303LSN31T1G*	3.1			CAR		
NCV303LSN34T1G*	3.4			CAT		
NCV303LSN40T1G*	4.0			SSD		
NCV303LSN42T1G*	4.2			SSE		
NCV303LSN44T1G*	4.4			SSF		
NCV303LSN45T1G*	4.5			SSG		
NCV303LSN46T1G*	4.6			SSH		

NOTE: The ordering information lists standard undervoltage thresholds with active low outputs. Additional active low threshold devices, ranging from 0.9 V to 4.9 V in 100 mV increments and NCP302 active high output devices, ranging from 0.9 V to 4.9 V in 100 mV increments can be manufactured. Contact your **onsemi** representative for availability. The electrical characteristics of these additional devices are shown in Tables 1 and 2.

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.
NCVxxx: T_{low} = −40°C, T_{high} = +125°C. Guaranteed by design.

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DISCONTINUED (Note 21)

Device	Threshold Voltage	Output Type	Reset	Marking	Package	Shipping†
NCP302LSN09T1G	0.9	CMOS	Active Low	SBO	TSOP−5 (Pb−Free)	3000 / Tape & Reel (7 inch Reel)
NCP302LSN15T1G	1.5			SBI		
NCP302LSN18T1G	1.8			SBF		
NCP302LSN20T1G	2.0			SBD		
NCV302LSN20T1G*	2.0			AHH		
NCP302LSN27T1G	2.7			SAW		
NCP302LSN28T1G	2.8			ALA		
NCP302LSN30T1G	3.0			SAT		
NCV302LSN30T1G*	3.0			ACJ		
NCP302LSN33T1G	3.3			SAQ		
NCP302LSN38T1G	3.8			SAK		
NCP302LSN40T1G	4.0			SAI		
NCP302LSN43T1G	4.3			SAF		
NCP302LSN45T1G	4.5			SAL		
NCP302LSN47T1G	4.7			SAC		
NCP302HSN09T1G	0.9		Active High	SDO		
NCP302HSN18T1G	1.8			SFH		
NCP302HSN27T1G	2.7			SDK		
NCP302HSN30T1G	3.0			SDI		
NCP302HSN40T1G	4.0			SJH		
NCP302HSN45T1G	4.5			SDG		
NCP303LSN09T1G	0.9	Open Drain	Active Low	SDE		
NCP303LSN10T1G	1.0			SDD		
NCP303LSN11T1G	1.1			SDC		
NCV303LSN12T1G*	1.2			SDB		
NCP303LSN13T1G	1.3			SDA		
NCV303LSN13T1G*	1.3			SRS		
NCP303LSN14T1G	1.4			SCZ		
NCV303LSN14T1G*	1.4			SRT		
NCP303LSN15T1G	1.5			SCY		
NCV303LSN15T1G*	1.5			SRU		
NCP303LSN16T1G	1.6			SCX		
NCP303LSN17T1G	1.7			SCW	TSOP−5	
NCP303LSN18T1G	1.8			SCV	TSOP−5 (Pb−Free)	
NCP303LSN20T1G	2.0			SCT		
NCP303LSN22T1G	2.2			SCR		
NCV303LSN22T1G*	2.2			ADD		
NCP303LSN23T1G	2.3			SCQ		
NCV303LSN23T1G*	2.3			SRX		
NCP303LSN24T1G	2.4			SCP		

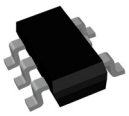
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DISCONTINUED (Note 21) (continued)

Device	Threshold Voltage	Output Type	Reset	Marking	Package	Shipping†
NCP303LSN25T1G	2.5	Open Drain	Active Low	SCO	TSOP−5 (Pb−Free)	3000 / Tape & Reel (7 inch Reel)
NCP303LSN26T1G	2.6			SCN		
NCP303LSN27T1G	2.7			SCM		
NCP303LSN28T1G	2.8			SCL		
NCV303LSN28T1G*	2.8			TAA		
NCP303LSN29T1G	2.9			SCK		
NCP303LSN30T1G	3.0			SCJ		
NCP303LSN31T1G	3.1			SCI		
NCP303LSN32T1G	3.2			SCH		
NCP303LSN33T1G	3.3			SCG		
NCP303LSN34T1G	3.4			SCF		
NCP303LSN36T1G	3.6			SCD		
NCV303LSN36T1G*	3.6			SSC		
NCP303LSN38T1G	3.8			SCA		
NCP303LSN40T1G	4.0			SBY		
NCP303LSN42T1G	4.2			SBW		
NCV303LSN43T1G*	4.3			SBV		
NCP303LSN44T1G	4.4			SBU		
NCV303LSN44T1*	4.4			SSF	TSOP−5	
NCP303LSN45T1G	4.5			SBT	TSOP−5 (Pb−Free)	
NCP303LSN46T1G	4.6			SBS		
NCV303LSN46T1*	4.6			SSH	TSOP−5	
NCP303LSN47T1G	4.7			SBR	TSOP−5 (Pb−Free)	
NCV303LSN47T1*	4.7			SSJ	TSOP−5	
NCV303LSN47T1G*	4.7			SSJ	TSOP−5 (Pb−Free)	
NCP303LSN49T1G	4.9			SBP		
NCV303LSN49T1*	4.9			SSI	TSOP−5	
NCV303LSN49T1G*	4.9			SSI	TSOP−5 (Pb−Free)	

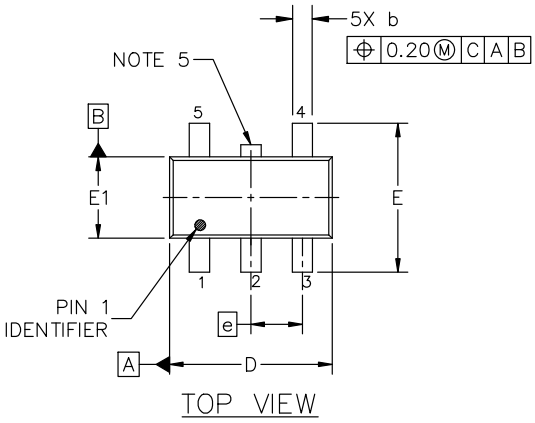
21. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

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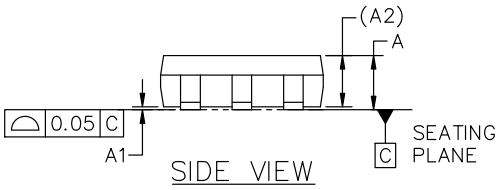


TSOP−5 3.00x1.50x0.95, 0.95P
CASE 483
ISSUE P

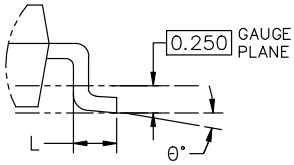
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TOP VIEW



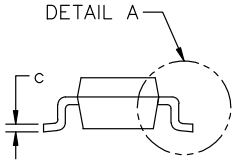
SIDE VIEW



DETAIL "A"
SCALE 2:1

NOTES:

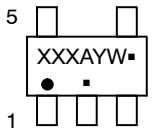
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS (ANGLES IN DEGREES).
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OF GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.



END VIEW

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.900	1.000	1.100
A1	0.010	0.055	0.100
A2		0.950 REF.	
b	0.250	0.375	0.500
c	0.100	0.180	0.260
D	2.850	3.000	3.150
E	2.500	2.750	3.000
E1	1.350	1.500	1.650
e		0.950 BSC	
L	0.200	0.400	0.600
θ	0°	5°	10°

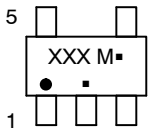
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MARKING DIAGRAM*



Analog

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

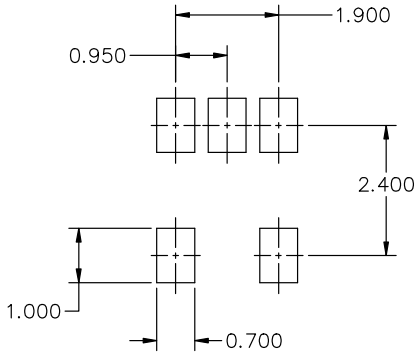
(Note: Microdot may be in either location)



Discrete/Logic

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



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