MOSFET – Power, Single, P-Channel, SC-70

-20 V, -1.37 A

NTS4101P

$V_{(BR)DSS}$	$R_{DS(on)}$ Typ	I_D Max
−20 V	83 mΩ @ −4.5 V	−1.37 A
	88 mΩ @ −3.6 V	
	104 mΩ @ −2.5 V	

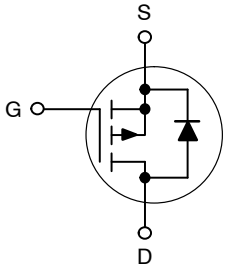
Features

- Leading −20 V Trench for Low $R_{DS(on)}$
- −2.5 V Rated for Low Voltage Gate Drive
- SC-70 Surface Mount for Small Footprint (2x2 mm)
- Pb-Free Package is Available

Applications

- High Side Load Switch
- Charging Circuit
- Single Cell Battery Applications such as: Cell Phones, Digital Cameras, PDAs

P-Channel MOSFET



MAXIMUM RATINGS (T_J = 25 °C unless otherwise stated)

Parameter			Symbol	Value	Units
Drain-to-Source Voltage			V_{DSS}	−20	V
Gate-to-Source Voltage			V_{GS}	±8	V
Continuous Drain Current (Note 1)	Steady State	T_A = 25 °C	I_D	−1.37	A
		T_A = 70 °C		−0.62	
Power Dissipation (Note 1)	Steady State	T_A = 25 °C	P_D	0.329	W
Pulsed Drain Current	t_p = 10 μs		I_{DM}	−4.0	A
Operating Junction and Storage Temperature			T_J, T_{STG}	−55 to 150	°C
Source Current (Body Diode), Continuous			I_S	−0.5	A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	°C

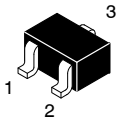
THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Units
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	380	°C/W

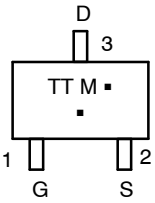
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).

MARKING DIAGRAM & PIN ASSIGNMENT



SC-70 (SOT-323)
CASE 419
STYLE 8



TT = Device Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location)

* Date Code orientation may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
NTS4101PT1G	SOT-323 (Pb-Free)	3000/Tape & Reel

DISCONTINUED (Note 1)

NTS4101PT1	SOT-323	3000/Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

1. **DISCONTINUED:** This device is not available. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.

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ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise stated)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = −250 μA		−20	−24.5		V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				−13.7		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = −16 V	T_J = 25 °C			−1.0	μA
			T_J = 70 °C			−5.0	
Gate-to-Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±8 V				±100	nA
ON CHARACTERISTICS (Note 2)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = −250 μA		−0.45	−0.64	−1.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				2.7		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	V_{GS} = −4.5 V, I_D = −1.0 A			83	120	mΩ
		V_{GS} = −3.6 V, I_D = −0.7 A			88	130	
		V_{GS} = −2.5 V, I_D = −0.3 A			104	160	
Forward Transconductance	G_{FS}	V_{DS} = −5.0 V, I_D = −1.3 A			5.2		S
CHARGES AND CAPACITANCES							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = −20 V			603	840	pF
Output Capacitance	C_{OSS}				90	125	
Reverse Transfer Capacitance	C_{RSS}				62	85	
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = −4.5 V, V_{DS} = −4.5 V, I_D = −1.0 A			6.4	9.0	nC
Threshold Gate Charge	$Q_{G(TH)}$				0.7		
Gate-to-Source Charge	Q_{GS}				1.0		
Gate-to-Drain Charge	Q_{GD}				1.5		
SWITCHING CHARACTERISTICS (Note 3)							
Turn-On Delay Time	$t_{d(ON)}$	V_{GS} = −4.5 V, V_{DD} = −4.0 V, I_D = −1.0 A, R_G = 6.2 Ω			6.2	12	ns
Rise Time	t_r				14.9	25	
Turn-Off Delay Time	$t_{d(OFF)}$				26	40	
Fall Time	t_f				18	30	
DRAIN-SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = −0.3 A	T_J = 25 °C		−0.61	−1.2	V
			T_J = 125 °C		−0.5		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI_{SD}/dt = 100 A/μs, I_S = −1.0 A			10.9	20	ns
Charge Time	T_a				7.1		
Discharge Time	T_b				3.8		
Reverse Recovery Charge	Q_{RR}				4.25		nC

2. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperatures.

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TYPICAL CHARACTERISTICS

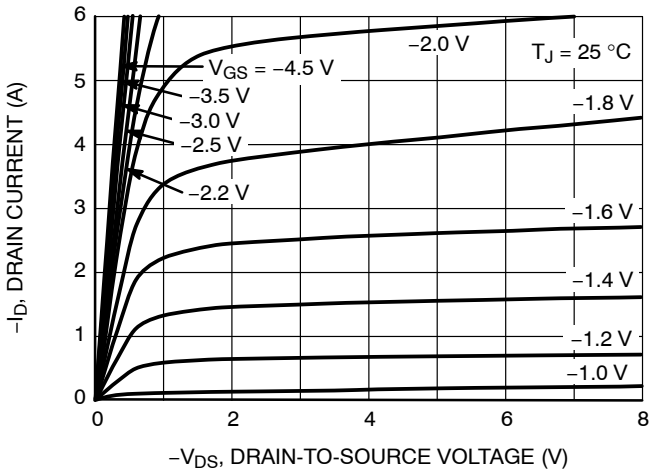


Figure 1. On-Region Characteristics

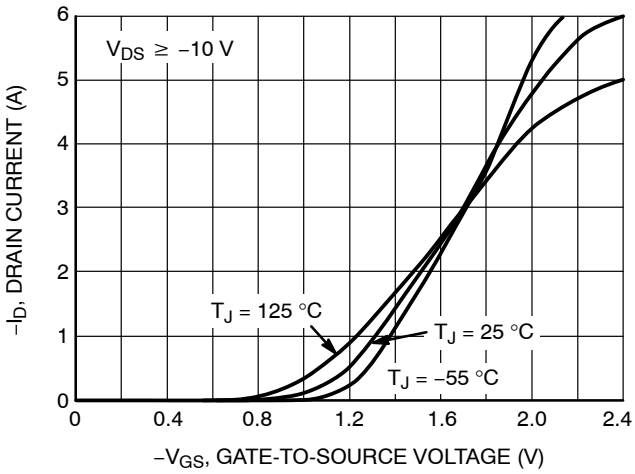


Figure 2. Transfer Characteristics

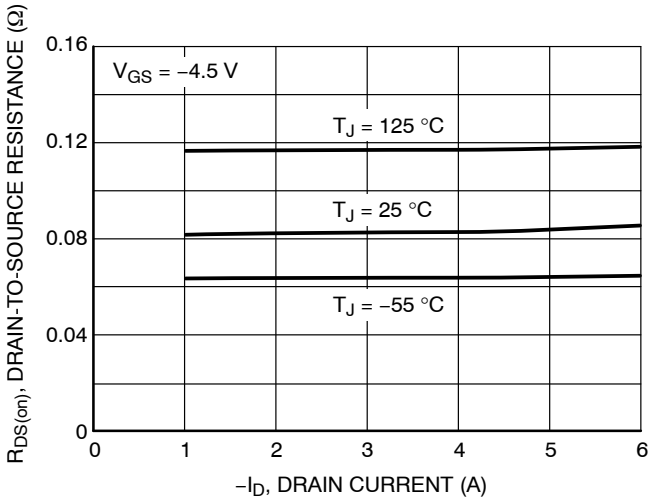


Figure 3. On-Resistance versus Drain Current and Temperature

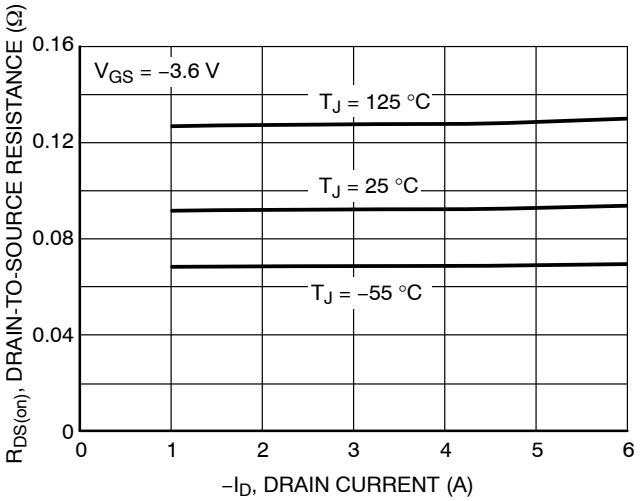


Figure 4. On-Resistance versus Drain Current and Temperature

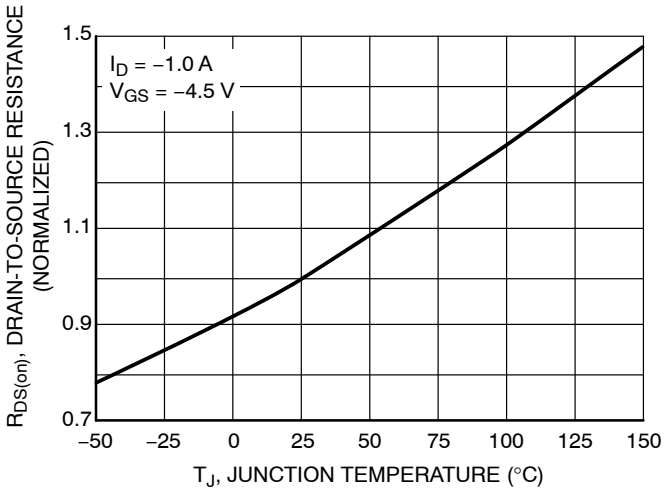


Figure 5. On-Resistance Variation with Temperature

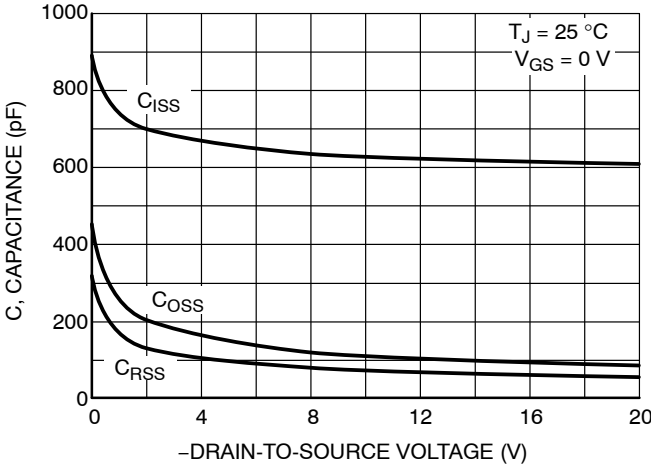


Figure 6. Capacitance Variation

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TYPICAL CHARACTERISTICS

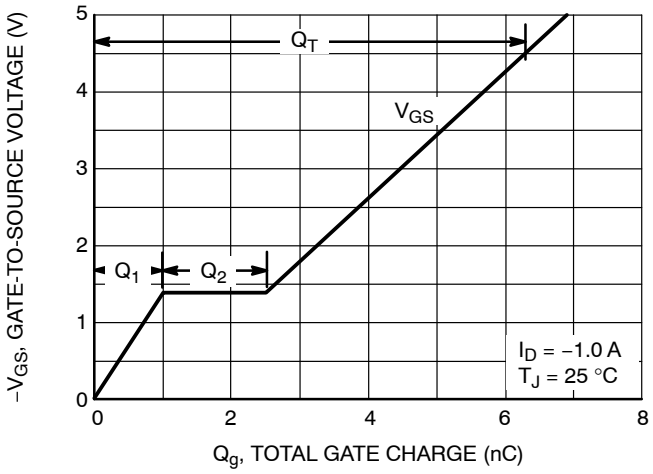


Figure 7. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

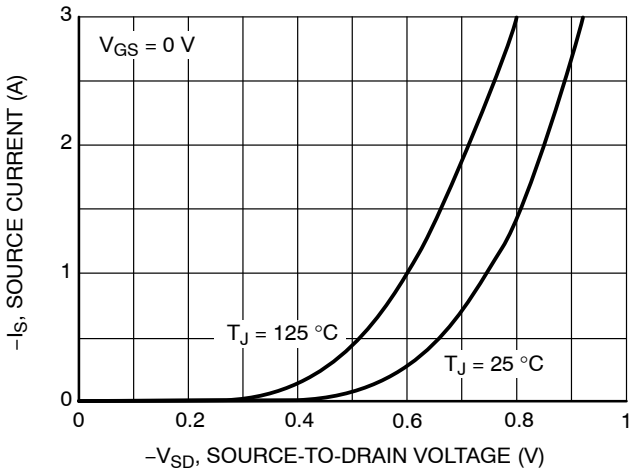


Figure 8. Diode Forward Voltage versus Current

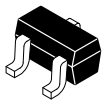
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REVISION HISTORY

Revision	Description of Changes	Date
4	Document rebranded to **onsemi** format. OPN NTS4101PT1 marked as discontinued.	1/29/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

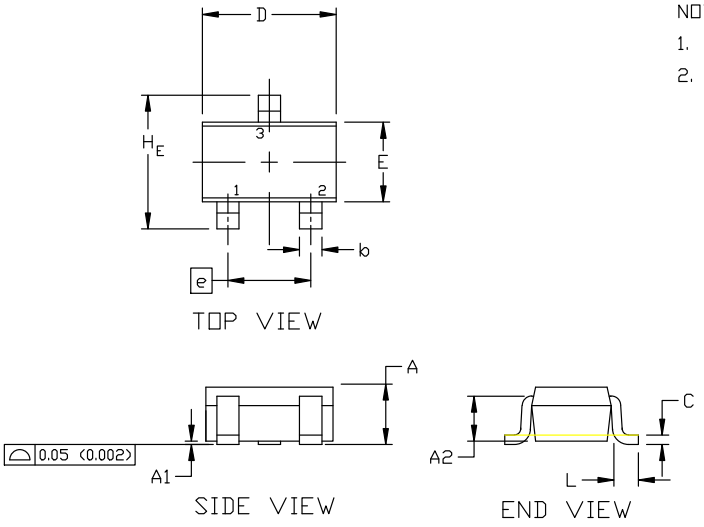
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SCALE 4:1

SC−70 (SOT−323)
CASE 419
ISSUE R

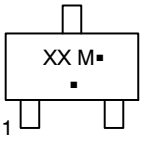
DATE 11 OCT 2022



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH

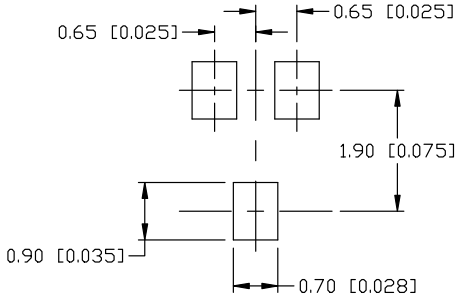
	MILLIMETERS			INCHES		
DIM	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.032	0.035	0.040
A1	0.00	0.05	0.10	0.000	0.002	0.004
A2	0.70 REF			0.028 BSC		
b	0.30	0.35	0.40	0.012	0.014	0.016
c	0.10	0.18	0.25	0.004	0.007	0.010
D	1.80	2.00	2.20	0.071	0.080	0.087
E	1.15	1.24	1.35	0.045	0.049	0.053
e	1.20	1.30	1.40	0.047	0.051	0.055
e1	0.65 BSC			0.026 BSC		
L	0.20	0.38	0.56	0.008	0.015	0.022
H_E	2.00	2.10	2.40	0.079	0.083	0.095

GENERIC MARKING DIAGRAM



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



* For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

SOLDERING FOOTPRINT

STYLE 1:
CANCELLED

STYLE 2:
PIN 1. ANODE
2. N.C.
3. CATHODE

STYLE 3:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 6:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 7:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 8:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. ANODE−CATHODE

STYLE 11:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

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DESCRIPTION:	**SC−70 (SOT−323)**	**PAGE 1 OF 1**

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