MMJT9435

Preferred Device

Bipolar Power Transistors

PNP Silicon

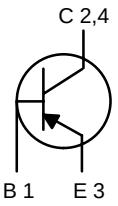
Features

- Pb−Free Packages are Available
- Collector −Emitter Sustaining Voltage −
  $V_{CEO(sus)}$ = 30 Vdc (Min) @ I_C = 10 mAdc
- High DC Current Gain −
  h_{FE} = 125 (Min) @ I_C = 0.8 Adc
  = 90 (Min) @ I_C = 3.0 Adc
- Low Collector −Emitter Saturation Voltage −
  $V_{CE(sat)}$ = 0.275 Vdc (Max) @ I_C = 1.2 Adc
  = 0.55 Vdc (Max) @ I_C = 3.0 Adc
- SOT−223 Surface Mount Packaging
- Epoxy Meets UL 94, V−0 @ 0.125 in
- ESD Ratings: Human Body Model, 3B; > 8000 V
  Machine Model, C; > 400 V

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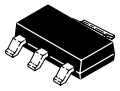
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POWER BJT
I_C = 3.0 AMPERES
BV_{CEO} = 30 VOLTS
$V_{CE(sat)}$ = 0.275 VOLTS

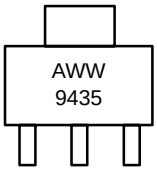


Schematic

MARKING DIAGRAM

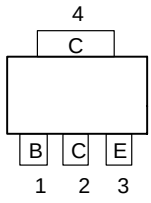


SOT−223
CASE 318E
STYLE 1



9435 = Specific Device Code
A = Assembly Location
WW = Work Week

PIN ASSIGNMENT



Top View Pinout

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

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MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	30	Vdc
Collector−Base Voltage	V_{CB}	45	Vdc
Emitter−Base Voltage	V_{EB}	6.0	Vdc
Base Current − Continuous	I_B	1.0	Adc
Collector Current − Continuous − Peak	I_C	3.0 5.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C Total P_D @ T_A = 25°C mounted on 1” sq. (645 sq. mm) Collector pad on FR−4 bd material Total P_D @ T_A = 25°C mounted on 0.012” sq. (7.6 sq. mm) Collector pad on FR−4 bd material	P_D	3.0 24 1.56 0.72	W mW/°C W
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case − Junction−to−Ambient on 1” sq. (645 sq. mm) Collector pad on FR−4 bd material − Junction−to−Ambient on 0.012” sq. (7.6 sq. mm) Collector pad on FR−4 bd material	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	42 80 174	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8” from case for 5 seconds	T_L	260	°C

ORDERING INFORMATION

Device	Package	Shipping†
MMJT9435T1	SOT−223	1000 / Tape & Reel
MMJT9435T1G	SOT−223 (Pb−Free)	1000 / Tape & Reel
MMJT9435T3	SOT−223	4000 / Tape & Reel
MMJT9435T3G	SOT−223 (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (I_C = 10 mAdc, I_B = 0 Adc)	$V_{CEO(sus)}$	30	–	–	Vdc
Emitter−Base Voltage (I_E = 50 μAdc, I_C = 0 Adc)	V_{EBO}	6.0	–	–	Vdc
Collector Cutoff Current (V_{CE} = 25 Vdc, R_{BE} = 200 Ω) (V_{CE} = 25 Vdc, R_{BE} = 200 Ω, T_J = 125°C)	I_{CER}	– –	– –	20 200	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc)	I_{EBO}	–	–	10	μAdc
ON CHARACTERISTICS (Note 1)					
Collector−Emitter Saturation Voltage (I_C = 0.8 Adc, I_B = 20 mAdc) (I_C = 1.2 Adc, I_B = 20 mAdc) (I_C = 3.0 Adc, I_B = 0.3 Adc)	$V_{CE(sat)}$	– – –	0.155 – –	0.210 0.275 0.550	Vdc
Base−Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.3 Adc)	$V_{BE(sat)}$	–	–	1.25	Vdc
Base−Emitter On Voltage (I_C = 1.2 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	–	–	1.10	Vdc
DC Current Gain (I_C = 0.8 Adc, V_{CE} = 1.0 Vdc) (I_C = 1.2 Adc, V_{CE} = 1.0 Vdc) (I_C = 3.0 Adc, V_{CE} = 1.0 Vdc)	h_{FE}	125 110 90	220 – –	– – –	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0 Adc, f = 1.0 MHz)	C_{ob}	–	100	150	pF
Input Capacitance (V_{EB} = 8.0 Vdc)	C_{ib}	–	135	–	pF
Current−Gain − Bandwidth Product (Note 2) (I_C = 500 mA, V_{CE} = 10 V, F_{test} = 1.0 MHz)	f_T	–	110	–	MHz

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. $f_T = |h_{FE}| \bullet f_{test}$

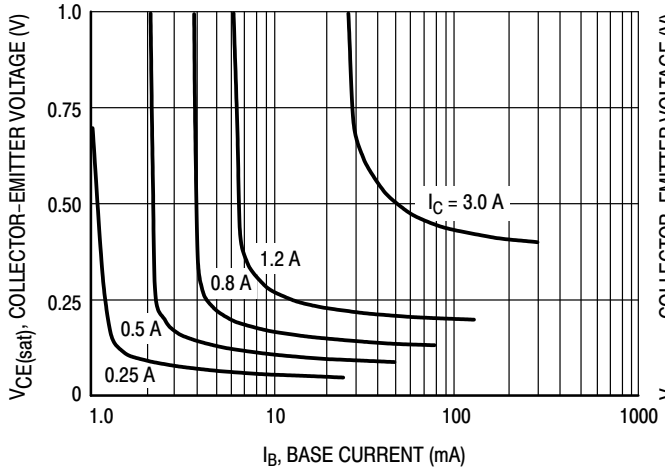


Figure 1. Collector Saturation Region

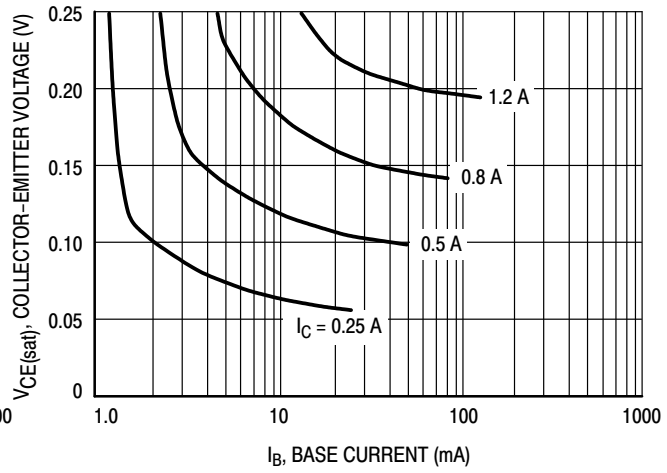


Figure 2. Collector Saturation Region

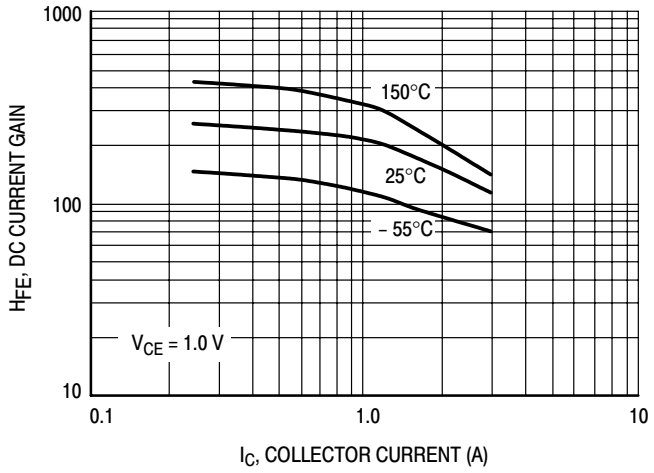


Figure 3. DC Current Gain

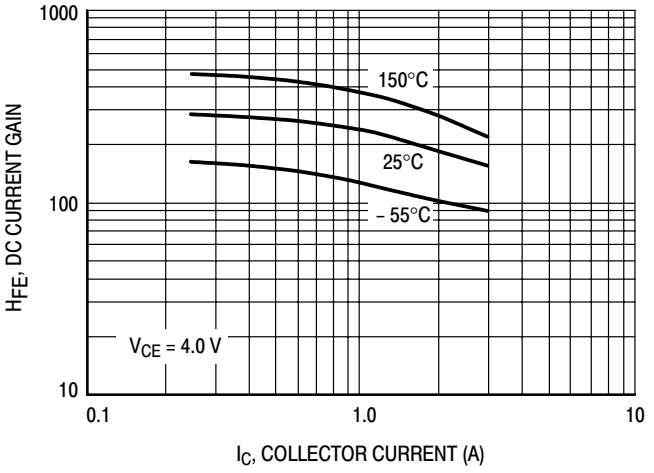


Figure 4. DC Current Gain

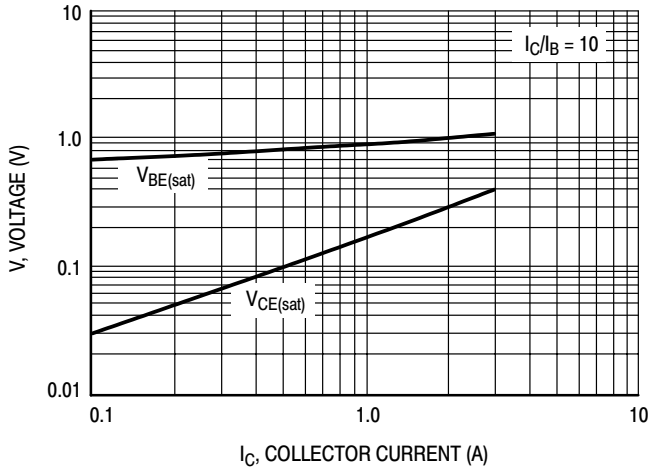


Figure 5. “On” Voltages

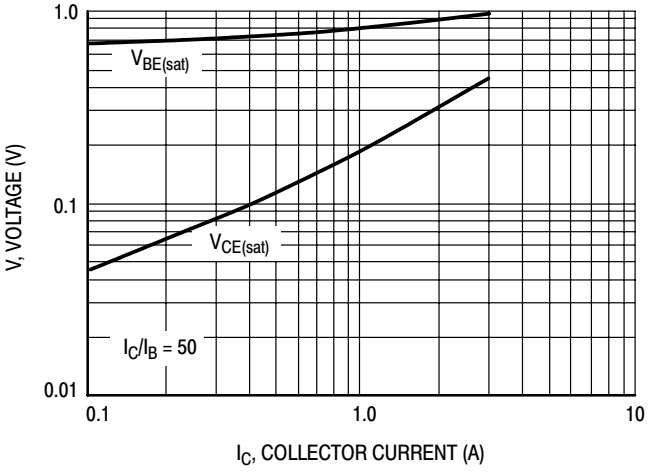


Figure 6. “On” Voltages

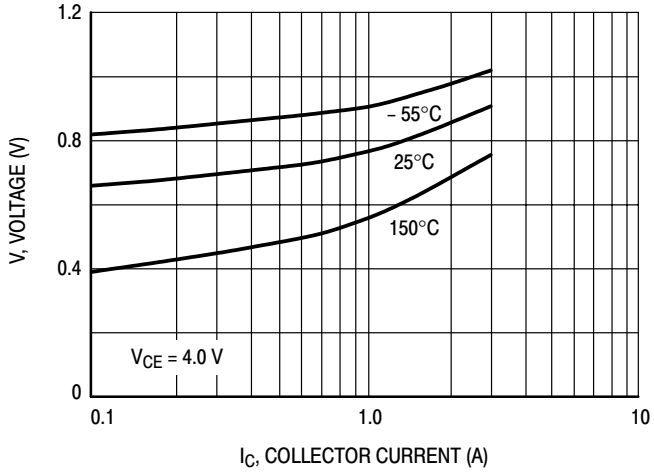


Figure 7. $V_{BE(on)}$ Voltage

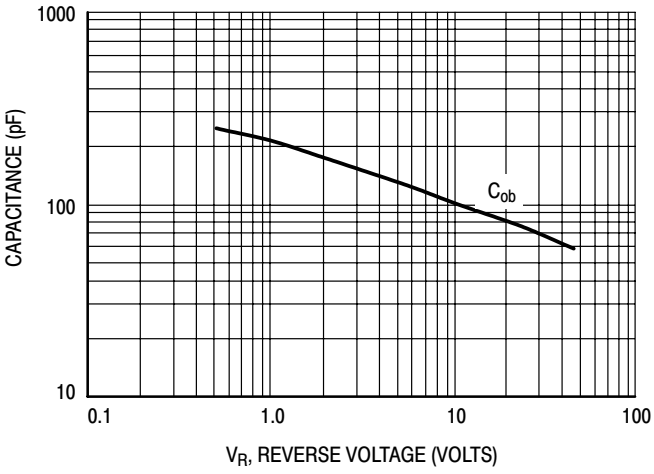


Figure 8. Output Capacitance

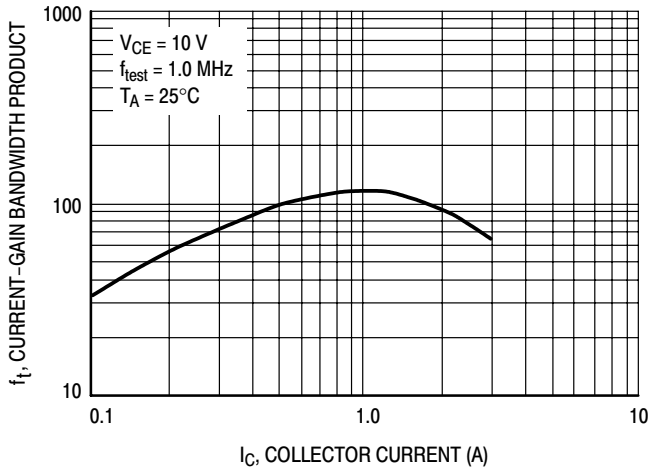


Figure 9. Current−Gain Bandwidth Product

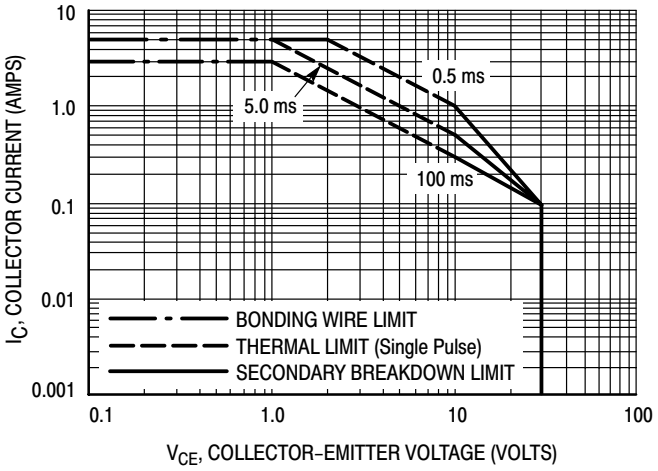


Figure 10. Active Region Safe Operating Area

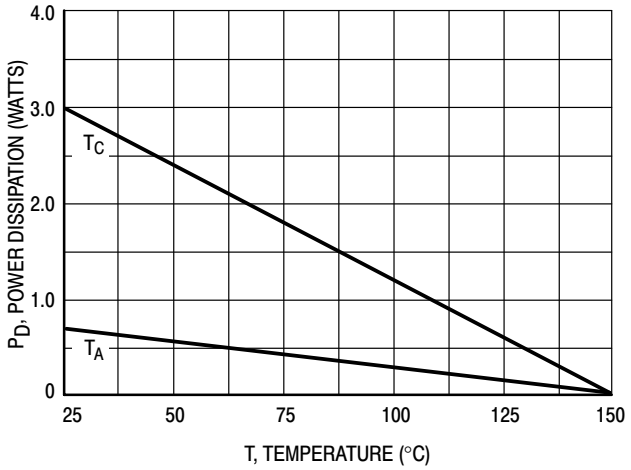


Figure 11. Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Secondary breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 12. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

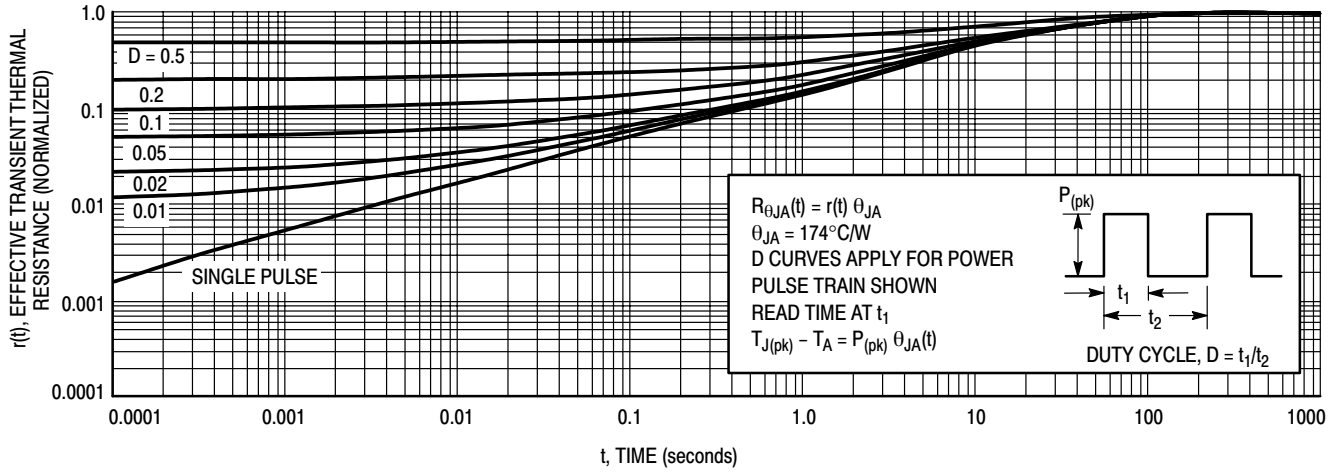


Figure 12. Thermal Response

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