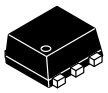
# Dual General Purpose Transistor

# NST857BDP6T5G

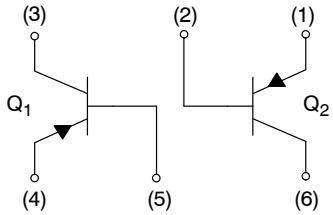


SOT−963
CASE 527AD

The NST857BDP6T5G device is a spin−off of our popular SOT−23/SOT−323/SOT−563 three−leaded device. It is designed for general purpose amplifier applications and is housed in the SOT−963 six−leaded surface mount package. By putting two discrete devices in one package, this device is ideal for low−power surface mount applications where board space is at a premium.

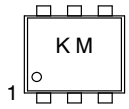
### Features

- $h_{FE}$, 220−475
- Low $V_{CE(sat)}$, ≤ 0.3 V
- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- This is a Pb−Free Device




NST857BDP6T5G

### MARKING DIAGRAM




K = Device Code
M = Date Code

### MAXIMUM RATINGS

| Symbol | Rating | Value | Unit |
|---|---|---|---|
| $V_{CEO}$ | Collector − Emitter Voltage | −45 | Vdc |
| $V_{CBO}$ | Collector − Base Voltage | −50 | Vdc |
| $V_{EBO}$ | Emitter − Base Voltage | −6.0 | Vdc |
| $I_C$ | Collector Current − Continuous | −100 | mAdc |
| ESD Class | Electrostatic Discharge HBM<br>MM | 2<br>B | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL CHARACTERISTICS

| Symbol | Characteristic (Single Heated) | Max | Unit |
|---|---|---|---|
| $P_D$ | Total Device Dissipation $T_A$ = 25°C<br>Derate above 25°C (Note 1) | 240<br>1.9 | mW<br>mW/°C |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient (Note 1) | 520 | °C/W |
| $P_D$ | Total Device Dissipation $T_A$ = 25°C<br>Derate above 25°C (Note 2) | 280<br>2.2 | mW<br>mW/°C |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient (Note 2) | 446 | °C/W |
| **Symbol** | **Characteristic (Dual Heated) (Note 3)** | **Max** | **Unit** |
| $P_D$ | Total Device Dissipation $T_A$ = 25°C<br>Derate above 25°C (Note 1) | 350<br>2.8 | mW<br>mW/°C |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient (Note 1) | 357 | °C/W |
| $P_D$ | Total Device Dissipation $T_A$ = 25°C<br>Derate above 25°C (Note 2) | 420<br>3.4 | mW<br>mW/°C |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient (Note 2) | 297 | °C/W |
| $T_J$, $T_{stg}$ | Junction and Storage Temperature Range | −55 to +150 | °C |

1. FR−4 @ 100 $mm^2$, 1 oz. copper traces, still air.
2. FR−4 @ 500 $mm^2$, 1 oz. copper traces, still air.
3. Dual heated values assume total power is sum of two equally powered channels.

### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| NST857BDP6T5G | SOT−963<br>(Pb−Free) | 8,000/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Symbol | Characteristic | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| $V_{(BR)CEO}$ | Collector – Emitter Breakdown Voltage ($I_C$ = −10 mA) | −45 | – | – | V |
| $V_{(BR)CES}$ | Collector – Emitter Breakdown Voltage ($I_C$ = −10 μA, $V_{EB}$ = 0) | −50 | – | – | V |
| $V_{(BR)CBO}$ | Collector – Base Breakdown Voltage ($I_C$ = −10 μA) | −50 | – | – | V |
| $V_{(BR)EBO}$ | Emitter – Base Breakdown Voltage ($I_E$ = −1.0 μA) | −5.0 | – | – | V |
| $I_{CBO}$ | Collector Cutoff Current ($V_{CB}$ = −30 V)<br>($V_{CB}$ = −30 V, $T_A$ = 150°C) | –<br>– | –<br>– | −15<br>−4.0 | nA<br>μA |
| **ON CHARACTERISTICS** | | | | | |
| $h_{FE}$ | DC Current Gain<br>($I_C$ = −10 μA, $V_{CE}$ = −5.0 V)<br>($I_C$ = −2.0 mA, $V_{CE}$ = −5.0 V) | <br>–<br>220 | <br>150<br>290 | <br>–<br>475 | – |
| $V_{CE(sat)}$ | Collector – Emitter Saturation Voltage<br>($I_C$ = −10 mA, $I_B$ = −0.5 mA)<br>($I_C$ = −100 mA, $I_B$ = −5.0 mA) | <br>–<br>– | <br>–<br>– | <br>−0.3<br>−0.7 | V |
| $V_{BE(sat)}$ | Base – Emitter Saturation Voltage<br>($I_C$ = −10 mA, $I_B$ = −0.5 mA)<br>($I_C$ = −100 mA, $I_B$ = −5.0 mA) | <br>–<br>– | <br>−0.7<br>−0.9 | <br>–<br>– | V |
| $V_{BE(on)}$ | Base – Emitter On Voltage<br>($I_C$ = −2.0 mA, $V_{CE}$ = −5.0 V)<br>($I_C$ = −10 mA, $V_{CE}$ = −5.0 V) | <br>−0.6<br>– | <br>–<br>– | <br>−0.75<br>−0.82 | V |
| **SMALL−SIGNAL CHARACTERISTICS** | | | | | |
| $f_T$ | Current – Gain – Bandwidth Product<br>($I_C$ = −10 mA, $V_{CE}$ = −5.0 Vdc, f = 100 MHz) | 100 | – | – | MHz |
| $C_{obo}$ | Output Capacitance<br>($V_{CB}$ = −10 V, f = 1.0 MHz) | – | – | 4.5 | pF |
| $C_{ibo}$ | Input Capacitance<br>($V_{EB}$ = −0.5 V, f = 1.0 MHz) | – | – | 10 | pF |
| NF | Noise Figure<br>($I_C$ = −0.2 mA, $V_{CE}$ = −5.0 Vdc, $R_S$ = 2.0 kΩ,<br>f = 1.0 kHz, BW = 200 Hz) | – | – | 10 | dB |

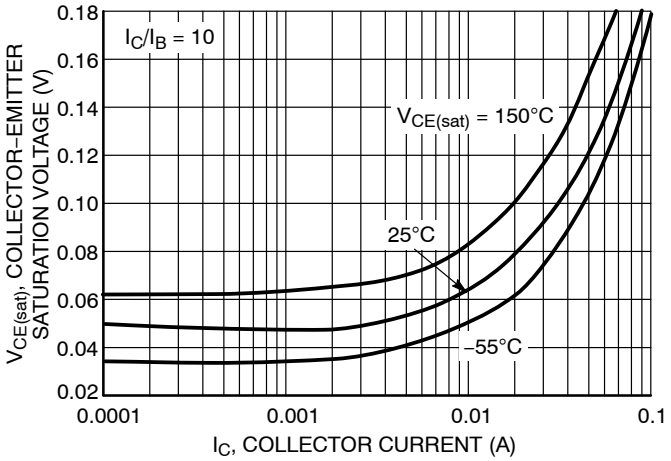



**Figure 1. Collector Emitter Saturation Voltage vs. Collector Current**

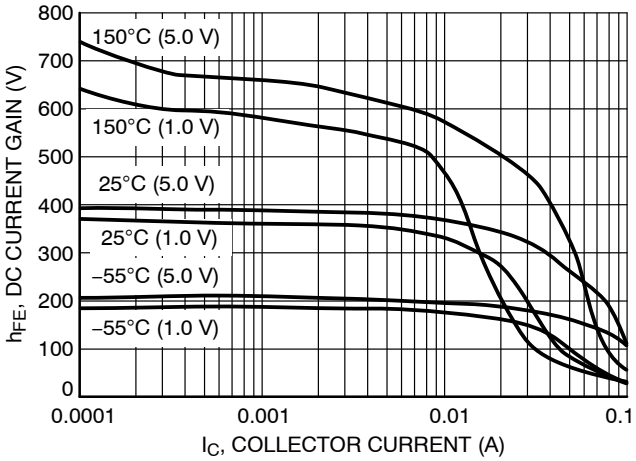



**Figure 2. DC Current Gain vs. Collector Current**

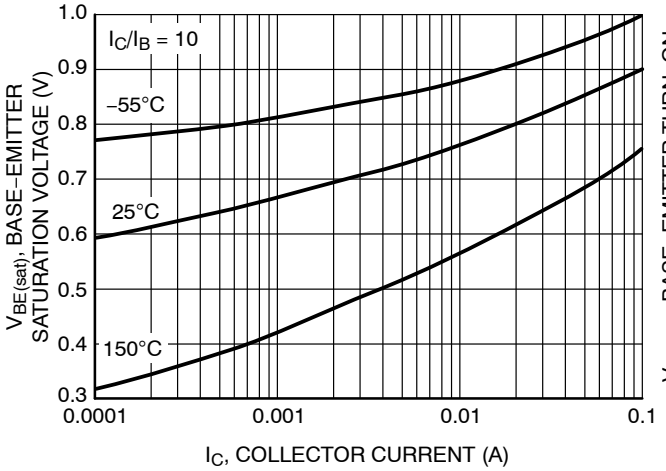



**Figure 3. Base Emitter Saturation Voltage vs. Collector Current**

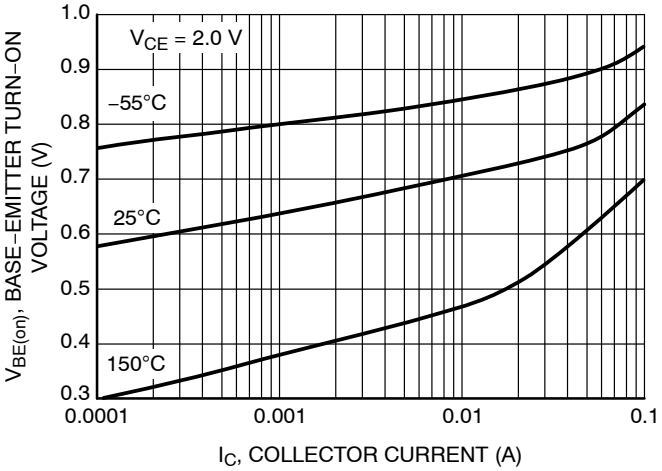



**Figure 4. Base Emitter Turn−On Voltage vs. Collector Current**

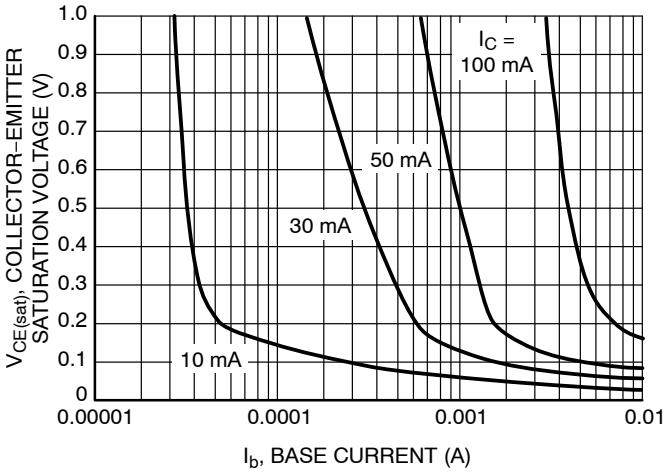



**Figure 5. Saturation Region**

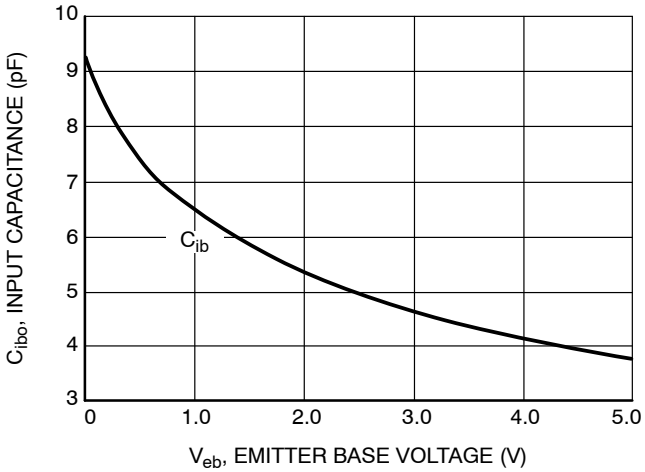



**Figure 6. Input Capacitance**

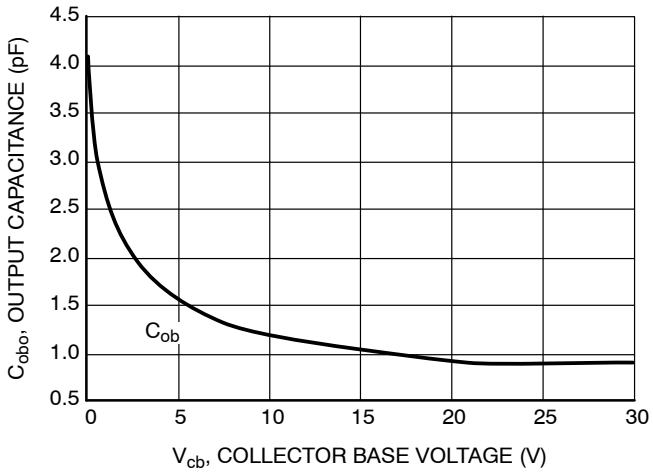
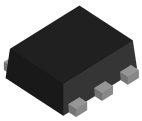



**Figure 7. Output Capacitance**

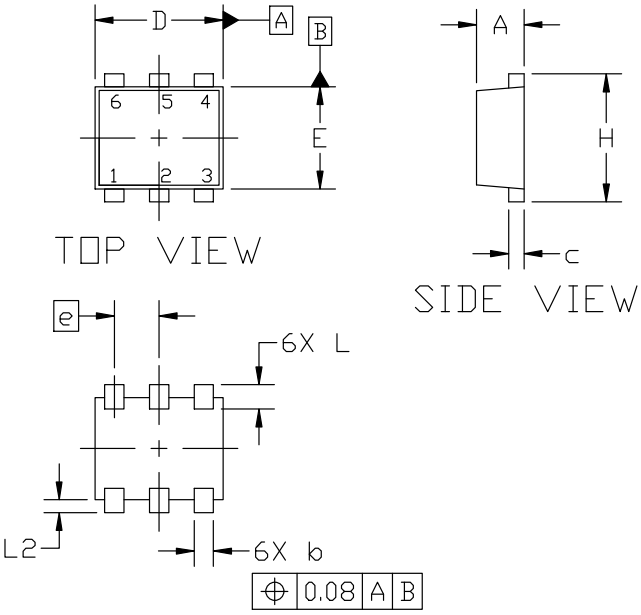


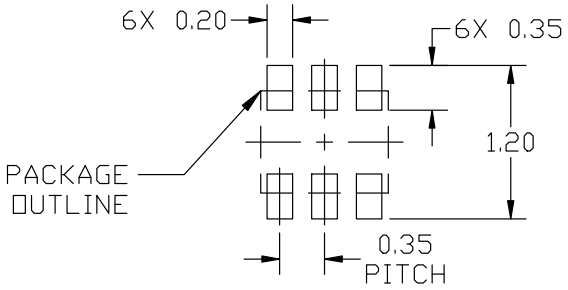
**SOT−963 1.00x1.00x0.37, 0.35P**
CASE 527AD
ISSUE F

DATE 20 FEB 2024

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | 0.34 | 0.37 | 0.40 |
| b | 0.10 | 0.15 | 0.20 |
| c | 0.07 | 0.12 | 0.17 |
| D | 0.95 | 1.00 | 1.05 |
| E | 0.75 | 0.80 | 0.85 |
| e | 0.35 BSC | | |
| H | 0.95 | 1.00 | 1.05 |
| L | 0.19 REF | | |
| L2 | 0.05 | 0.10 | 0.15 |




*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference manual, SOLDERRM/D.

STYLE 1:
PIN 1. EMITTER 1
2. BASE 1
3. COLLECTOR 2
4. EMITTER 2
5. BASE 2
6. COLLECTOR 1

STYLE 2:
PIN 1. EMITTER 1
2. EMITTER2
3. BASE 2
4. COLLECTOR 2
5. BASE 1
6. COLLECTOR 1

STYLE 3:
PIN 1. CATHODE 1
2. CATHODE 1
3. ANODE/ANODE 2
4. CATHODE 2
5. CATHODE 2
6. ANODE/ANODE 1

STYLE 4:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 5:
PIN 1. CATHODE
2. CATHODE
3. ANODE
4. ANODE
5. CATHODE
6. CATHODE

STYLE 6:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

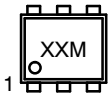
STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. ANODE
6. CATHODE

STYLE 8:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 9:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 10:
PIN 1. CATHODE 1
2. N/C
3. CATHODE 2
4. ANODE 2
5. N/C
6. ANODE 1

**GENERIC MARKING DIAGRAM***




XX = Specific Device Code
M = Month Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

| | | |
|---|---|---|
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