Step-Up/Down/ Inverting Switching Regulators, 2.5 A

NCV33163

The NCV33163 series are monolithic power switching regulators that contain the primary functions required for DC−to−DC converters. This series is specifically designed to be incorporated in step−up, step−down, and voltage−inverting applications with a minimum number of external components.

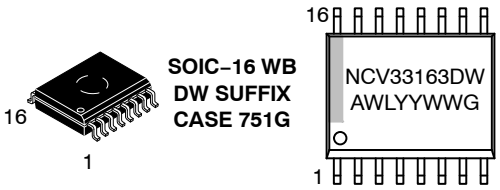
These devices consist of two high gain voltage feedback comparators, temperature compensated reference, controlled duty cycle oscillator, driver with bootstrap capability for increased efficiency, and a high current output switch. Protective features consist of cycle−by−cycle current limiting, and internal thermal shutdown. Also included is a low voltage indicator output designed to interface with microprocessor based systems.

These devices are contained in a 16 pin dual−in−line heat tab plastic package for improved thermal conduction.

Features

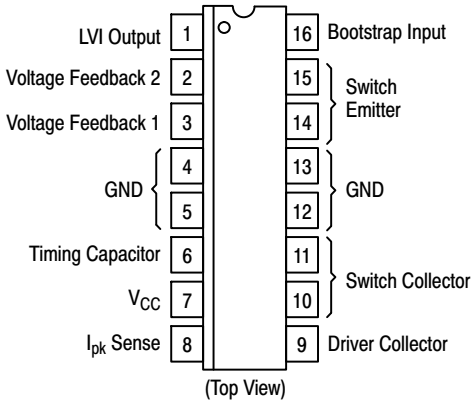
- Output Switch Current in Excess of 2.0 A
- Operation from 2.5 V to 60 V_{OC} Input
- Low Standby Current
- Precision 2% Reference
- Controlled Duty Cycle Oscillator
- Driver with Bootstrap Capability for Increased Efficiency
- Cycle−by−Cycle Current Limiting
- Internal Thermal Shutdown Protection
- Low Voltage Indicator Output for Direct Microprocessor Interface
- Heat Tab Power Package
- Moisture Sensitivity Level (MSL) Equals 1
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements
- Pb−Free Packages are Available

MARKING DIAGRAMS



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

PIN CONNECTIONS



(Top View)

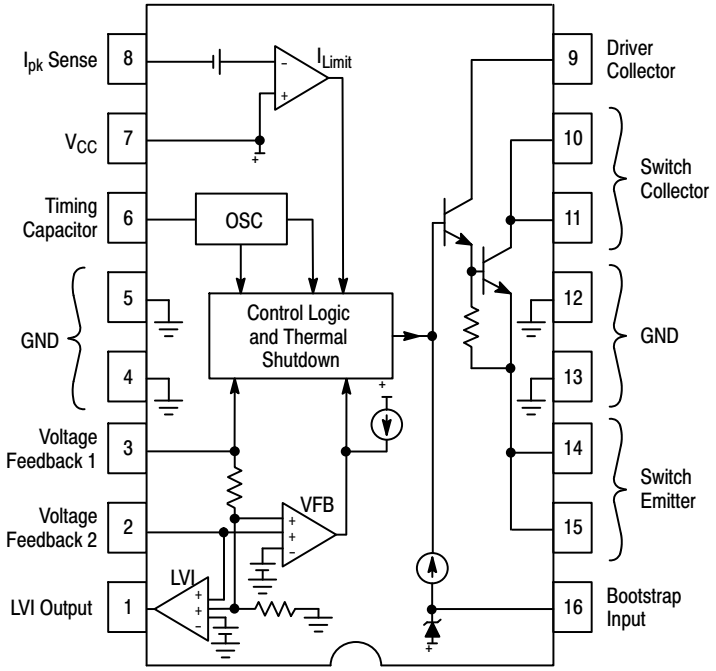
ORDERING INFORMATION

Device	Package	Shipping†
NCV33163DWR2G	SOIC−16 WB (Pb−Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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May, 2023 − Rev. 5
Publication Order Number:
NCV33163/D



This device contains 114 active transistors.

Figure 1. Representative Block Diagram

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	60	V
Switch Collector Voltage Range	$V_{C(switch)}$	−1.0 to + 60	V
Switch Emitter Voltage Range	$V_{E(switch)}$	− 2.0 to $V_{C(switch)}$	V
Switch Collector to Emitter Voltage	$V_{CE(switch)}$	60	V
Switch Current (Note 2)	I_{SW}	2.5	A
Driver Collector Voltage	$V_{C(driver)}$	−1.0 to +60	V
Driver Collector Current	$I_{C(driver)}$	150	mA
Bootstrap Input Current Range (Note 2)	I_{BS}	−100 to +100	mA
Current Sense Input Voltage Range	$V_{Ipk\ (Sense)}$	(V_{CC}−7.0) to (V_{CC}+1.0)	V
Feedback and Timing Capacitor Input Voltage Range	V_{in}	−1.0 to + 7.0	V
Low Voltage Indicator Output Voltage Range	$V_{C(LVI)}$	−1.0 to + 60	V
Low Voltage Indicator Output Sink Current	$I_{C(LVI)}$	10	mA
Thermal Characteristics P Suffix, Dual−In−Line Case 648C Thermal Resistance, Junction−to−Air Thermal Resistance, Junction−to−Case (Pins 4, 5, 12, 13) DW Suffix, Surface Mount Case 751G Thermal Resistance, Junction−to−Air Thermal Resistance, Junction−to−Case (Pins 4, 5, 12, 13)	 $R_{\theta JA}$ $R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JC}$	 80 15 94 18	°C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature	T_A	− 40 to + 115	°C
Storage Temperature Range	T_{stg}	− 65 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series contains ESD protection and exceeds the following tests:
   Human Body Model 1500 V per MIL−STD−883, Method 3015.
   Machine Model Method 150 V.
2. Maximum package power dissipation limits must be observed.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 15 V, Pin 16 = V_{CC}, C_T = 620 pF, for typical values T_A = 25°C, for min/max values T_A = −40°C to +115°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Frequency T_A = 25°C Total Variation over V_{CC} = 2.5 V to 60 V, and Temperature	f_{OSC}	 46 45	 55 –	 59 60	kHz
Charge Current	I_{chg}	–	225	–	μA
Discharge Current	I_{dischg}	–	25	–	μA
Charge to Discharge Current Ratio	I_{chg}/I_{dischg}	8.0	9.0	10	–
Sawtooth Peak Voltage	$V_{OSC(P)}$	–	1.25	–	V
Sawtooth Valley Voltage	$V_{OSC(V)}$	–	0.55	–	V
FEEDBACK COMPARATOR 1					
Threshold Voltage T_A = 25°C Line Regulation (V_{CC} = 2.5 V to 60 V, T_A = 25°C) Total Variation over Line, and Temperature	$V_{th(FB1)}$	 4.9 – 4.85	 5.05 0.008 –	 5.2 0.03 5.25	 V %/V V
Input Bias Current (V_{FB1} = 5.05 V)	$I_{IB(FB1)}$	–	100	200	μA
FEEDBACK COMPARATOR 2					
Threshold Voltage T_A = 25°C Line Regulation (V_{CC} = 2.5 V to 60 V, T_A = 25°C) Total Variation over Line, and Temperature	$V_{th(FB2)}$	 1.225 – 1.213	 1.25 0.008 –	 1.275 0.03 1.287	 V %/V V
Input Bias Current (V_{FB2} = 1.25 V)	$I_{IB(FB2)}$	– 0.4	0	0.4	μA
CURRENT LIMIT COMPARATOR					
Threshold Voltage T_A = 25°C Total Variation over V_{CC} = 2.5 V to 60 V, and Temperature	$V_{th(Ipk\ Sense)}$	 – 230	 250 –	 – 270	mV
Input Bias Current ($V_{Ipk\ (Sense)}$ = 15 V)	$I_{IB(sense)}$	–	1.0	20	μA
DRIVER AND OUTPUT SWITCH (Note 3)					
Sink Saturation Voltage (I_{SW} = 2.5 A, Pins 14, 15 grounded) Non−Darlington Connection ($R_{Pin\ 9}$ = 110 Ω to V_{CC}, $I_{SW}/I_{DRV} \approx 20$) Darlington Connection (Pins 9, 10, 11 connected)	$V_{CE(sat)}$	 – –	 0.6 1.0	 1.0 1.4	V
Collector Off−State Leakage Current (V_{CE} = 60 V)	$I_{C(off)}$	–	0.02	100	μA
Bootstrap Input Current Source (V_{BS} = V_{CC} + 5.0 V)	$I_{source(DRV)}$	0.5	2.0	4.0	mA
Bootstrap Input Zener Clamp Voltage (I_Z = 25 mA)	V_Z	V_{CC} + 6.0	V_{CC} + 7.0	V_{CC} + 9.0	V
LOW VOLTAGE INDICATOR					
Input Threshold (V_{FB2} Increasing)	V_{th}	1.07	1.125	1.18	V
Input Hysteresis (V_{FB2} Decreasing)	V_H	–	15	–	mV
Output Sink Saturation Voltage (I_{sink} = 2.0 mA)	$V_{OL(LVI)}$	–	0.15	0.4	V
Output Off−State Leakage Current (V_{OH} = 15 V)	I_{OH}	–	0.01	5.0	μA
TOTAL DEVICE					
Standby Supply Current (V_{CC} = 2.5 V to 60 V, Pin 8 = V_{CC}, Pins 6, 14, 15 = GND, remaining pins open)	I_{CC}	–	6.0	10	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

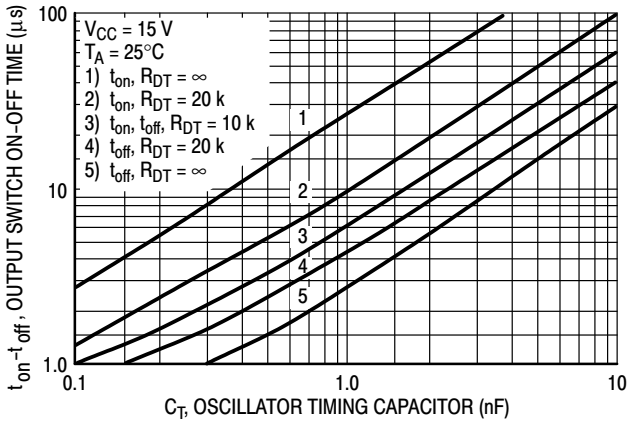


Figure 2. Output Switch On−Off Time versus Oscillator Timing Capacitor

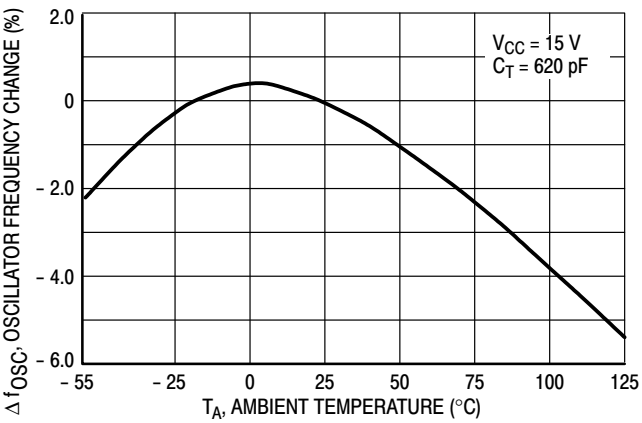


Figure 3. Oscillator Frequency Change versus Temperature

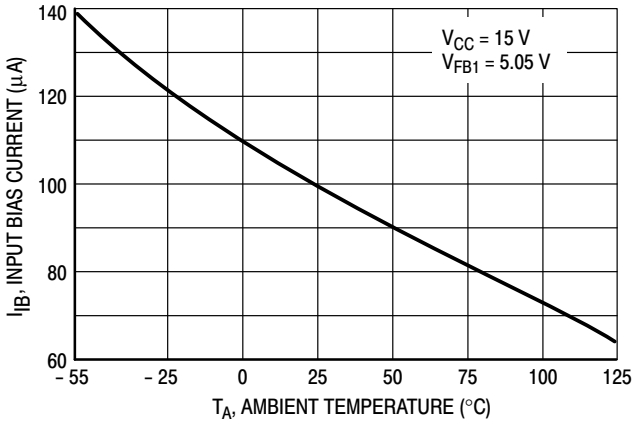


Figure 4. Feedback Comparator 1 Input Bias Current versus Temperature

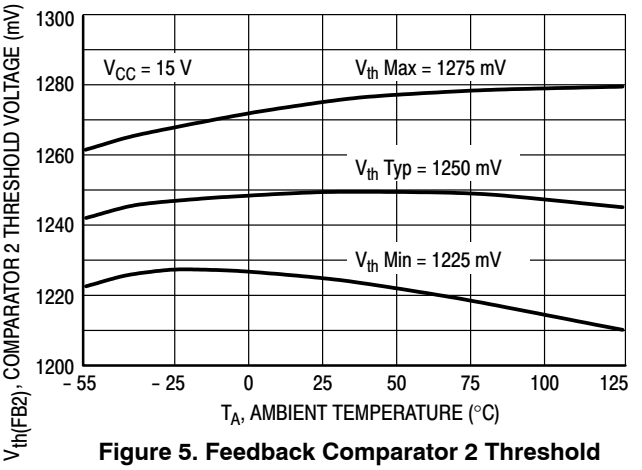


Figure 5. Feedback Comparator 2 Threshold Voltage versus Temperature

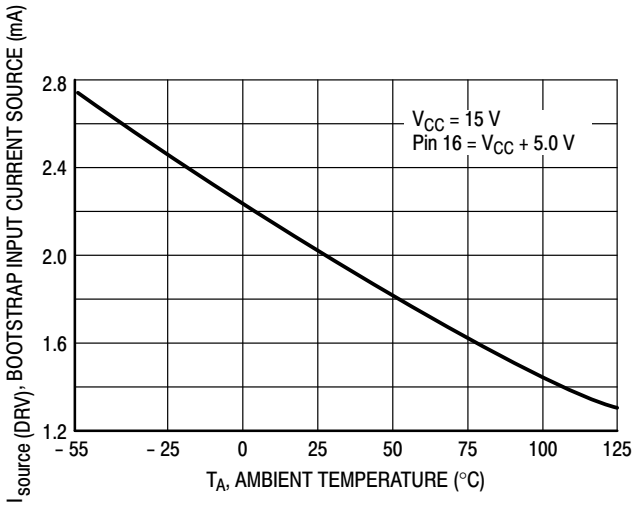


Figure 6. Bootstrap Input Current Source versus Temperature

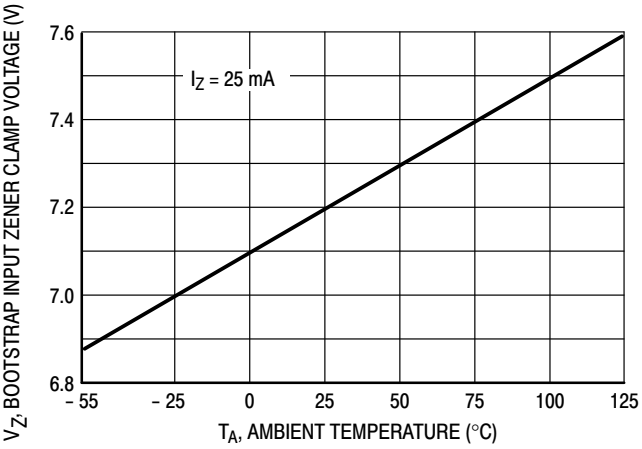


Figure 7. Bootstrap Input Zener Clamp Voltage versus Temperature

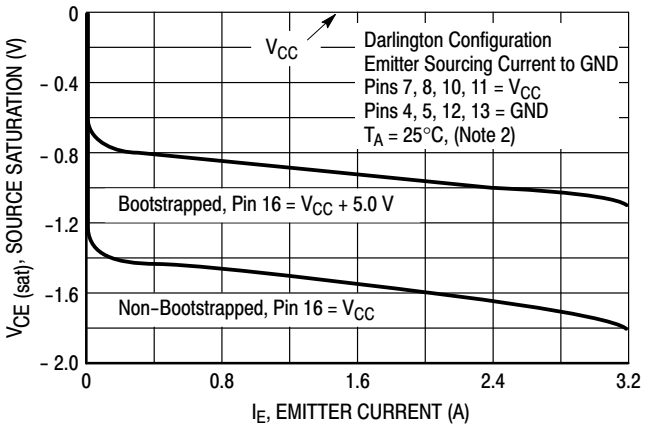


Figure 8. Output Switch Source Saturation versus Emitter Current

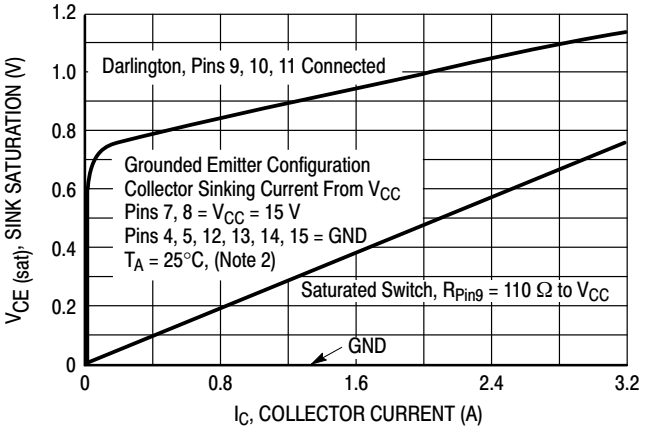


Figure 9. Output Switch Sink Saturation versus Collector Current

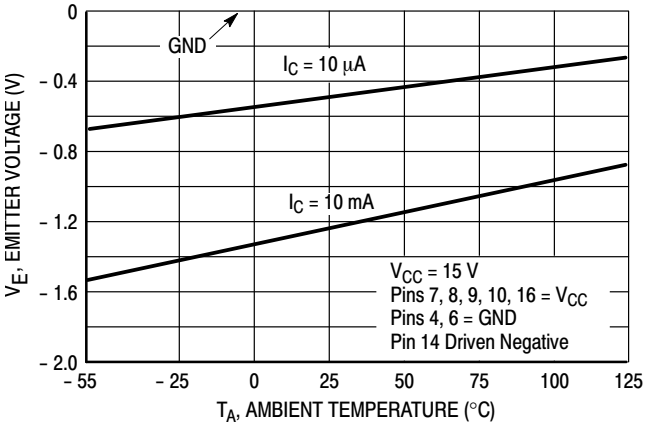


Figure 10. Output Switch Negative Emitter Voltage versus Temperature

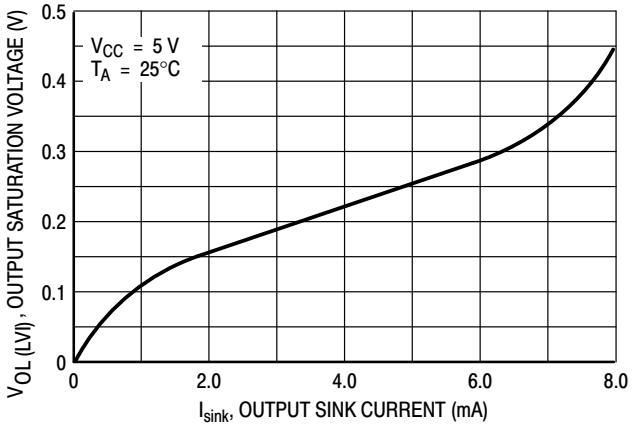


Figure 11. Low Voltage Indicator Output Sink Saturation Voltage versus Sink Current

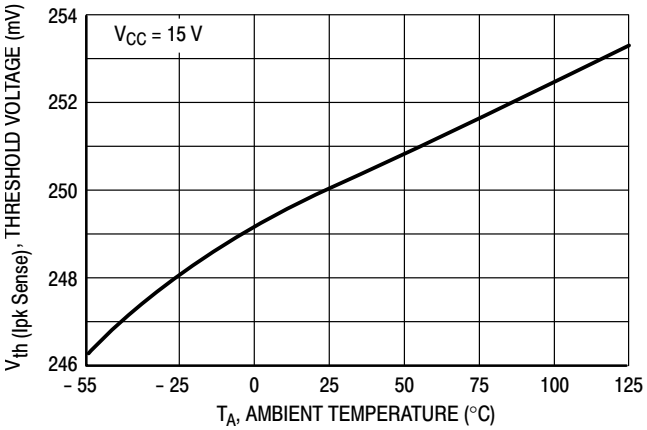


Figure 12. Current Limit Comparator Threshold Voltage versus Temperature

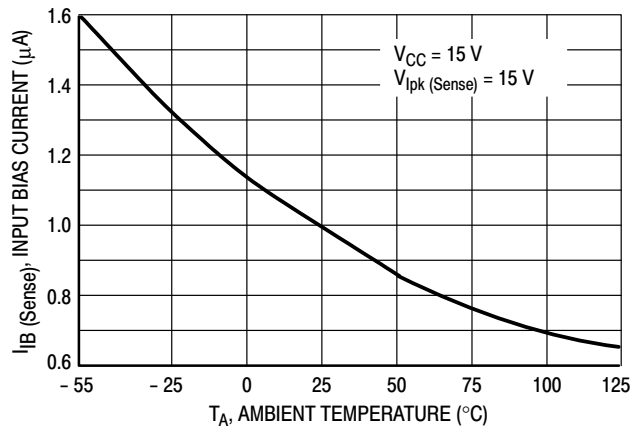


Figure 13. Current Limit Comparator Input Bias Current versus Temperature

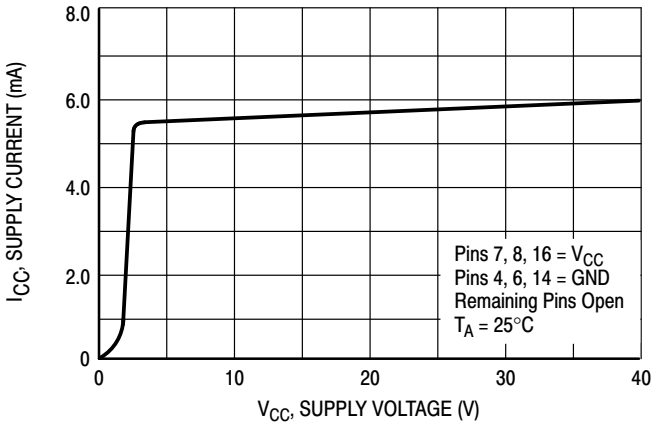


Figure 14. Standby Supply Current versus Supply Voltage

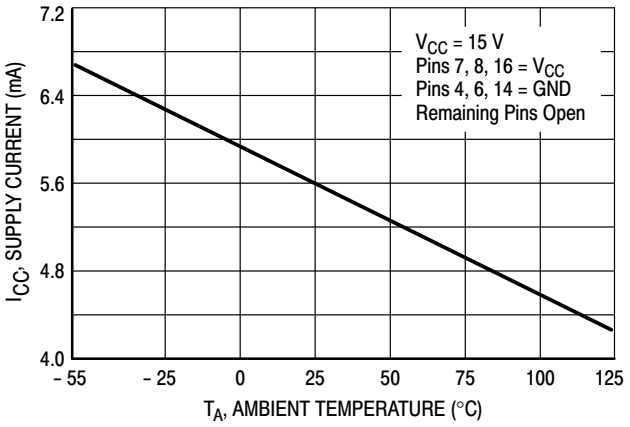


Figure 15. Standby Supply Current versus Temperature

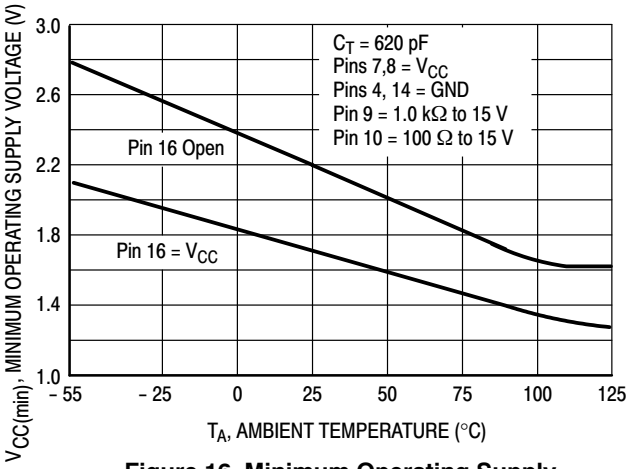


Figure 16. Minimum Operating Supply Voltage versus Temperature

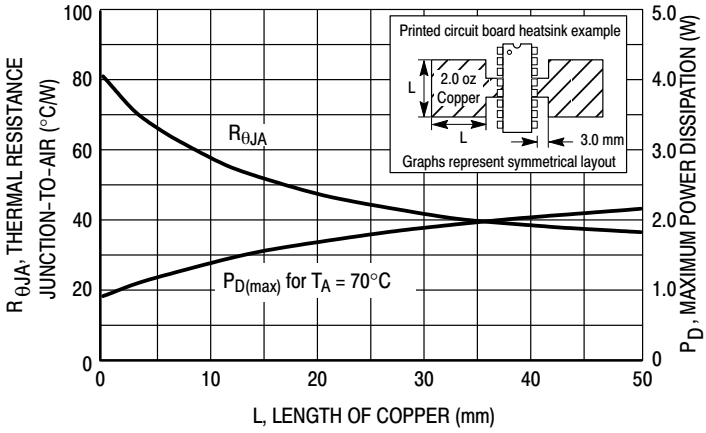


Figure 17. P Suffix (DIP–16) Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

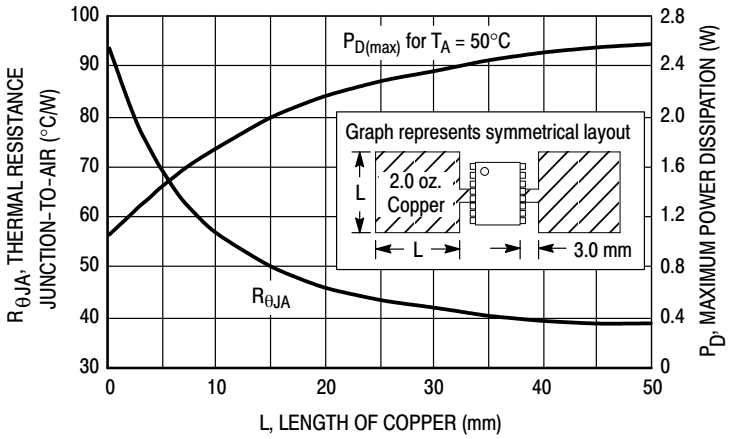


Figure 18. DW Suffix (SOP–16L) Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

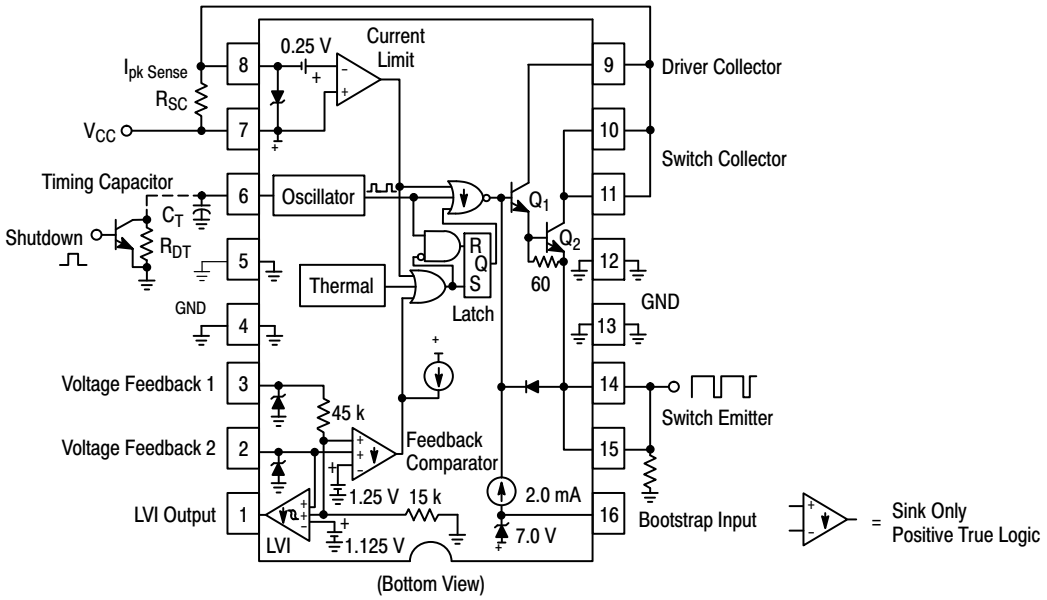


Figure 19. Representative Block Diagram

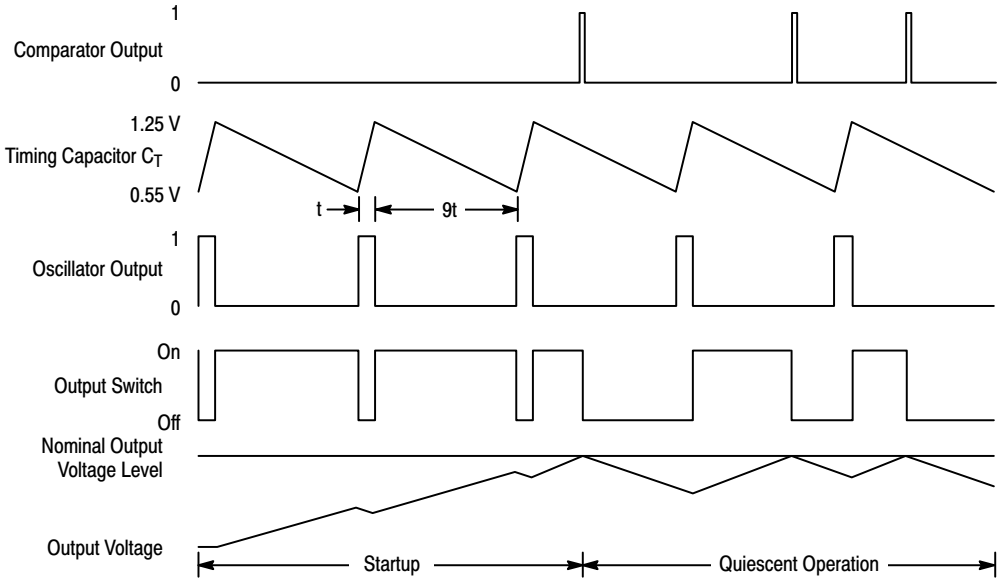


Figure 20. Typical Operating Waveforms

INTRODUCTION

The NCV33163 series are monolithic power switching regulators optimized for DC−to−DC converter applications. The combination of features in this series enables the system designer to directly implement step−up, step−down, and voltage−inverting converters with a minimum number of external components. Potential applications include cost sensitive consumer products as well as equipment for the automotive, computer, and industrial markets. A Representative Block Diagram is shown in Figure 19.

Operating Description

The NCV33163 operates as a fixed on−time, variable off−time voltage mode ripple regulator. In general, this mode of operation is somewhat analogous to a capacitor charge pump and does not require dominant pole loop compensation for converter stability. The Typical Operating Waveforms are shown in Figure 20. The output voltage waveform shown is for a step−down converter with the ripple and phasing exaggerated for clarity. During initial converter startup, the feedback comparator senses that the output voltage level is below nominal. This causes the output switch to turn on and off at a frequency and duty cycle controlled by the oscillator, thus pumping up the output filter capacitor. When the output voltage level reaches nominal, the feedback comparator sets the latch, immediately terminating switch conduction. The feedback comparator will inhibit the switch until the load current causes the output voltage to fall below nominal. Under these conditions, output switch conduction can be inhibited for a partial oscillator cycle, a partial cycle plus a complete cycle, multiple cycles, or a partial cycle plus multiple cycles.

Oscillator

The oscillator frequency and on−time of the output switch are programmed by the value selected for timing capacitor C_T. Capacitor C_T is charged and discharged by a 9 to 1 ratio internal current source and sink, generating a negative going sawtooth waveform at Pin 6. As C_T charges, an internal pulse is generated at the oscillator output. This pulse is connected to the NOR gate center input, preventing output switch conduction, and to the AND gate upper input, allowing the latch to be reset if the comparator output is low. Thus, the output switch is always disabled during ramp−up and can be enabled by the comparator output only at the start of ramp−down. The oscillator peak and valley thresholds are 1.25 V and 0.55 V, respectively, with a charge current of 225 μA and a discharge current of 25 μA, yielding a maximum on−time duty cycle of 90%. A reduction of the maximum duty cycle may be required for specific converter configurations. This can be accomplished with the addition of an external deadtime resistor (R_{DT}) placed across C_T. The resistor increases the discharge current which reduces the on−time of the output switch. A graph of the Output Switch On−Off Time versus Oscillator Timing Capacitance for various values of R_{DT} is shown in Figure 2. Note that the maximum output duty cycle, $t_{on}/t_{on} + t_{off}$, remains constant for values of C_T greater than 0.2 nF. The converter output can be inhibited by clamping C_T to ground with an external NPN small−signal transistor.

Feedback and Low Voltage Indicator Comparators

Output voltage control is established by the Feedback comparator. The inverting input is internally biased at 1.25 V and is not pinned out. The converter output voltage is typically divided down with two external resistors and monitored by the high impedance noninverting input at Pin 2. The maximum input bias current is ±0.4 μA, which can cause an output voltage error that is equal to the product of the input bias current and the upper divider resistance value. For applications that require 5.0 V, the converter output can be directly connected to the noninverting input at Pin 3. The high impedance input, Pin 2, must be grounded to prevent noise pickup. The internal resistor divider is set for a nominal voltage of 5.05 V. The additional 50 mV compensates for a 1.0% voltage drop in the cable and connector from the converter output to the load. The Feedback comparator's output state is controlled by the highest voltage applied to either of the two noninverting inputs.

The Low Voltage Indicator (LVI) comparator is designed for use as a reset controller in microprocessor−based systems. The inverting input is internally biased at 1.125 V, which sets the noninverting input thresholds to 90% of nominal. The LVI comparator has 15 mV of hysteresis to prevent erratic reset operation. The Open Collector output is capable of sinking in excess of 6.0 mA (see Figure 11). An external resistor (R_{LVI}) and capacitor (C_{DLY}) can be used to program a reset delay time (t_{DLY}) by the formula shown below, where $V_{th(MPU)}$ is the microprocessor reset input threshold. Refer to Figure 21.

$$t_{DLY} = R_{LVI}\, C_{DLY}\, \ln\left(\frac{1}{1 - \frac{V_{th(MPU)}}{V_{out}}}\right)$$

Current Limit Comparator, Latch and Thermal Shutdown

With a voltage mode ripple converter operating under normal conditions, output switch conduction is initiated by the oscillator and terminated by the Voltage Feedback comparator. Abnormal operating conditions occur when the converter output is overloaded or when feedback voltage sensing is lost. Under these conditions, the Current Limit comparator will protect the Output Switch.

The switch current is converted to a voltage by inserting a fractional ohm resistor, R_{SC}, in series with V_{CC} and output switch transistor Q_2. The voltage drop across R_{SC} is monitored by the Current Sense comparator. If the voltage drop exceeds 250 mV with respect to V_{CC}, the comparator will set the latch and terminate output switch conduction on a cycle−by−cycle basis. This Comparator/Latch configuration ensures that the Output Switch has only a single on−time during a given oscillator cycle. The calculation for a value of R_{SC} is:

$$R_{SC} = \frac{0.25\ V}{I_{pk}\ (Switch)}$$

Figures 12 and 13 show that the Current Sense comparator threshold is tightly controlled over temperature and has a typical input bias current of 1.0 μA. The propagation delay from the comparator input to the Output Switch is typically 200 ns. The parasitic inductance associated with R_{SC} and the circuit layout should be minimized. This will prevent unwanted voltage spikes that may falsely trip the Current Limit comparator.

Internal thermal shutdown circuitry is provided to protect the IC in the event that the maximum junction temperature is exceeded. When activated, typically at 170°C, the Latch is forced into the “Set” state, disabling the Output Switch. This feature is provided to prevent catastrophic failures from accidental device overheating. It is not intended to be used as a replacement for proper heatsinking.

Driver and Output Switch

To aid in system design flexibility and conversion efficiency, the driver current source and collector, and output switch collector and emitter are pinned out separately. This allows the designer the option of driving the output switch into saturation with a selected force gain or driving it near saturation when connected as a Darlington. The output switch is designed to switch a maximum of 60 V collector to emitter, with up to 2.5 A peak collector current. The minimum value for R_{SC} is:

$$R_{SC(min)} = \frac{0.25\ V}{2.5\ A} = 0.100\ \Omega$$

When configured for step−down or voltage−inverting applications, as in Figures 21 and 25, the inductor will forward bias the output rectifier when the switch turns off. Rectifiers with a high forward voltage drop or long turn−on delay time should not be used. If the emitter is allowed to go sufficiently negative, collector current will flow, causing additional device heating and reduced conversion efficiency.

Figure 10 shows that by clamping the emitter to 0.5 V, the collector current will be in the range 10 μA over temperature. A 1N5822 or equivalent Schottky barrier rectifier is recommended to fulfill these requirements.

A bootstrap input is provided to reduce the output switch saturation voltage in step−down and voltage−inverting converter applications. This input is connected through a series resistor and capacitor to the switch emitter and is used to raise the internal 2.0 mA bias current source above V_{CC}. An internal zener limits the bootstrap input voltage to V_{CC} +7.0 V. The capacitor’s equivalent series resistance must limit the zener current to less than 100 mA. An additional series resistor may be required when using tantalum or other low ESR capacitors. The equation below is used to calculate a minimum value bootstrap capacitor based on a minimum zener voltage and an upper limit current source.

$$C_{B(min)} = I\ \frac{\Delta t}{\Delta V} = 4.0\ mA \frac{t_{on}}{4.0\ V} = 0.001\ t_{on}$$

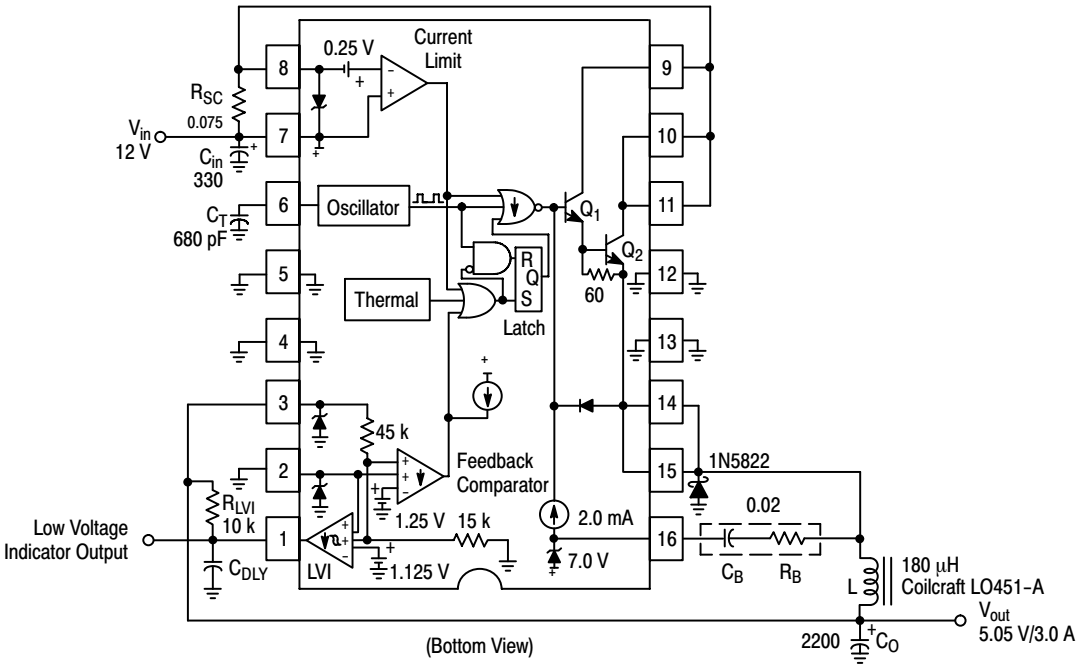
Parametric operation of the NCV33163 is guaranteed over a supply voltage range of 2.5 V to 60 V. When operating below 3.0 V, the Bootstrap Input should be connected to V_{CC}. Figure 16 shows that functional operation down to 1.7 V at room temperature is possible.

Package

The NCV33163 is contained in a heat−sinkable 16−lead plastic dual−in−line package in which the die is mounted on a special heat tab copper alloy lead frame. This tab consists of the four center ground pins that are specifically designed to improve thermal conduction from the die to the circuit board. Figures 17 and 18 show a simple and effective method of utilizing the printed circuit board medium as a heat dissipater by soldering these pins to an adequate area of copper foil. This permits the use of standard layout and mounting practices while having the ability to halve the junction−to−air thermal resistance. These examples are for a symmetrical layout on a single−sided board with two ounce per square foot of copper.

APPLICATIONS

The following converter applications show the simplicity and flexibility of this circuit architecture. Three main converter topologies are demonstrated with actual test data shown below each of the circuit diagrams.



Test	Condition	Results
Line Regulation	V_{in} = 8.0 V to 24 V, I_O = 3.0 A	6.0 mV = ± 0.06%
Load Regulation	V_{in} = 12 V, I_O = 0.6 A to 3.0 A	2.0 mV = ± 0.02%
Output Ripple	V_{in} = 12 V, I_O = 3.0 A	36 mVpp
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	3.3 A
Efficiency, Without Bootstrap	V_{in} = 12 V, I_O = 3.0 A	76.7%
Efficiency, With Bootstrap	V_{in} = 12 V, I_O = 3.0 A	81.2%

Figure 21. Step−Down Converter

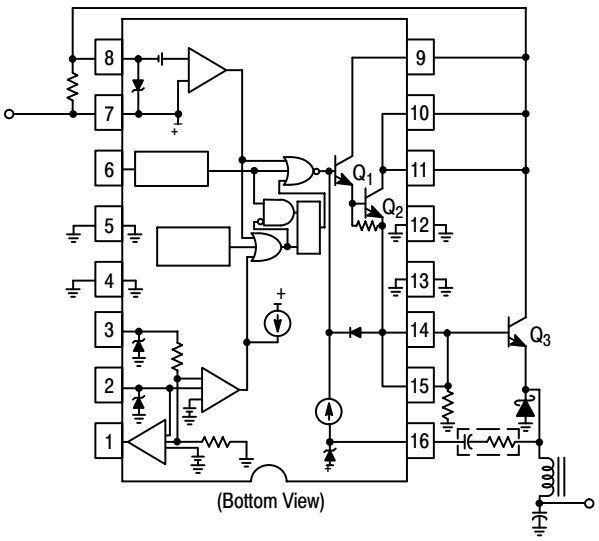


Figure 22A. External NPN Switch

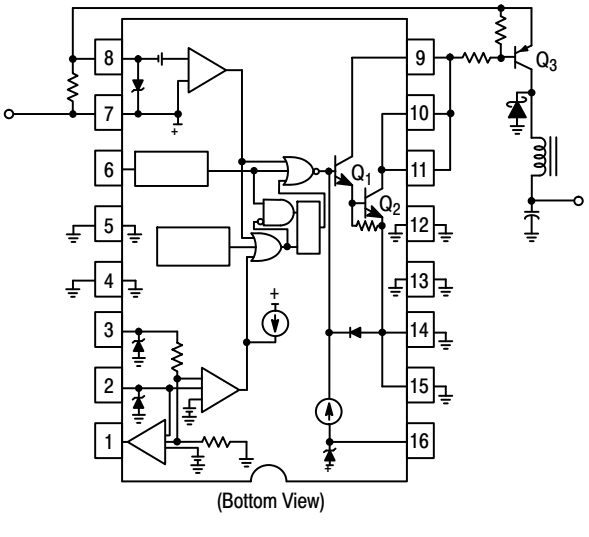
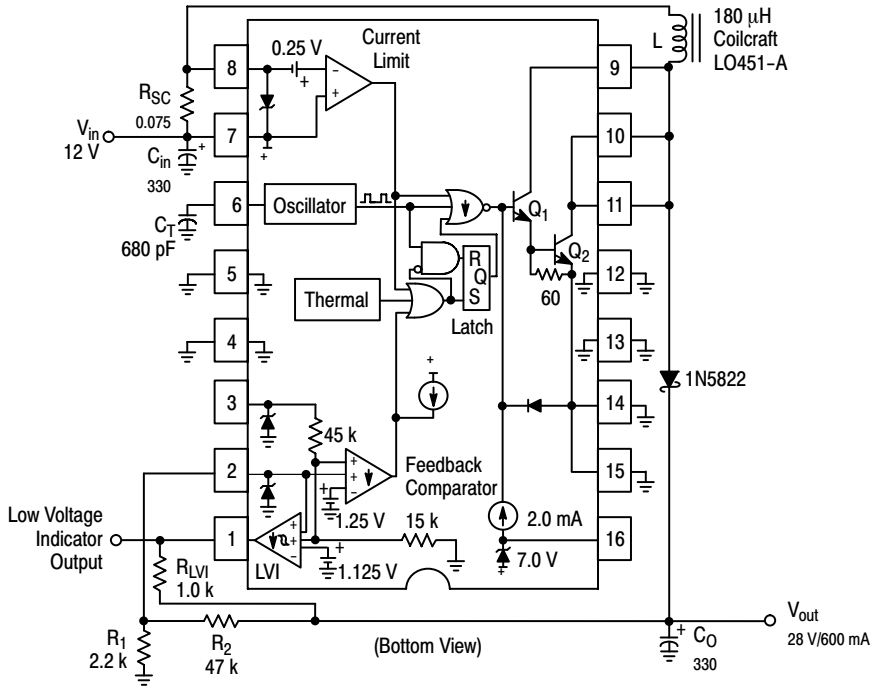


Figure 22B. External PNP Saturated Switch

Figure 22. External Current Boost Connections for $I_{pk\ (Switch)}$ Greater Than 2.5 A



Test	Condition	Results
Line Regulation	V_{in} = 9.0 V to 16 V, I_O = 0.6 A	30 mV = ± 0.05%
Load Regulation	V_{in} = 12 V, I_O = 0.1 A to 0.6 A	50 mV = ± 0.09%
Output Ripple	V_{in} = 12 V, I_O = 0.6 A	140 mVpp
Efficiency	V_{in} = 12 V, I_O = 0.6 A	88.1%

Figure 23. Step−Up Converter

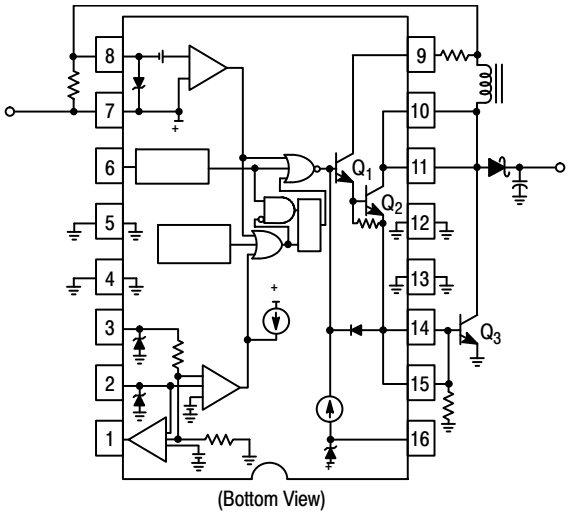


Figure 24A. External NPN Switch

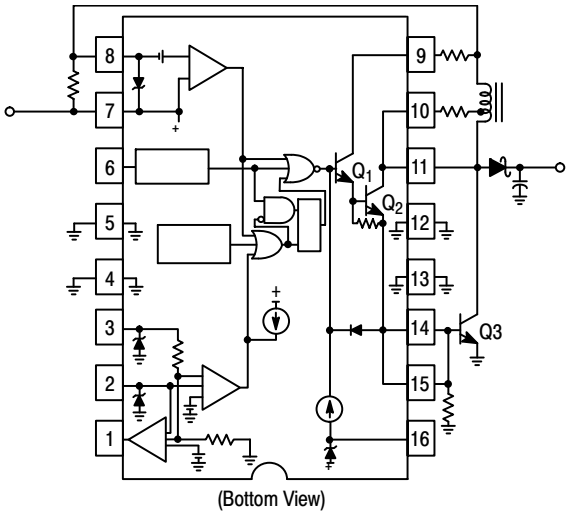
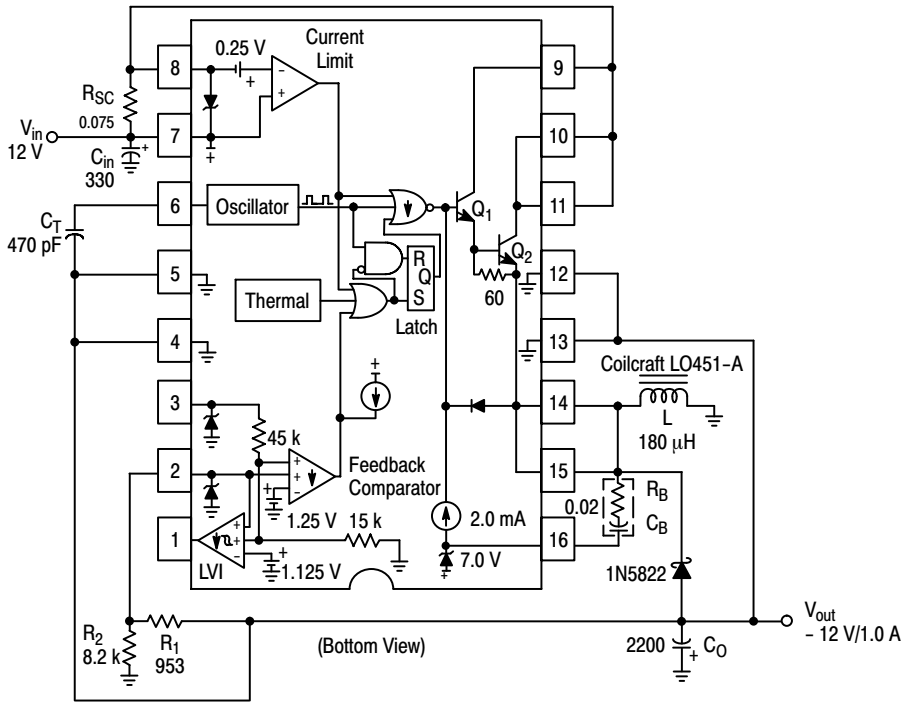


Figure 24B. External PNP Saturated Switch

Figure 24. External Current Boost Connections for $I_{pk\ (Switch)}$ Greater Than 2.5 A



Test	Condition	Results
Line Regulation	V_{in} = 9.0 V to 16 V, I_O = 1.0 A	5.0 mV = ± 0.02%
Load Regulation	V_{in} = 12 V, I_O = 0.6 A to 1.0 A	2.0 mV = ± 0.01%
Output Ripple	V_{in} = 12 V, I_O = 1.0 A	130 mVpp
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	3.2 A
Efficiency, Without Bootstrap	V_{in} = 12 V, I_O = 1.0 A	73.1%
Efficiency, With Bootstrap	V_{in} = 12 V, I_O = 1.0 A	77.5%

Figure 25. Voltage−Inverting Converter

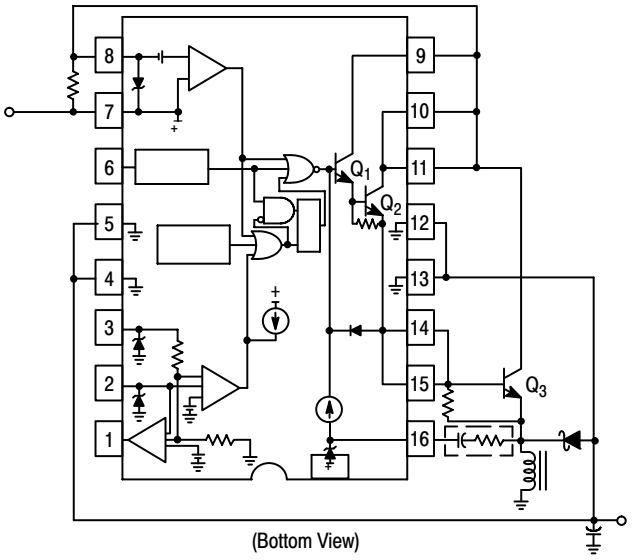


Figure 26A. External NPN Switch

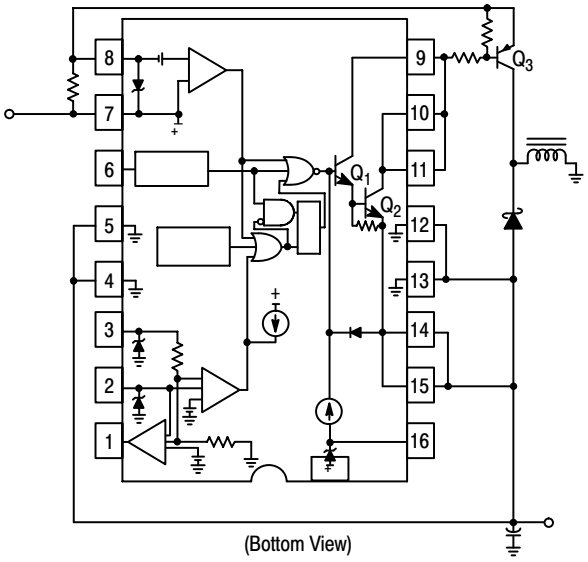


Figure 26B. External PNP Saturated Switch

Figure 26. External Current Boost Connections for $I_{pk\ (Switch)}$ Greater Than 2.5 A

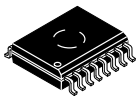
Calculation	Step−Down	Step−Up	Voltage−Inverting
$\frac{t_{on}}{t_{off}}$ (Notes 2, 3)	$\frac{V_{out} + V_F}{V_{in} - V_{sat} - V_{out}}$	$\frac{V_{out} + V_F - V_{in}}{V_{in} - V_{sat}}$	$\frac{\lvert V_{out}\rvert + V_F}{V_{in} - V_{sat}}$
t_{on}	$\frac{\frac{t_{on}}{t_{off}}}{f\left(\frac{t_{on}}{t_{off}} + 1\right)}$	$\frac{\frac{t_{on}}{t_{off}}}{f\left(\frac{t_{on}}{t_{off}} + 1\right)}$	$\frac{\frac{t_{on}}{t_{off}}}{f\left(\frac{t_{on}}{t_{off}} + 1\right)}$
C_T	$\frac{32.143 \cdot 10^{-6}}{f}$	$\frac{32.143 \cdot 10^{-6}}{f}$	$\frac{32.143 \cdot 10^{-6}}{f}$
$I_{L(avg)}$	I_{out}	$I_{out}\left(\frac{t_{on}}{t_{off}} + 1\right)$	$I_{out}\left(\frac{t_{on}}{t_{off}} + 1\right)$
$I_{pk\ (Switch)}$	$I_{L(avg)} + \frac{\Delta I_L}{2}$	$I_{L(avg)} + \frac{\Delta I_L}{2}$	$I_{L(avg)} + \frac{\Delta I_L}{2}$
R_{SC}	$\frac{0.25}{I_{pk\ (Switch)}}$	$\frac{0.25}{I_{pk\ (Switch)}}$	$\frac{0.25}{I_{pk\ (Switch)}}$
L	$\left(\frac{V_{in} - V_{sat} - V_{out}}{\Delta I_L}\right) t_{on}$	$\left(\frac{V_{in} - V_{sat}}{\Delta I_L}\right) t_{on}$	$\left(\frac{V_{in} - V_{sat}}{\Delta I_L}\right) t_{on}$
$V_{ripple(pp)}$	$\Delta I_L \sqrt{\left(\frac{1}{8 f C_O}\right)^2 + (ESR)^2}$	$\approx \frac{t_{on}\, I_{out}}{C_O}$	$\approx \frac{t_{on}\, I_{out}}{C_O}$
V_{out}	$V_{ref}\left(\frac{R_2}{R_1} + 1\right)$	$V_{ref}\left(\frac{R_2}{R_1} + 1\right)$	$V_{ref}\left(\frac{R_2}{R_1} + 1\right)$

The following Converter Characteristics must be chosen:

V_{in} − Nominal operating input voltage.
V_{out} − Desired output voltage.
I_{out} − Desired output current.
ΔI_L − Desired peak−to−peak inductor ripple current. For maximum output current it is suggested that ΔI_L be chosen to be less than 10% of the average inductor current $I_{L(avg)}$. This will help prevent $I_{pk\ (Switch)}$ from reaching the current limit threshold set by R_{SC}. If the design goal is to use a minimum inductance value, let $\Delta I_L = 2(I_{L(avg)})$. This will proportionally reduce converter output current capability.
f − Maximum output switch frequency.
$V_{ripple(pp)}$ − Desired peak−to−peak output ripple voltage. For best performance the ripple voltage should be kept to a low value since it will directly affect line and load regulation. Capacitor C_O should be a low equivalent series resistance (ESR) electrolytic designed for switching regulator applications.

NOTES: 1. V_{sat} − Saturation voltage of the output switch, refer to Figures 8 and 9.
2. V_F − Output rectifier forward voltage drop. Typical value for 1N5822 Schottky barrier rectifier is 0.5 V.
3. The calculated t_{on}/t_{off} must not exceed the minimum guaranteed oscillator charge to discharge ratio of 8, at the minimum operating input voltage.

Figure 27. Design Equations

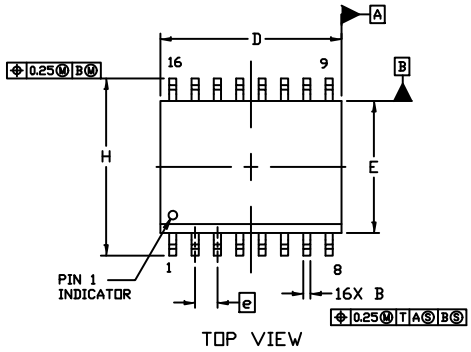


1

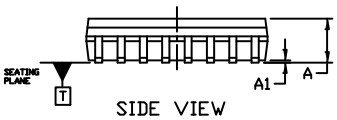
SCALE 1:1

SOIC−16 WB
CASE 751G
ISSUE E

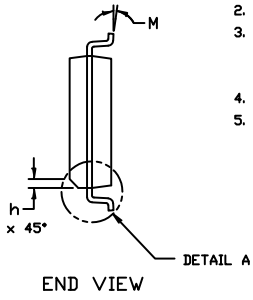
DATE 08 OCT 2021



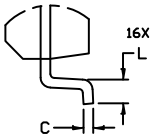
TOP VIEW



SIDE VIEW



END VIEW

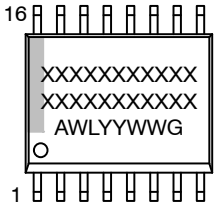


DETAIL A
2X SCALE

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION OR FLASH TO BE 0.15 PER SIDE.

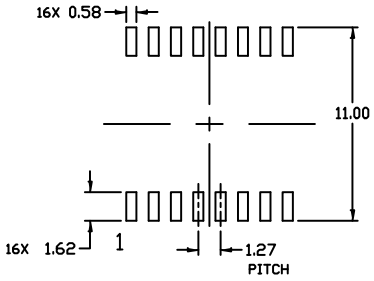
	MILLIMETERS	
DIM	MIN.	MAX.
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.53 REF	
L	0.50	0.90
M	0°	7°

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



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