NCP1571

Low Voltage Synchronous Buck Controller

The NCP1571 is a low voltage buck controller. It provides the control for a DC−DC power solution producing an output voltage as low as 0.980 V over a wide current range. The NCP1571−based solution is powered from 12 V with the output derived from a 2−7 V supply. It contains all required circuitry for a synchronous NFET buck regulator using the $V^{2\,™}$ control method to achieve the fastest possible transient response and best overall regulation. NCP1571 operates at a fixed internal 200 kHz frequency and is packaged in an SOIC−8.

This device provides undervoltage lockout protection, Soft−Start, Power Good with delay, and built−in adaptive non−overlap. During undervoltage lockout, the NCP1571 controller allows the power supply output to drift down, allowing the load time to shut off. This operation distinguishes the NCP1571 from other parts in its family.

Features

- Pb−Free Package is Available
- 0.980 V ± 1.0% Reference Voltage
- V^2 Control Topology
- 200 ns Transient Response
- Programmable Soft−Start
- Power Good
- Programmable Power Good Delay
- 40 ns Gate Rise and Fall Times (3.3 nF Load)
- Adaptive FET Non−Overlap Time
- Fixed 200 kHz Oscillator Frequency
- Undervoltage Lockout Holds Both Gate Outputs Low
- On/Off Control Through Use of the COMP Pin
- Overvoltage Protection through Synchronous MOSFETs
- Synchronous N−Channel Buck Design
- Dual Supply, 12 V Control, 2−7 V Power Source

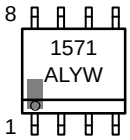
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MARKING DIAGRAM

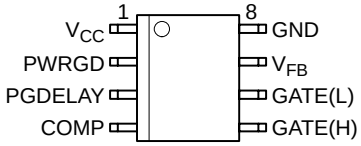


SOIC−8
D SUFFIX
CASE 751



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping†
NCP1571D	SOIC−8	98 Units/Rail
NCP1571DR2	SOIC−8	2500 Tape & Reel
NCP1571DR2G	SOIC−8 (Pb−Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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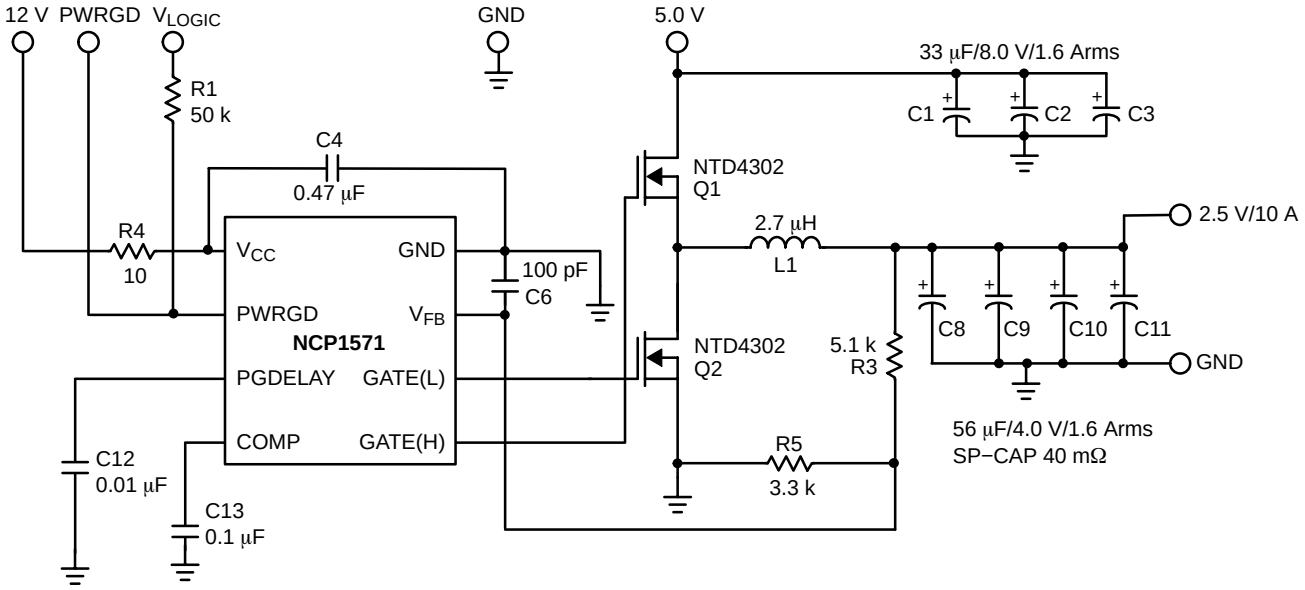


Figure 1. Applications Circuit

MAXIMUM RATINGS

Rating	Value	Unit
Operating Junction Temperature	150	°C
Storage Temperature Range	−65 to 150	°C
ESD Susceptibility (Human Body Model)	2.0	kV
Lead Temperature Soldering: Reflow: (Note 1)	230 peak	°C
Moisture Sensitivity Level	2	−
Package Thermal Resistance, SOIC−8 Junction−to−Case, $R_{\theta JC}$ Junction−to−Ambient, $R_{\theta JA}$	 48 165	 °C/W °C/W

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. 60 second maximum above 183°C.

MAXIMUM RATINGS

Pin Name	Pin Symbol	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
IC Power Input	V_{CC}	15 V	−0.5 V	N/A	1.5 A Peak 450 mA DC
Compensation Capacitor	COMP	6.0 V	−0.5 V	10 mA	10 mA
Voltage Feedback Input	V_{FB}	6.0 V	−0.5 V	1.0 mA	1.0 mA
Power Good Output	PWRGD	15 V	−0.5 V	1.0 mA	20 mA
Power Good Delay	PGDELAY	6.0 V	−0.5 V	1.0 mA	10 mA
High−Side FET Driver	GATE(H)	15 V	−0.5 V −2.0 V for 50 ns	1.5 A Peak 200 mA DC	1.5 A Peak 200 mA DC
Low−Side FET Driver	GATE(L)	15 V	−0.5 V −2.0 V for 50 ns	1.5 A Peak 200 mA DC	1.5 A Peak 200 mA DC
Ground	GND	0.5 V	−0.5 V	1.5 A Peak 450 mA DC	N/A

ELECTRICAL CHARACTERISTICS (0°C < T_J < 125°C, 11.4 V < V_{CC} < 12.6 V, $C_{GATE(H)}$ = $C_{GATE(L)}$ = 3.3 nF, $C_{PGDELAY}$ = 0.01 μF, C_{COMP} = 0.1 μF; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Error Amplifier					
V_{FB} Bias Current	V_{FB} = 0 V	−	0.2	2.0	μA
COMP Source Current	COMP = 1.5 V, V_{FB} = 0.8 V	15	30	60	μA
COMP Sink Current	COMP = 1.5 V, V_{FB} = 1.2 V	15	30	60	μA
Reference Voltage	COMP = V_{FB} T_J < 25°C	0.970 0.965	0.980 0.980	0.990 0.995	V V
COMP Max Voltage	V_{FB} = 0.8 V	2.4	2.7	−	V
COMP Min Voltage	V_{FB} = 1.2 V	−	0.1	0.2	V
COMP Fault Discharge Current at UVLO	COMP = 1.2 V, V_{CC} = 6.9 V	0.5	1.7	−	mA
COMP Fault Discharge Threshold to Reset UVLO	−	0.1	0.25	0.3	V
Open Loop Gain	−	−	98	−	dB
Unity Gain Bandwidth	−	−	20	−	kHz
PSRR @ 1.0 kHz	−	−	70	−	dB
Output Transconductance	−	−	32	−	mmho
Output Impedance	−	−	2.5	−	MΩ
GATE(H) and GATE(L)					
Rise Time	1.0 V < GATE(L), GATE(H) < V_{CC} − 2.0 V	−	40	80	ns
Fall Time	V_{CC} − 2.0 V < GATE(L), GATE(H) < 1.0 V	−	40	80	ns
GATE(H) to GATE(L) Delay	GATE(H) < 2.0 V, GATE(L) > 2.0 V	40	60	100	ns
GATE(L) to GATE(H) Delay	GATE(L) < 2.0 V, GATE(H) > 2.0 V	40	60	100	ns
Minimum Pulse Width	GATE(X) = 4.0 V	−	250	−	ns
High Voltage (AC)	Measure GATE(L) or GATE(H) 0.5 nF < $C_{GATE(H)}$ = $C_{GATE(L)}$ < 10 nF Note 2	V_{CC} − 0.5	V_{CC}	−	V
Low Voltage (AC)	Measure GATE(L) or GATE(H) 0.5 nF < $C_{GATE(H)}$ = $C_{GATE(L)}$ < 10 nF Note 2	−	0	0.5	V
GATE(H)/(L) Pulldown	Resistance to GND. Note 2	20	50	115	kΩ
Power Good					
Lower Threshold, V_O Rising	 T_J < 25°C	0.852 0.847	0.882 0.882	0.912 0.917	V V
Lower Threshold, V_O Falling	 T_J < 25°C	0.663 0.658	0.685 0.685	0.709 0.714	V V
PWRGD Low Voltage	I_{SINK} = 1.0 mA, V_{FB} = 0 V	−	0.15	0.4	V
Delay Charge Current	PGDELAY = 2.0 V	7.0	12	18	μA
Delay Clamp Voltage	−	3.45	4.0	4.3	V
Delay Charge Threshold	Ramp PGDELAY, Monitor PWRGD	3.1	3.3	3.5	V
Delay Discharge Current at UVLO	PGDELAY = 0.5 V, V_{CC} = 6.9 V	0.5	2.0	−	mA

2. Guaranteed by design. Not tested in production.

ELECTRICAL CHARACTERISTICS (continued) ($0°C < T_J < 125°C$, $11.4\ V < V_{CC} < 12.6\ V$, $C_{GATE(H)} = C_{GATE(L)} = 3.3\ nF$, $C_{PGDELAY} = 0.01\ \mu F$, $C_{COMP} = 0.1\ \mu F$; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Power Good					
Delay Discharge Threshold to Reset UVLO	PGDELAY = 0.5 V, V_{CC} = 12 V to 6.9 to 12 V, Ramp PGDELAY to 0.1 V, Monitor I (PGDELAY)	0.1	0.25	0.3	V
"Good" Signal Delay	With 0.01 μF. Note 3	1.0	3.0	5.0	ms
PWM Comparator					
PWM Comparator Offset	V_{FB} = 0 V, Increase COMP Until GATE(H) Starts Switching	0.475	0.525	0.575	V
Ramp Max Duty Cycle	–	–	80	–	%
Artificial Ramp	Duty Cycle = 50%	18	25	35	mV
Transient Response	COMP = 1.5 V, V_{FB} 20 mV Overdrive. Note 3	–	200	300	ns
V_{FB} Input Range	Note 3	0	–	1.4	V
Oscillator					
Switching Frequency	–	150	200	250	kHz
General Electrical Specifications					
V_{CC} Supply Current	COMP = 0 V (No Switching)	–	10	15	mA
Start Threshold	GATE(H) Switching, COMP Charging	8.0	8.5	9.0	V
Stop Threshold	GATE(H) Not Switching, COMP Discharging	7.0	7.5	8.0	V
Hysteresis	Start − Stop	0.75	1.0	1.25	V

3. Guaranteed by design. Not tested in production.

PACKAGE PIN DESCRIPTION

PACKAGE PIN #	PIN SYMBOL	FUNCTION
1	V_{CC}	Power supply input.
2	PWRGD	Open collector output goes low when V_{FB} is out of regulation. User must externally limit current into this pin to less than 20 mA.
3	PGDELAY	External capacitor programs PWRGD low−to−high transition delay.
4	COMP	Error amp output. PWM comparator reference input. A capacitor to LGND provides error amp compensation and Soft−Start. Pulling pin < 0.475 V locks gate outputs to a zero percent duty cycle state.
5	GATE(H)	High−side switch FET driver pin. Capable of delivering peak currents of 1.5 A.
6	GATE(L)	Low−side synchronous FET driver pin. Capable of delivering peak currents of 1.5 A.
7	V_{FB}	Error amplifier and PWM comparator input.
8	GND	Power supply return.

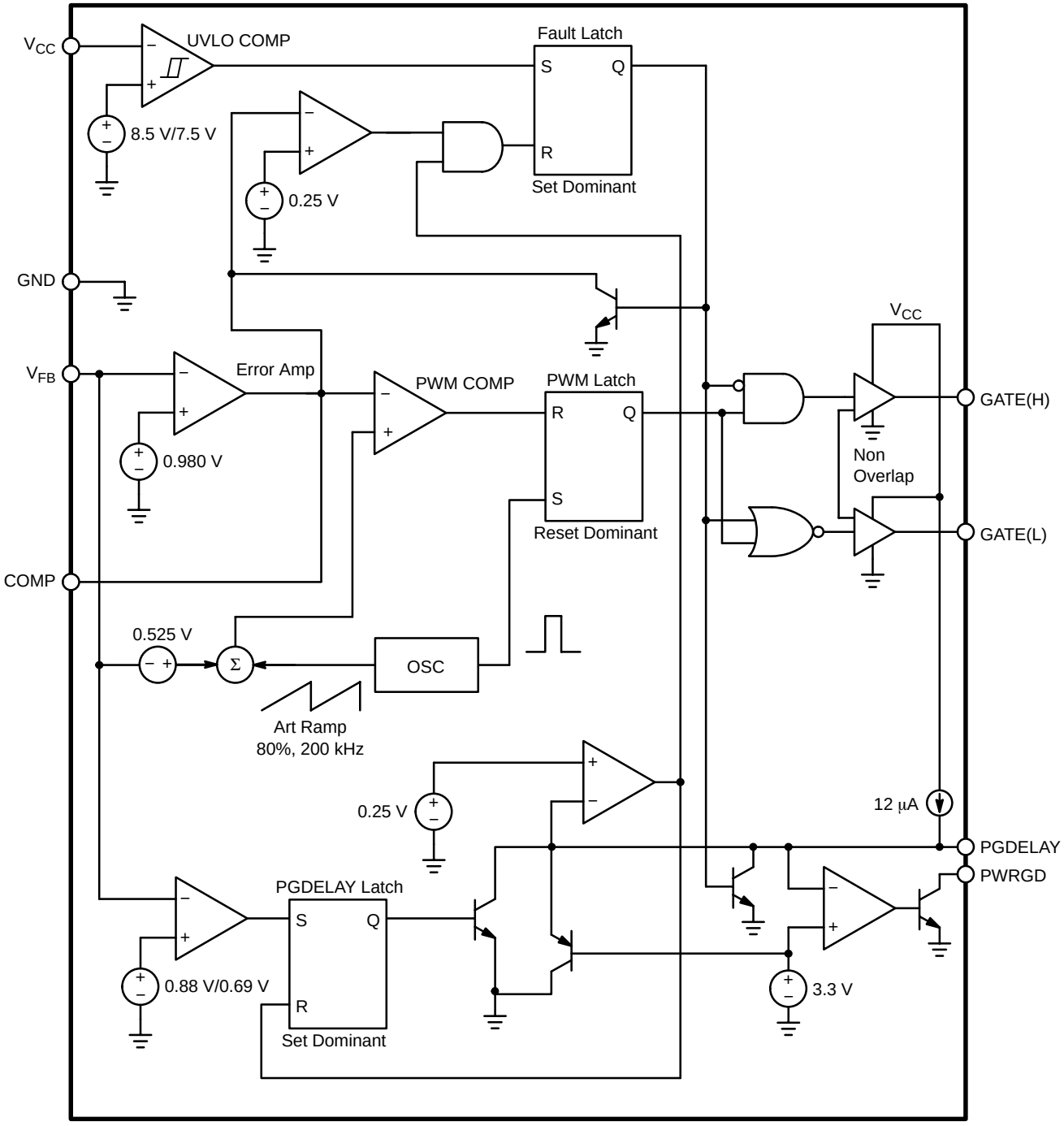


Figure 2. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

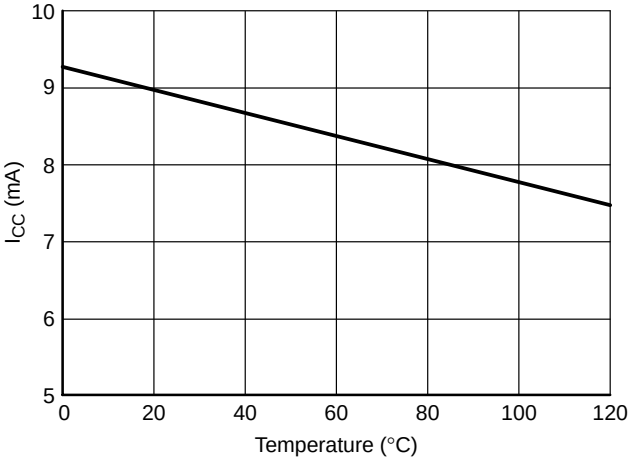


Figure 3. Supply Current vs. Temperature

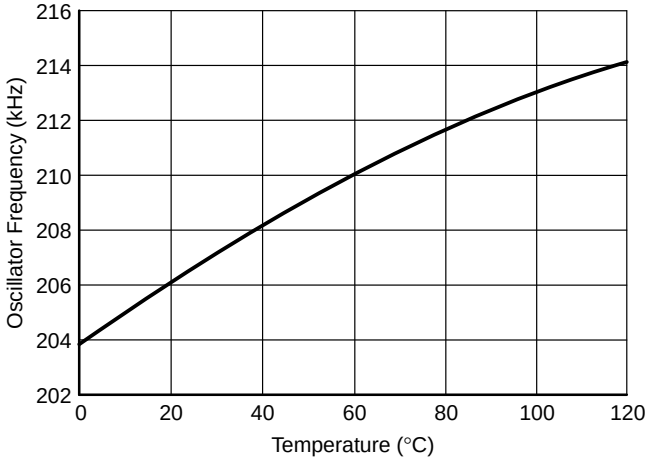


Figure 4. Oscillator Frequency vs. Temperature

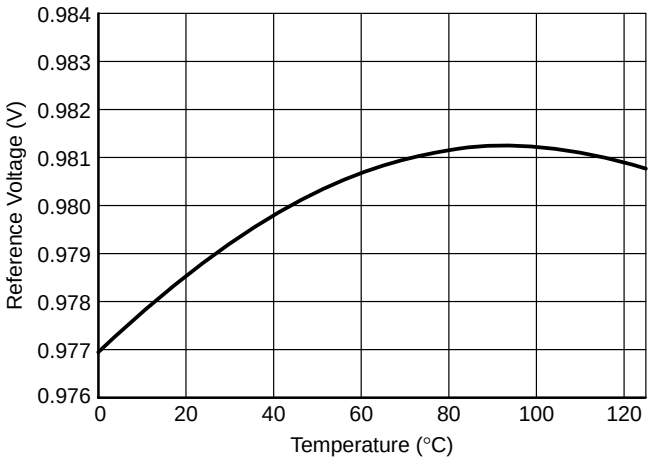


Figure 5. Reference Voltage vs. Temperature

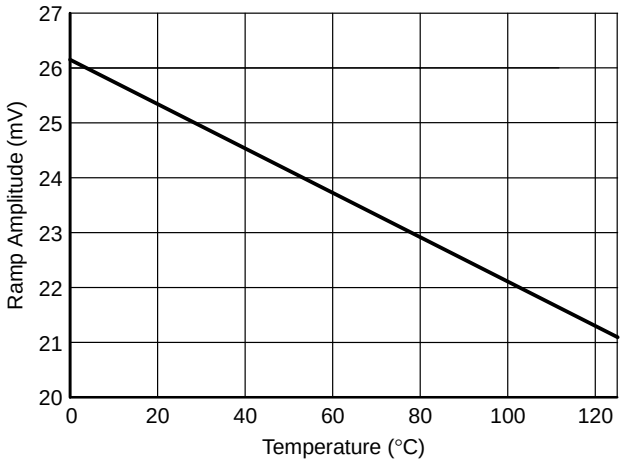


Figure 6. Artificial Ramp Amplitude vs. Temperature (50% Duty Cycle)

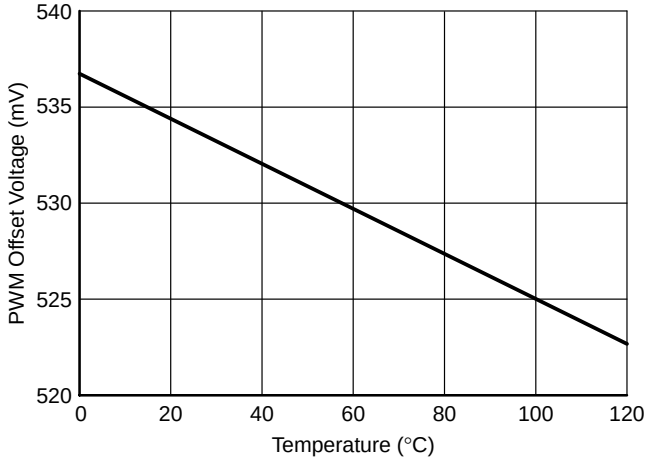


Figure 7. PWM Offset Voltage vs. Temperature

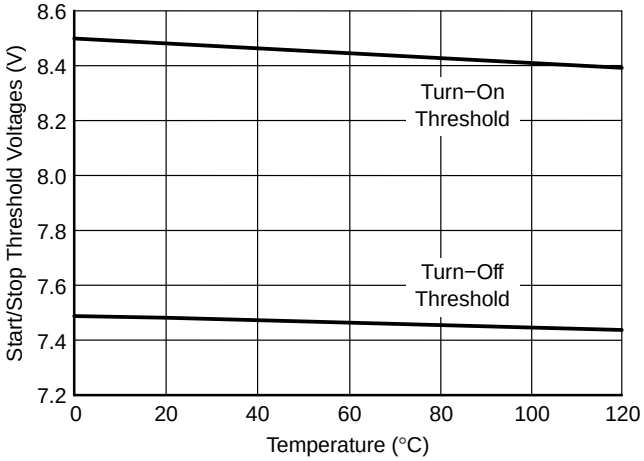


Figure 8. Undervoltage Lockout Thresholds vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

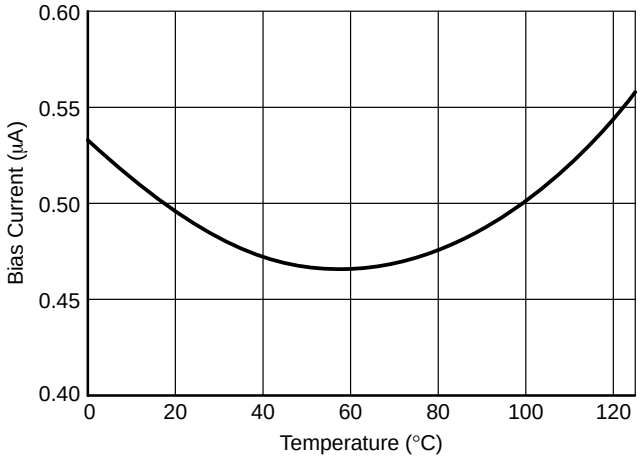


Figure 9. V_{FB} Bias Current vs. Temperature

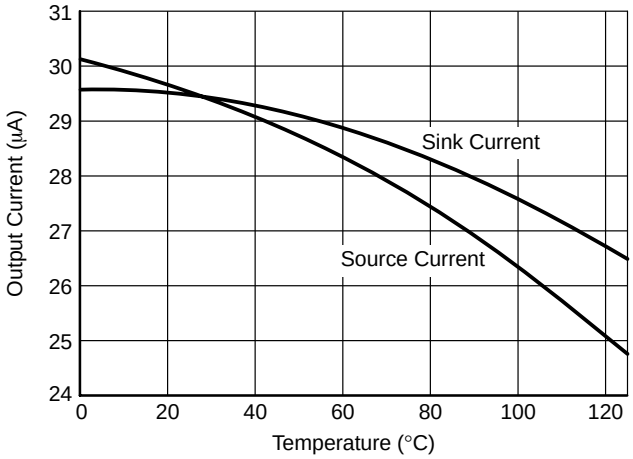


Figure 10. Error Amp Output Currents vs. Temperature

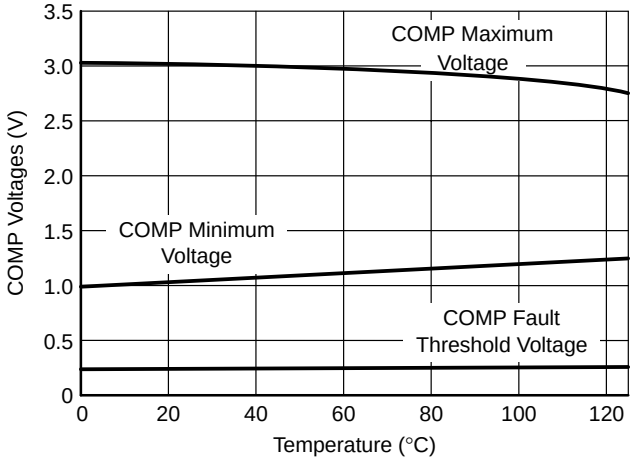


Figure 11. COMP Voltages vs. Temperature

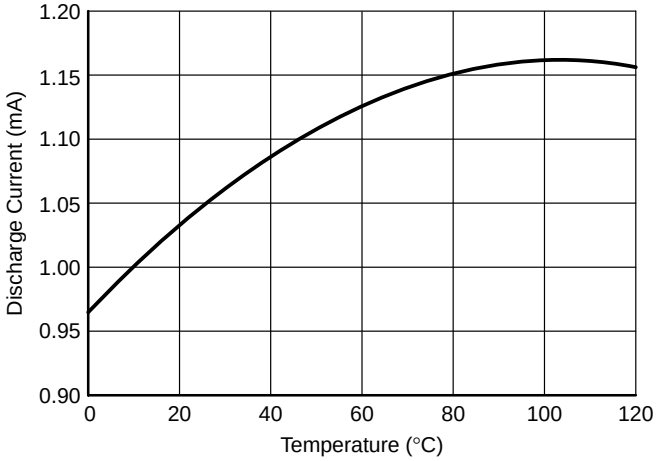


Figure 12. COMP Fault Mode Discharge Current vs. Temperature

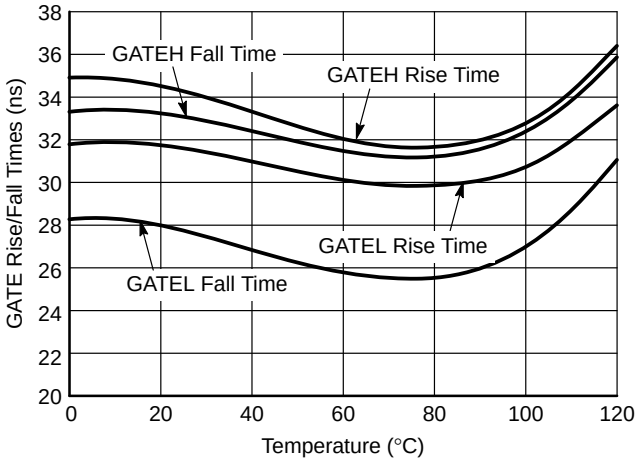


Figure 13. GATE Output Rise and Fall Times vs. Temperature

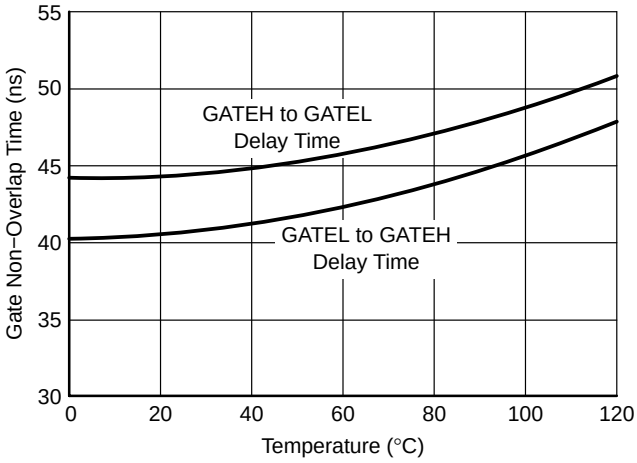


Figure 14. GATE Non−Overlap Times vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

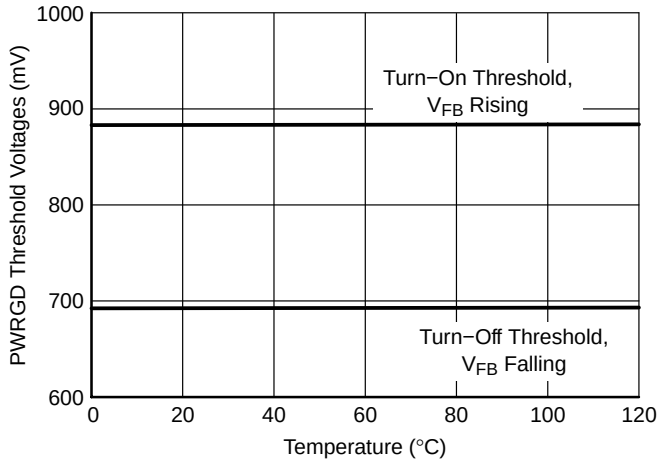


Figure 15. PWRGD Thresholds vs. Temperature

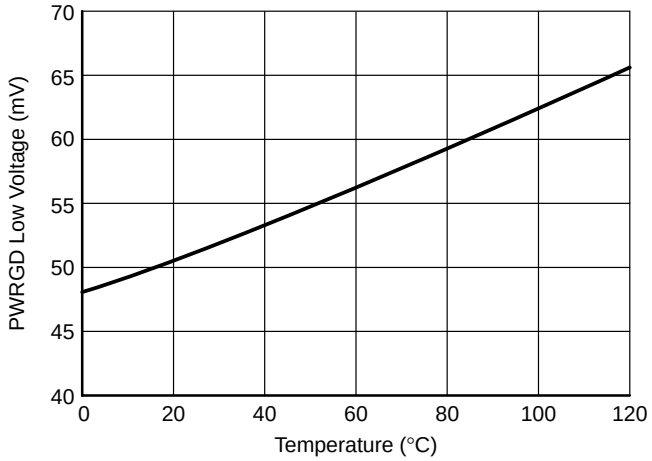


Figure 16. PWRGD Output Low Voltage vs. Temperature

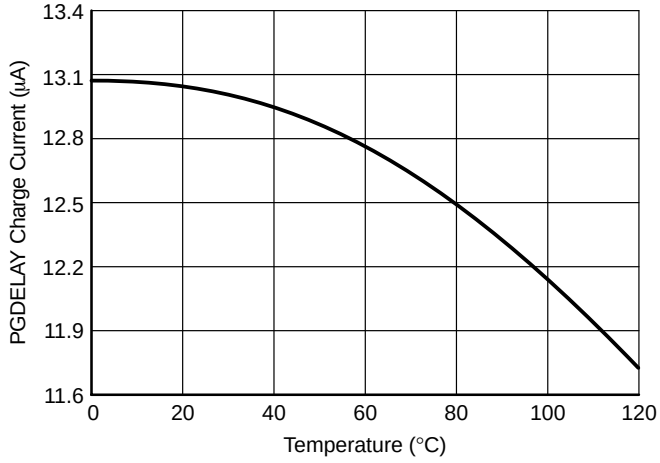


Figure 17. PGDELAY Charge Current vs. Temperature

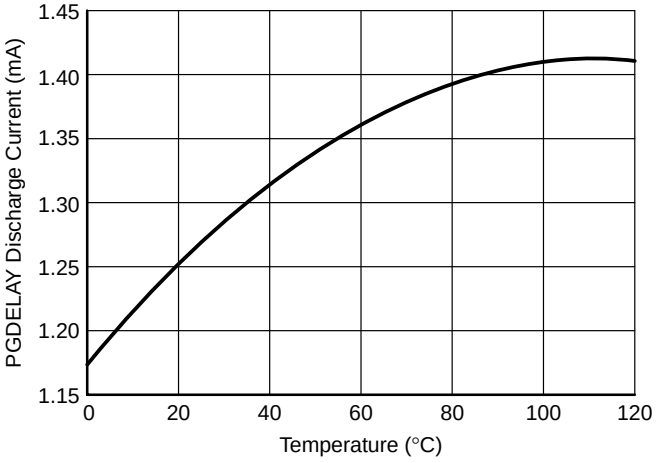


Figure 18. PGDELAY Discharge Current vs. Temperature

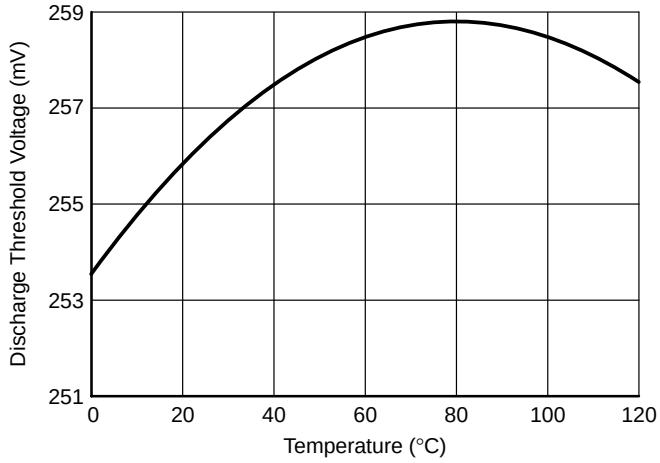


Figure 19. PGDELAY Discharge Threshold Voltage vs. Temperature

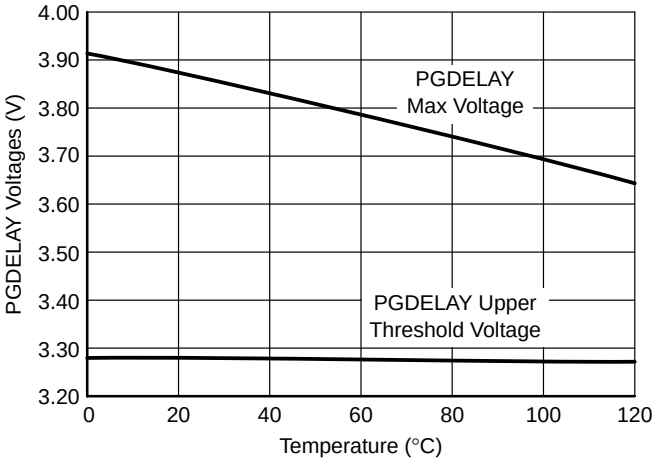


Figure 20. PGDELAY Voltages vs. Temperature

APPLICATION INFORMATION

THEORY OF OPERATION

The NCP1571 is a simple, synchronous, fixed−frequency, low−voltage buck controller using the V^2 control method. It provides a programmable−delay Power Good function to indicate when the output voltage is out of regulation.

V^2 Control Method

The V^2 control method uses a ramp signal generated by the ESR of the output capacitors. This ramp is proportional to the AC current through the main inductor and is offset by the DC output voltage. This control scheme inherently compensates for variation in either line or load conditions, since the ramp signal is generated from the output voltage itself. The V^2 method differs from traditional techniques such as voltage mode control, which generates an artificial ramp, and current mode control, which generates a ramp using the inductor current.

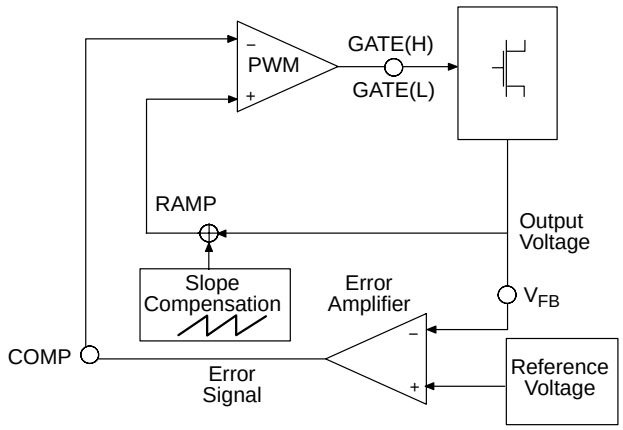


Figure 21. V^2 Control with Slope Compensation

The V^2 control method is illustrated in Figure 21. The output voltage generates both the error signal and the ramp signal. Since the ramp signal is simply the output voltage, it is affected by any change in the output, regardless of the origin of that change. The ramp signal also contains the DC portion of the output voltage, allowing the control circuit to drive the main switch from 0% to 100% duty cycle as required.

A variation in line voltage changes the current ramp in the inductor, which causes the V^2 control scheme to compensate the duty cycle. Since any variation in inductor current modifies the ramp signal, as in current mode control, the V^2 control scheme offers the same advantages in line transient response.

A variation in load current will affect the output voltage, modifying the ramp signal. A load step immediately changes the state of the comparator output, which controls the main switch. The comparator response time and the transition speed of the main switch determine the load transient response. Unlike traditional control methods, the reaction time to the output load step is not related to the crossover frequency of the error signal loop.

The error signal loop can have a low crossover frequency, since the transient response is handled by the ramp signal loop. The main purpose of this ‘slow’ feedback loop is to provide DC accuracy. Noise immunity is significantly improved, since the error amplifier bandwidth can be rolled off at a low frequency. Enhanced noise immunity improves remote sensing of the output voltage, since the noise associated with long feedback traces can be effectively filtered.

Line and load regulation are drastically improved because there are two independent control loops. A voltage mode controller relies on the change in the error signal to compensate for a deviation in either line or load voltage. This change in the error signal causes the output voltage to change corresponding to the gain of the error amplifier, which is normally specified as line and load regulation. A current mode controller maintains a fixed error signal during line transients, since the slope of the ramp signal changes in this case. However, regulation of load transients still requires a change in the error signal. The V^2 method of control maintains a fixed error signal for both line and load variation, since the ramp signal is affected by both line and load.

The stringent load transient requirements of modern microprocessors require the output capacitors to have very low ESR. The resulting shallow slope in the output ripple can lead to pulse width jitter and variation caused by both random and synchronous noise. A ramp waveform generated in the oscillator is added to the ramp signal from the output voltage to provide the proper voltage ramp at the beginning of each switching cycle. This slope compensation increases the noise immunity, particularly at duty cycles above 50%.

Startup

The NCP1571 features a programmable Soft−Start function, which is implemented through the error amplifier and the external compensation capacitor. This feature prevents stress to the power components and limits output voltage overshoot during startup. As power is applied to the regulator, the NCP1571 undervoltage lockout circuit (UVL) monitors the IC’s supply voltage (V_{CC}). The UVL circuit holds both gate outputs low until V_{CC} exceeds the 8.5 V threshold. A hysteresis function of 1.0 V improves noise immunity. The compensation capacitor connected to the COMP pin is charged by a 30 μA current source. When the capacitor voltage exceeds the 0.525 V offset of the PWM comparator, the PWM control loop will allow switching to occur. The upper gate driver GATE(H) is activated, turning on the upper MOSFET. The current ramps up through the main inductor and linearly powers the output capacitors and load. When the regulator output voltage exceeds the COMP pin voltage minus the 0.525 V PWM comparator offset threshold and the artificial ramp, the PWM comparator terminates the initial pulse.

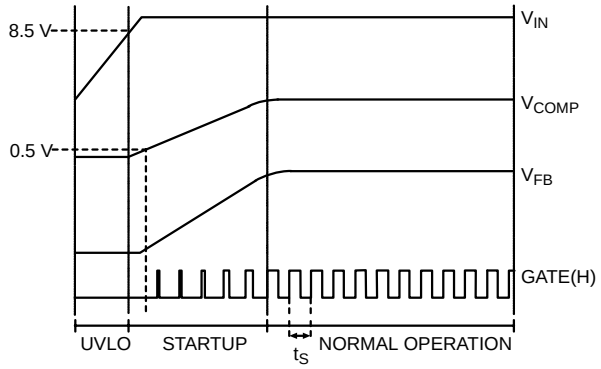


Figure 22. Idealized Waveforms

Normal Operation

During normal operation, the duty cycle of the gate drivers remains approximately constant as the V^2 control loop maintains the regulated output voltage under steady state conditions. Variations in supply line or output load conditions will result in changes in duty cycle to maintain regulation.

Input Supplies

The NCP1571 can be used in applications where a 12 V supply is available along with a lower voltage supply. Often the lower voltage supply is 5 V, but it can be any voltage less than the 12 V supply minus the required gate drive voltage of the top MOSFET. The greater the difference between the two voltages, the better the efficiency due to increasing V_{GS} available to turn on the upper MOSFET. In order to maintain power supply stability, the lower supply voltage should be at least 1.5 times the desired voltage.

A lower supply voltage between 2−7 V is recommended.

Gate Charge Effect on Switching Times

When using the onboard gate drivers, the gate charge has an important effect on the switching times of the FETs. A finite amount of time is required to charge the effective capacitor seen at the gate of the FET. Therefore, the rise and fall times rise linearly with increased capacitive loading.

Transient Response

The 200 ns reaction time of the control loop provides fast transient response to any variations in input voltage and output current. Pulse−by−pulse adjustment of duty cycle is provided to quickly ramp the inductor current to the required level. Since the inductor current cannot be changed instantaneously, regulation is maintained by the output capacitors during the time required to slew the inductor current. For better transient response, several high frequency and bulk output capacitors are usually used.

Overvoltage Protection

Overvoltage protection is provided as a result of the normal operation of the V^2 control method and requires no additional external components. The control loop responds to an overvoltage condition within 200 ns, turning off the upper MOSFET and disconnecting the regulator from its input voltage. This results in a crowbar action to clamp the output voltage, preventing damage to the load. The regulator remains in this state until the overvoltage condition ceases.

Power Good

The PWRGD pin is asserted when the output voltage is within regulation limits. Sensing for the PWRGD pin is achieved through the V_{FB} pin. When the output voltage is rising, PWRGD goes high at 90% of the designed output voltage. When the output voltage is falling, PWRGD goes low at 70% of the designed output voltage. PWRGD is an open−collector output and should be externally pulled to logic high through a resistor to limit current to no more than 20 mA. Figure 23 shows the hysteretic nature of the PWRGD pin's operation.

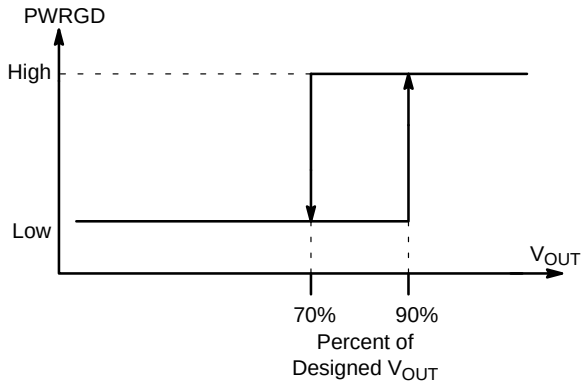


Figure 23. PWRGD Assertion

Shutdown

When the input voltage connected to V_{CC} falls through the lower threshold of the UVLO comparator, a fault latch is set. The fault latch provides a signal that forces both GATE(H) and GATE(L) into their logic low state, producing a high−impedance output at the converter switch node. At the same time, the latch also turns on two transistors which pull down on the COMP and PGDELAY pins, quickly discharging their external capacitors, and allowing PWRGD to fall.

CONVERTER DESIGN

Selection of the Output Capacitors

These components must be selected and placed carefully to yield optimal results. Capacitors should be chosen to provide acceptable ripple on the regulator output voltage. Key specifications for output capacitors are their ESR Equivalent Series Resistance (ESR), and Equivalent Series Inductance (ESL). For best transient response, a combination of low value/high frequency and bulk capacitors placed close to the load will be required.

In order to determine the number of output capacitors the maximum voltage transient allowed during load transitions has to be specified. The output capacitors must hold the output voltage within these limits since the inductor current

can not change with the required slew rate. The output capacitors must therefore have a very low ESL and ESR.

The voltage change during the load current transient is:

$$\Delta V_{OUT} = \Delta I_{OUT} \times \left(\frac{ESL}{\Delta t} + ESR + \frac{t_{TR}}{C_{OUT}} \right)$$

where:

$\Delta I_{OUT} / \Delta t$ = load current slew rate;

ΔI_{OUT} = load transient;

Δt = load transient duration time;

ESL = Maximum allowable ESL including capacitors, circuit traces, and vias;

ESR = Maximum allowable ESR including capacitors and circuit traces;

t_{TR} = output voltage transient response time.

The designer has to independently assign values for the change in output voltage due to ESR, ESL, and output capacitor discharging or charging. Empirical data indicates that most of the output voltage change (droop or spike depending on the load current transition) results from the total output capacitor ESR.

The maximum allowable ESR can then be determined according to the formula:

$$ESR_{MAX} = \frac{\Delta V_{ESR}}{\Delta I_{OUT}}$$

where:

ΔV_{ESR} = change in output voltage due to ESR (assigned by the designer)

Once the maximum allowable ESR is determined, the number of output capacitors can be found by using the formula:

$$\text{Number of capacitors} = \frac{ESR_{CAP}}{ESR_{MAX}}$$

where:

ESR_{CAP} = maximum ESR per capacitor (specified in manufacturer's data sheet).

ESR_{MAX} = maximum allowable ESR.

The actual output voltage deviation due to ESR can then be verified and compared to the value assigned by the designer:

$$\Delta V_{ESR} = \Delta I_{OUT} \times ESR_{MAX}$$

Similarly, the maximum allowable ESL is calculated from the following formula:

$$ESL_{MAX} = \frac{\Delta V_{ESL} \times \Delta t}{\Delta I}$$

Selection of the Input Inductor

A common requirement is that the buck controller must not disturb the input voltage. One method of achieving this is by using an input inductor and a bypass capacitor. The input inductor isolates the supply from the noise generated in the switching portion of the buck regulator and also limits the inrush current into the input capacitors upon power up. The inductor's limiting effect on the input current slew rate becomes increasingly beneficial during load transients. The worst case is when the load changes from no load to full load (load step), a condition under which the highest voltage change across the input capacitors is also seen by the input inductor. The inductor successfully blocks the ripple current while placing the transient current requirements on the input bypass capacitor bank, which has to initially support the sudden load change.

The minimum inductance value for the input inductor is therefore:

$$L_{IN} = \frac{\Delta V}{(dI/dt)_{MAX}}$$

where:

L_{IN} = input inductor value;

ΔV = voltage seen by the input inductor during a full load swing;

$(dI/dt)_{MAX}$ = maximum allowable input current slew rate.

The designer must select the LC filter pole frequency so that at least 40 dB attenuation is obtained at the regulator switching frequency. The LC filter is a double−pole network with a slope of −2.0, a roll−off rate of −40 dB/dec, and a corner frequency:

$$f_C = \frac{1}{2\pi \times \sqrt{LC}}$$

where:

L = input inductor;

C = input capacitor(s).

Selection of the Output Inductor

There are many factors to consider when choosing the output inductor. Maximum load current, core and winding losses, ripple current, short circuit current, saturation characteristics, component height and cost are all variables that the designer should consider. However, the most important consideration may be the effect inductor value has on transient response.

The amount of overshoot or undershoot exhibited during a current transient is defined as the product of the current step and the output filter capacitor ESR. Choosing the inductor value appropriately can minimize the amount of energy that must be transferred from the inductor to the capacitor or vice−versa. In the subsequent paragraphs, we will determine the minimum value of inductance required for our system and consider the trade−off of ripple current vs. transient response.

In order to choose the minimum value of inductance, input voltage, output voltage and output current must be known. Most computer applications use reasonably well regulated bulk power supplies so that, while the equations below specify $V_{IN(MAX)}$ or $V_{IN(MIN)}$, it is possible to use the nominal value of V_{IN} in these calculations with little error.

Current in the inductor while operating in the continuous current mode is defined as the load current plus ripple current.

$$I_L = I_{LOAD} + I_{RIPPLE}$$

The ripple current waveform is triangular, and the current is a function of voltage across the inductor, switch FET on−time and the inductor value. FET on−time can be defined as the product of duty cycle and switch frequency, and duty cycle can be defined as a ratio of V_{OUT} to V_{IN}. Thus,

$$I_{RIPPLE} = \frac{(V_{IN} - V_{OUT})V_{OUT}}{(f_{OSC})(L)(V_{IN})}$$

Peak inductor current is defined as the load current plus half of the peak current. Peak current must be less than the maximum rated FET switch current, and must also be less than the inductor saturation current. Thus, the maximum output current can be defined as:

$$I_{OUT(MAX)} = I_{SWITCH(MAX)} - \frac{(V_{IN(MAX)} - V_{OUT})V_{OUT}}{(2)(f_{OSC})(L)(V_{IN(MAX)})}$$

Since the maximum output current must be less than the maximum switch current, the minimum inductance required can be determined.

$$L_{(MIN)} = \frac{(V_{IN(MIN)} - V_{OUT})V_{OUT}}{(f_{OSC})(I_{SWITCH(MAX)})(V_{IN(MIN)})}$$

This equation identifies the value of inductor that will provide the full rated switch current as inductor ripple current, and will usually result in inefficient system operation. The system will sink current away from the load during some portion of the duty cycle unless load current is greater than half of the rated switch current. Some value larger than the minimum inductance must be used to ensure the converter does not sink current. Choosing larger values of inductor will reduce the ripple current, and inductor value can be designed to accommodate a particular value of ripple current by replacing $I_{SWITCH(MAX)}$ with a desired value of I_{RIPPLE}:

$$L_{(RIPPLE)} = \frac{(V_{IN(MIN)} - V_{OUT})V_{OUT}}{(f_{OSC})(I_{RIPPLE})(V_{IN(MIN)})}$$

However, reducing the ripple current will cause transient response times to increase. The response times for both increasing and decreasing current steps are shown below.

$$T_{RESPONSE(INCREASING)} = \frac{(L)(\Delta I_{OUT})}{(V_{IN} - V_{OUT})}$$

$$T_{RESPONSE(DECREASING)} = \frac{(L)(\Delta I_{OUT})}{(V_{OUT})}$$

Inductor value selection also depends on how much output ripple voltage the system can tolerate. Output ripple voltage is defined as the product of the output ripple current and the output filter capacitor ESR.

Thus, output ripple voltage can be calculated as:

$$V_{RIPPLE} = (ESR_C)(I_{RIPPLE}) = \frac{(ESR_C)(V_{IN} - V_{OUT})V_{OUT}}{(f_{OSC})(L)(V_{IN})}$$

Finally, we should consider power dissipation in the output inductors. Power dissipation is proportional to the square of inductor current:

$$P_D = (I_L^2)(ESR_L)$$

The temperature rise of the inductor relative to the air surrounding it is defined as the product of power dissipation and thermal resistance to ambient:

$$\Delta T(inductor) = (Ra)(P_D)$$

Ra for an inductor designed to conduct 20 A to 30 A is approximately 45°C/W. The inductor temperature is given as:

$$T(inductor) = \Delta T(inductor) + Tambient$$

V_{CC} Bypass Filtering

A small RC filter should be added between module V_{CC} and the V_{CC} input to the IC. A 10 Ω resistor and a 0.47 μF capacitor should be sufficient to ensure the controller IC does not operate erratically due to injected noise, and will also supply reserve charge for the onboard gate drivers.

Input Filter Capacitors

The input filter capacitors provide a charge reservoir that minimizes supply voltage variations due to changes in current flowing through the switch FETs. These capacitors must be chosen primarily for ripple current rating.

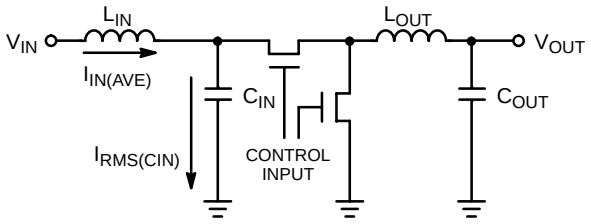


Figure 24.

Consider the schematic shown in Figure 24. The average current flowing in the input inductor L_{IN} for any given output current is:

$$I_{IN(AVE)} = I_{OUT} \times \frac{V_{OUT}}{V_{IN}}$$

Input capacitor current is positive into the capacitor when the switch FETs are off, and negative out of the capacitor when the switch FETs are on. When the switches are off, $I_{IN(AVE)}$ flows into the capacitor. When the switches are on, capacitor current is equal to the per−phase output current minus $I_{IN(AVE)}$. If we ignore the small current variation due to the output ripple current, we can approximate the input capacitor current waveform as a square wave. We can then calculate the RMS input capacitor ripple current:

$$I_{RMS(CIN)} = \sqrt{I_{IN(AVE)}^2 + \frac{V_{OUT}}{V_{IN}} \times \left[(I_{OUT\ per\ phase} - I_{IN(AVE)})^2 - I_{IN(AVE)}^2\right]}$$

The input capacitance must be designed to conduct the worst case input ripple current. This will require several capacitors in parallel. In addition to the worst case current, attention must be paid to the capacitor manufacturer's derating for operation over temperature.

As an example, let us define the input capacitance for a 5 V to 3.3 V conversion at 10 A at an ambient temperature of 60°C. Efficiency of 80% is assumed. Average input current in the input filter inductor is:

$$I_{IN(AVE)} = (10\ A)(3.3\ V/5\ V) = 6.6\ A$$

Input capacitor RMS ripple current is then

$$I_{IN(RMS)} = \sqrt{6.6^2 + \frac{3.3\ V}{5\ V} \times [(10\ A - 6.6\ A)^2 - 6.6\ A^2]}$$

$$= 4.74\ A$$

If we consider a Rubycon MBZ series capacitor, the ripple current rating for a 6.3 V, 1800 nF capacitor is 2000 mA at 100 kHz and 105°C. We determine the number of input capacitors by dividing the ripple current by the percapacitor current rating:

$$\text{Number of capacitors} = 4.74\ A/2.0\ A = 2.3$$

A total of at least 3 capacitors in parallel must be used to meet the input capacitor ripple current requirements.

Output Switch FETs

Output switch FETs must be chosen carefully, since their properties vary widely from manufacturer to manufacturer. The NCP1571 system is designed assuming that N−Channel FETs will be used. The FET characteristics of most concern are the gate charge/gate−source threshold voltage, gate capacitance, on−resistance, current rating and the thermal capability of the package.

The onboard FET driver has a limited drive capability. If the switch FET has a high gate charge, the amount of time the FET stays in its ohmic region during the turn−on and turn−off transitions is larger than that of a low gate charge FET, with the result that the high gate charge FET will consume more power. Similarly, a low on−resistance FET will dissipate less power than will a higher on−resistance FET at a given current. Thus, low gate charge and low $R_{DS(ON)}$ will result in higher efficiency and will reduce generated heat.

It can be advantageous to use multiple switch FETs to reduce power consumption. By placing a number of FETs in parallel, the effective $R_{DS(ON)}$ is reduced, thus reducing the ohmic power loss. However, placing FETs in parallel increases the gate capacitance so that switching losses increase. As long as adding another parallel FET reduces the ohmic power loss more than the switching losses increase, there is some advantage to doing so. However, at some point the law of diminishing returns will take hold, and a marginal increase in efficiency may not be worth the board area required to add the extra FET. Additionally, as more FETs are used, the limited drive capability of the FET driver will have to charge a larger gate capacitance, resulting in increased gate voltage rise and fall times. This will affect the amount of time the FET operates in its ohmic region and will increase power dissipation.

The following equations can be used to calculate power dissipation in the switch FETs.

For ohmic power losses due to $R_{DS(ON)}$:

$$P_{ON(TOP)} = \frac{(R_{DS(ON)(TOP)})(I_{RMS(TOP)})^2}{(\text{number of topside FETs})}$$

$$P_{ON(BOTTOM)} = \frac{(R_{DS(ON)(BOTTOM)})(I_{RMS(BOTTOM)})^2}{(\text{number of bottom−side FETs})}$$

where:

n = number of phases.

Note that $R_{DS(ON)}$ increases with temperature. It is good practice to use the value of $R_{DS(ON)}$ at the FET's maximum junction temperature in the calculations shown above.

$$I_{RMS(TOP)} = \sqrt{I_{PK}^2 - (I_{PK})(I_{RIPPLE}) + \frac{D}{3} I_{RIPPLE}^2}$$

$$I_{RMS(BOTTOM)} = I_{PK}^2 - (I_{PK} I_{RIPPLE}) + \frac{(1 - D)}{3} I_{RIPPLE}^2$$

$$I_{RIPPLE} = \frac{(V_{IN} - V_{OUT})(V_{OUT})}{(f_{OSC})(L)(V_{IN})}$$

$$I_{PEAK} = I_{LOAD} + \frac{I_{RIPPLE}}{2} = \frac{I_{OUT}}{3} + \frac{I_{RIPPLE}}{2}$$

where:

D = Duty cycle.

For switching power losses:

$$P_D = nCV^2(f_{OSC})$$

where:

n = number of switch FETs (either top or bottom),

C = FET gate capacitance,

V = maximum gate drive voltage (usually V_{CC}),

f_{OSC} = switching frequency.

Layout Considerations

1. The fast response time of V^2 technology increases the IC's sensitivity to noise on the V_{FB} line. Fortunately, a simple RC filter, formed by the feedback network and a small capacitor (100 pF works well, shown below as C6) placed between V_{FB} and GND, filters out most noise and provides a system practically immune to jitter. This capacitor should be located as close as possible to the IC.
2. The COMP capacitor (shown below as C13) should be connected via its own path to the IC ground. The COMP capacitor is sensitive to the intermittent ground drops caused by switching currents. A separate ground path will reduce the potential for jitter.
3. The V_{CC} bypass capacitor (0.1 μF or greater, shown below as C4) should be located as close as possible to the IC. This capacitor's connection to GND must be as short as possible. The 10 Ω resistor (shown below as R3) should be placed close to the V_{CC} pin.
4. The IC should not be placed in the path of switching currents. If a ground plane is used, care should be taken by the designer to ensure that the IC is not located over a ground or other current return path.

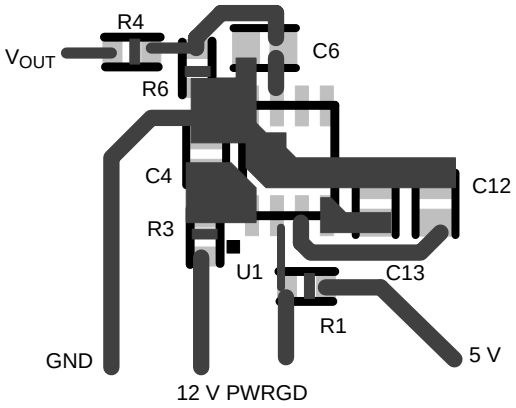


Figure 25.

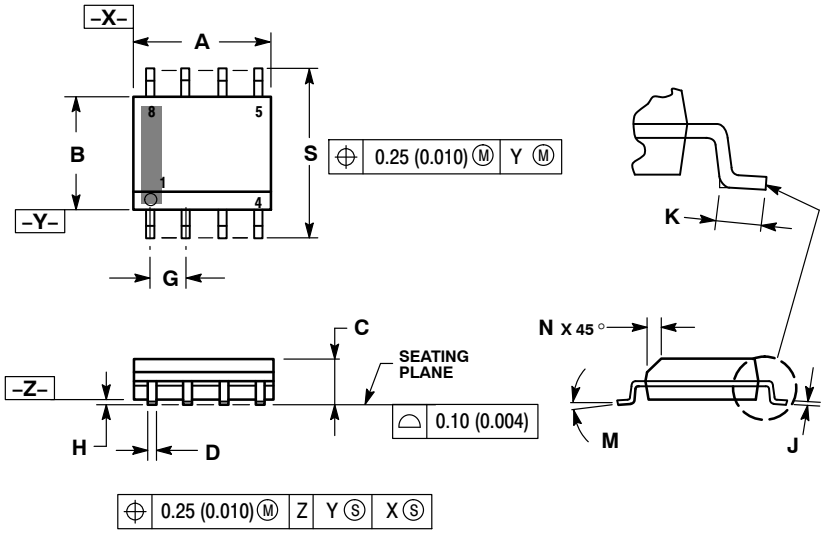
V^2 is a trademark of Switch Power, Inc.



SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

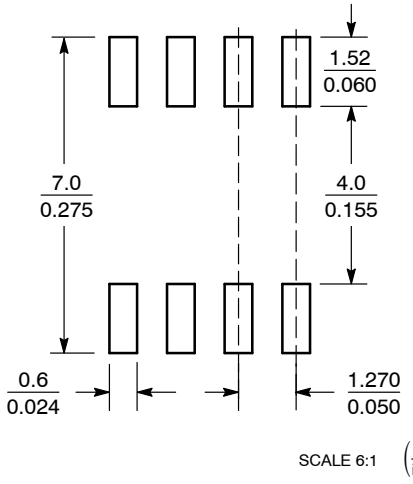
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

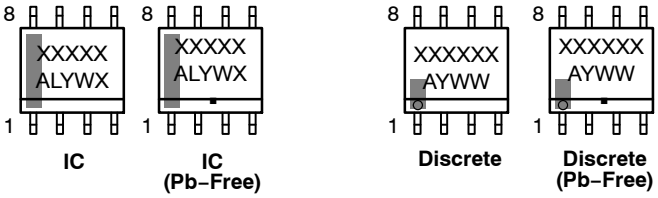
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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