LDO Regulator - Ultra-Low I_Q, CMOS

150 mA

NCP170

The NCP170 series of CMOS low dropout regulators are designed specifically for portable battery-powered applications which require ultra-low quiescent current. The ultra-low consumption of typ. 500 nA ensures long battery life and dynamic transient boost feature improves device transient response for wireless communication applications. The device is available in small 1 × 1 mm XDFN4, SOT-563 and TSOP-5 packages.

Features

- Operating Input Voltage Range: 2.2 V to 5.5 V
- Output Voltage Range: 1.2 V to 3.6 V (0.1 V Steps)
- Ultra-Low Quiescent Current Typ. 0.5 μA
- Low Dropout: 170 mV Typ. at 150 mA
- High Output Voltage Accuracy ±1%
- Stable with Ceramic Capacitors 1 μF
- Over-Current Protection
- Thermal Shutdown Protection
- NCP170A for Active Discharge Option
- Available in Small 1 × 1 mm XDFN4, SOT−563 and TSOP-5 Packages
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Battery Powered Equipments
- Portable Communication Equipments
- Cameras, Image Sensors and Camcorders

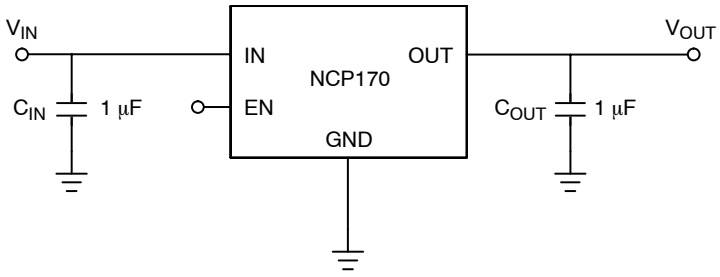
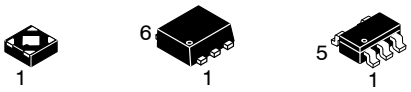


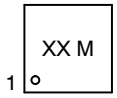
Figure 1. Typical Application Schematic



XDFN4	SOT−563	TSOP−5
MX SUFFIX	XV SUFFIX	SN SUFFIX
CASE 711AJ	CASE 463A	CASE 483

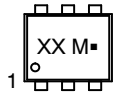
MARKING DIAGRAMS

XDFN4



XX = Specific Device Code
M = Date Code

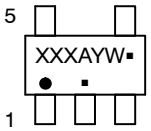
SOT−563



XX = Specific Device Code
M = Month Code
▪ = Pb-Free Package

*Pb-Free indicator, “G” or microdot “▪”, may or may not be present.

TSOP−5



XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 22 of this data sheet.

© Semiconductor Components Industries, LLC, 2017

PIN FUNCTION DESCRIPTION

Pin No. XDFN4	Pin No. SOT−563	Pin No. TSOP−5	Pin Name	Description
4	1	1	IN	Power Supply Input Voltage
2	2	2	GND	Power Supply Ground
3	6	3	EN	Chip Enable Pin (Active “H”)
1	3	5	OUT	Output Pin
EPAD	–	–	EPAD	Internally Connected to GND
–	4	4	NC	No Connect
–	5	–	GND	Power Supply Ground

ABSOLUTE MAXIMUM RATINGS

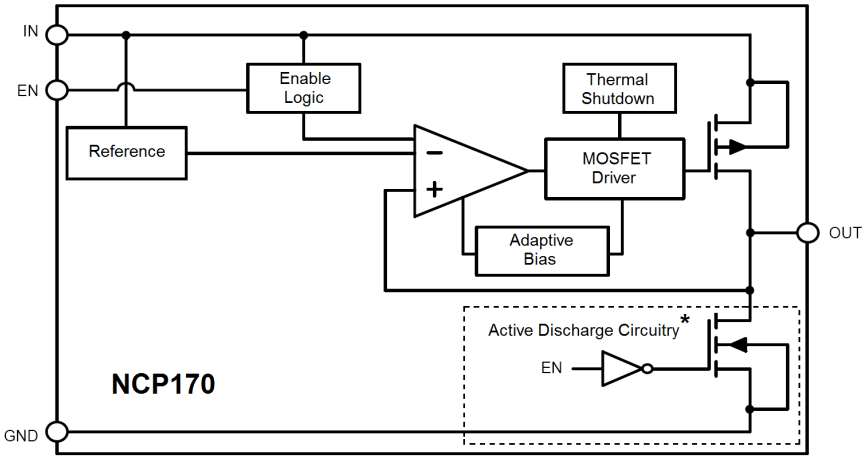
Symbol	Rating	Value	Unit
V_{IN}	Input Voltage (Note 1)	6.0	V
V_{OUT}	Output Voltage	−0.3 to V_{IN} + 0.3	V
V_{CE}	Chip Enable Input	−0.3 to 6.0	V
$T_{J(MAX)}$	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature	−55 to 150	°C
ESD_{HBM}	ESD Capability, Human Body Model (Note 2)	2000	V
ESD_{MM}	ESD Capability, Machine Model (Note 2)	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC-Q100-002 (EIA/JESD22-A114)
   ESD Machine Model tested per AEC-Q100-003 (EIA/JESD22-A115)
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78

THERMAL CHARACTERISTICS

Symbol	Rating	Value	Unit
$R_{\theta JA}$	Thermal Characteristics, Thermal Resistance, Junction-to-Air XDFN4 1 × 1 mm SOT−563 TSOP−5	 250 200 250	°C/W



* Active discharge feature is present only in NCP170AxxvvvTyG devices.

Figure 2. Simplified Block Diagram

ELECTRICAL CHARACTERISTICS – VOLTAGE VERSION 1.2 V

(–40°C ≤ T_J ≤ 85°C; V_{IN} = 2.5 V; I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 1.0 μF, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Operating Input Voltage		2.2	–	5.5	V
V_{OUT}	Output Voltage	T_A = +25°C	1.188	1.2	1.212	V
		–40°C ≤ T_J ≤ 85°C	1.176	1.2	1.224	
$Line_{Reg}$	Line Regulation	2.5 V < V_{IN} ≤ 5.5 V, I_{OUT} = 1 mA	–	0.05	0.20	%/V
$Load_{Reg}$	Load Regulation	0 mA < I_{OUT} ≤ 150 mA, V_{IN} = 2.5 V	–20	1	20	mV
V_{DO}	Dropout Voltage	(Note 4)	–	–	–	mV
I_{OUT}	Output Current	(Note 5)	150	–	–	mA
I_{SC}	Short Circuit Current Limit	V_{OUT} = 0 V	–	225	–	mA
I_Q	Quiescent Current	I_{OUT} = 0 mA	–	0.5	0.9	μA
I_{STB}	Standby Current	V_{EN} = 0 V, T_J = 25°C	–	0.1	0.5	μA
V_{ENH}	EN Pin Threshold Voltage	EN Input Voltage “H”	1.2	–	–	V
V_{ENL}	EN Pin Threshold Voltage	EN Input Voltage “L”	–	–	0.4	V
I_{EN}	EN Pin Current	V_{EN} ≤ V_{IN} ≤ 5.5 V (Note 6)	–	10	–	nA
PSRR	Power Supply Rejection Ratio	f = 1 kHz, V_{IN} = 2.2 V + 200 mVpp Modulation I_{OUT} = 150 mA I_{OUT} = 10 mA	 – –	 57 63	 – –	dB
V_{NOISE}	Output Noise Voltage	V_{IN} = 5.5 V, I_{OUT} = 1 mA, f = 100 Hz to 1 MHz, C_{OUT} = 1 μF	–	85	–	μV_{rms}
R_{LOW}	Active Output Discharge Resistance (A option only)	V_{IN} = 5.5 V, V_{EN} = 0 V (Note 6)	–	100	–	Ω
T_{SD}	Thermal Shutdown Temperature	Temperature Increasing from T_J = +25°C (Note 6)	–	175	–	°C
T_{SDH}	Thermal Shutdown Hysteresis	Temperature Falling from T_{SD} (Note 6)	–	25	–	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Performance guaranteed over the indicated operating temperature range by design and/or characterization production tested at T_J = T_A = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
4. Not Characterized at V_{IN} = 2.2 V, V_{OUT} = 1.2 V, I_{OUT} = 150 mA.
5. Respect SOA.
6. Guaranteed by design and characterization.

ELECTRICAL CHARACTERISTICS – VOLTAGE VERSION 1.5 V

(–40°C ≤ T_J ≤ 85°C; V_{IN} = 2.5 V; I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 1.0 μF, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 7)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Operating Input Voltage		2.2	–	5.5	V
V_{OUT}	Output Voltage	T_A = +25°C	1.485	1.5	1.515	V
		–40°C ≤ T_J ≤ 85°C	1.470	1.5	1.530	
$Line_{Reg}$	Line Regulation	4.3 V < V_{IN} ≤ 5.5 V, I_{OUT} = 1 mA	–	0.05	0.20	%/V
$Load_{Reg}$	Load Regulation	0 mA < I_{OUT} ≤ 150 mA, V_{IN} = 4.3 V	–20	–	20	mV
V_{DO}	Dropout Voltage	I_{OUT} = 150 mA (Note 8)	–	–	–	mV
I_{OUT}	Output Current	(Note 9)	150	–	–	mA
I_{SC}	Short Circuit Current Limit	V_{OUT} = 0 V	–	225	–	mA
I_Q	Quiescent Current	I_{OUT} = 0 mA	–	0.5	0.9	μA
I_{STB}	Standby Current	V_{EN} = 0 V, T_J = 25°C	–	0.1	0.5	μA
V_{ENH}	EN Pin Threshold Voltage	EN Input Voltage “H”	1.2	–	–	V
V_{ENL}	EN Pin Threshold Voltage	EN Input Voltage “L”	–	–	0.4	V
I_{EN}	EN Pin Current	V_{EN} ≤ V_{IN} ≤ 5.5 V (Note 10)	–	10	–	nA
PSRR	Power Supply Rejection Ratio	f = 1 kHz, V_{IN} = 2.5 V + 200 mVpp Modulation I_{OUT} = 150 mA	–	57	–	dB
V_{NOISE}	Output Noise Voltage	V_{IN} = 5.5 V, I_{OUT} = 1 mA, f = 100 Hz to 1 MHz, C_{OUT} = 1 μF	–	90	–	μV_{rms}
R_{LOW}	Active Output Discharge Resistance (A option only)	V_{IN} = 5.5 V, V_{EN} = 0 V (Note 10)	–	100	–	Ω
T_{SD}	Thermal Shutdown Temperature	Temperature Increasing from T_J = +25°C (Note 10)	–	175	–	°C
T_{SDH}	Thermal Shutdown Hysteresis	Temperature Falling from T_{SD} (Note 10)	–	25	–	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Performance guaranteed over the indicated operating temperature range by design and/or characterization production tested at T_J = T_A = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
8. Not Characterized at V_{IN} = 2.2 V, V_{OUT} = 1.5 V, I_{OUT} = 150 mA.
9. Respect SOA.
10. Guaranteed by design and characterization.

ELECTRICAL CHARACTERISTICS – VOLTAGE VERSION 1.8 V

(–40°C ≤ T_J ≤ 85°C; V_{IN} = 2.8 V; I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 1.0 μF, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 11)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Operating Input Voltage		2.2	–	5.5	V
		I_{OUT} < 30 mA	2.0	–	5.5	
V_{OUT}	Output Voltage	T_A = +25°C	1.782	1.8	1.818	V
		–40°C ≤ T_J ≤ 85°C	1.764	1.8	1.836	
$Line_{Reg}$	Line Regulation	2.8 V < V_{IN} ≤ 5.5 V, I_{OUT} = 1 mA	–	0.05	0.20	%/V
$Load_{Reg}$	Load Regulation	0 mA < I_{OUT} ≤ 150 mA, V_{IN} = 2.8 V	–20	1	20	mV
V_{DO}	Dropout Voltage	I_{OUT} = 150 mA (Note 12)	–	350	480	mV
I_{OUT}	Output Current	(Note 13)	150	–	–	mA
I_{SC}	Short Circuit Current Limit	V_{OUT} = 0 V	–	225	–	mA
I_Q	Quiescent Current	I_{OUT} = 0 mA	–	0.5	0.9	μA
I_{STB}	Standby Current	V_{EN} = 0 V, T_J = 25°C	–	0.1	0.5	μA
V_{ENH}	EN Pin Threshold Voltage	EN Input Voltage “H”	1.2	–	–	V
V_{ENL}	EN Pin Threshold Voltage	EN Input Voltage “L”	–	–	0.4	V
I_{EN}	EN Pull Down Current	V_{EN} ≤ V_{IN} ≤ 5.5 V (Note 14)	–	10	–	nA
PSRR	Power Supply Rejection Ratio	f = 1 kHz, V_{IN} = 2.8 V + 200 mVpp Modulation I_{OUT} = 150 mA	–	57	–	dB
V_{NOISE}	Output Noise Voltage	V_{IN} = 5.5 V, I_{OUT} = 1 mA f = 100 Hz to 1 MHz, C_{OUT} = 1 μF	–	95	–	μV_{rms}
R_{LOW}	Active Output Discharge Resistance (A option only)	V_{IN} = 5.5 V, V_{EN} = 0 V (Note 14)	–	100	–	Ω
T_{SD}	Thermal Shutdown Temperature	Temperature Increasing from T_J = +25°C (Note 14)	–	175	–	°C
T_{SDH}	Thermal Shutdown Hysteresis	Temperature Falling from T_{SD} (Note 14)	–	25	–	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

11. Performance guaranteed over the indicated operating temperature range by design and/or characterization production tested at T_J = T_A = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
12. Characterized when V_{OUT} falls 54 mV below the regulated voltage and only for devices with V_{OUT} = 1.8 V.
13. Respect SOA.
14. Guaranteed by design and characterization.

ELECTRICAL CHARACTERISTICS – VOLTAGE VERSION 1.9 V

(−40°C ≤ T_J ≤ 85°C; V_{IN} = 2.9 V; I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 1.0 μF, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 15)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Operating Input Voltage		2.2	–	5.5	V
V_{OUT}	Output Voltage	T_A = +25°C	1.881	1.9	1.919	V
		−40°C ≤ T_J ≤ 85°C	1.862	1.9	1.938	
$Line_{Reg}$	Line Regulation	3.5 V < V_{IN} ≤ 5.5 V, I_{OUT} = 1 mA	–	0.05	0.20	%/V
$Load_{Reg}$	Load Regulation	0 mA < I_{OUT} ≤ 150 mA, V_{IN} = 3.5 V	−20	1	20	mV
V_{DO}	Dropout Voltage	I_{OUT} = 150 mA (Note 16)	–	335	460	mV
I_{OUT}	Output Current	(Note 17)	150	–	–	mA
I_{SC}	Short Circuit Current Limit	V_{OUT} = 0 V	–	225	–	mA
I_Q	Quiescent Current	I_{OUT} = 0 mA	–	0.5	0.9	μA
I_{STB}	Standby Current	V_{EN} = 0 V, T_J = 25°C	–	0.1	0.5	μA
V_{ENH}	EN Pin Threshold Voltage	EN Input Voltage “H”	1.2	–	–	V
V_{ENL}	EN Pin Threshold Voltage	EN Input Voltage “L”	–	–	0.4	V
I_{EN}	EN Pull Down Current	V_{EN} ≤ V_{IN} ≤ 5.5 V (Note 18)	–	10	–	nA
PSRR	Power Supply Rejection Ratio	f = 1 kHz, V_{IN} = 3.5 V + 200 mVpp Modulation I_{OUT} = 150 mA	–	57	–	dB
V_{NOISE}	Output Noise Voltage	V_{IN} = 5.5 V, I_{OUT} = 1 mA f = 100 Hz to 1 MHz, C_{OUT} = 1 μF	–	100	–	μV_{rms}
R_{LOW}	Active Output Discharge Resistance (A option only)	V_{IN} = 5.5 V, V_{EN} = 0 V (Note 18)	–	100	–	Ω
T_{SD}	Thermal Shutdown Temperature	Temperature Increasing from T_J = +25°C (Note 18)	–	175	–	°C
T_{SDH}	Thermal Shutdown Hysteresis	Temperature Falling from T_{SD} (Note 18)	–	25	–	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

15. Performance guaranteed over the indicated operating temperature range by design and/or characterization production tested at T_J = T_A = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
16. Characterized when V_{OUT} falls 57 mV below the regulated voltage and only for devices with V_{OUT} = 1.9 V.
17. Respect SOA.
18. Guaranteed by design and characterization.

ELECTRICAL CHARACTERISTICS – VOLTAGE VERSION 2.5 V

(–40°C ≤ T_J ≤ 85°C; V_{IN} = 3.5 V; I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 1.0 μF, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 19)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Operating Input Voltage		2.2	–	5.5	V
V_{OUT}	Output Voltage	T_A = +25°C	2.475	2.5	2.525	V
		–40°C ≤ T_J ≤ 85°C	2.450	2.5	2.550	
$Line_{Reg}$	Line Regulation	3.5 V < V_{IN} ≤ 5.5 V, I_{OUT} = 1 mA	–	0.05	0.20	%/V
$Load_{Reg}$	Load Regulation	0 mA < I_{OUT} ≤ 150 mA, V_{IN} = 3.5 V	–20	1	20	mV
V_{DO}	Dropout Voltage	I_{OUT} = 150 mA (Note 20)	–	240	330	mV
I_{OUT}	Output Current	(Note 21)	150	–	–	mA
I_{SC}	Short Circuit Current Limit	V_{OUT} = 0 V	–	225	–	mA
I_Q	Quiescent Current	I_{OUT} = 0 mA	–	0.5	0.9	μA
I_{STB}	Standby Current	V_{EN} = 0 V, T_J = 25°C	–	0.1	0.5	μA
V_{ENH}	EN Pin Threshold Voltage	EN Input Voltage “H”	1.2	–	–	V
V_{ENL}	EN Pin Threshold Voltage	EN Input Voltage “L”	–	–	0.4	V
I_{EN}	EN Pull Down Current	V_{EN} ≤ V_{IN} ≤ 5.5 V (Note 22)	–	10	–	nA
PSRR	Power Supply Rejection Ratio	f = 1 kHz, V_{IN} = 3.5 V + 200 mVpp Modulation I_{OUT} = 150 mA	–	57	–	dB
V_{NOISE}	Output Noise Voltage	V_{IN} = 5.5 V, I_{OUT} = 1 mA f = 100 Hz to 1 MHz, C_{OUT} = 1 μF	–	125	–	μV_{rms}
R_{LOW}	Active Output Discharge Resistance (A option only)	V_{IN} = 5.5 V, V_{EN} = 0 V (Note 22)	–	100	–	Ω
T_{SD}	Thermal Shutdown Temperature	Temperature Increasing from T_J = +25°C (Note 22)	–	175	–	°C
T_{SDH}	Thermal Shutdown Hysteresis	Temperature Falling from T_{SD} (Note 22)	–	25	–	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

19. Performance guaranteed over the indicated operating temperature range by design and/or characterization production tested at T_J = T_A = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
20. Characterized when V_{OUT} falls 75 mV below the regulated voltage and only for devices with V_{OUT} = 2.5 V.
21. Respect SOA.
22. Guaranteed by design and characterization.

ELECTRICAL CHARACTERISTICS – VOLTAGE VERSION 2.8 V

(–40°C ≤ T_J ≤ 85°C; V_{IN} = 3.8 V; I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 1.0 μF, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 23)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Operating Input Voltage		2.2	–	5.5	V
V_{OUT}	Output Voltage	T_A = +25°C	2.772	2.8	2.828	V
		–40°C ≤ T_J ≤ 85°C	2.744	2.8	2.856	
$Line_{Reg}$	Line Regulation	3.8 V < V_{IN} ≤ 5.5 V, I_{OUT} = 1 mA	–	0.05	0.20	%/V
$Load_{Reg}$	Load Regulation	0 mA < I_{OUT} ≤ 150 mA, V_{IN} = 3.8 V	–20	1	20	mV
V_{DO}	Dropout Voltage	I_{OUT} = 150 mA (Note 24)	–	210	300	mV
I_{OUT}	Output Current	(Note 25)	150	–	–	mA
I_{SC}	Short Circuit Current Limit	V_{OUT} = 0 V	–	195	–	mA
I_Q	Quiescent Current	I_{OUT} = 0 mA	–	0.5	0.9	μA
I_{STB}	Standby Current	V_{EN} = 0 V, T_J = 25°C	–	0.1	0.5	μA
V_{ENH}	EN Pin Threshold Voltage	EN Input Voltage “H”	1.2	–	–	V
V_{ENL}	EN Pin Threshold Voltage	EN Input Voltage “L”	–	–	0.4	V
I_{EN}	EN Pull Down Current	V_{EN} ≤ V_{IN} ≤ 5.5 V (Note 26)	–	10	–	nA
PSRR	Power Supply Rejection Ratio	f = 1 kHz, V_{IN} = 3.8 V + 200 mVpp Modulation I_{OUT} = 150 mA	–	40	–	dB
V_{NOISE}	Output Noise Voltage	V_{IN} = 5.5 V, I_{OUT} = 1 mA f = 100 Hz to 1 MHz, C_{OUT} = 1 μF	–	125	–	μV_{rms}
R_{LOW}	Active Output Discharge Resistance (A option only)	V_{IN} = 5.5 V, V_{EN} = 0 V (Note 26)	–	100	–	Ω
T_{SD}	Thermal Shutdown Temperature	Temperature Increasing from T_J = +25°C (Note 26)	–	175	–	°C
T_{SDH}	Thermal Shutdown Hysteresis	Temperature Falling from T_{SD} (Note 26)	–	25	–	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

23. Performance guaranteed over the indicated operating temperature range by design and/or characterization production tested at T_J = T_A = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
24. Characterized when V_{OUT} falls 84 mV below the regulated voltage and only for devices with V_{OUT} = 2.8 V.
25. Respect SOA.
26. Guaranteed by design and characterization.

ELECTRICAL CHARACTERISTICS – VOLTAGE VERSION 3.0 V

(–40°C ≤ T_J ≤ 85°C; V_{IN} = 4.0 V; I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 1.0 μF, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 27)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Operating Input Voltage		2.2	–	5.5	V
V_{OUT}	Output Voltage	T_A = +25°C	2.97	3.0	3.03	V
		–40°C ≤ T_J ≤ 85°C	2.94	3.0	3.06	
$Line_{Reg}$	Line Regulation	4.0 V < V_{IN} ≤ 5.5 V, I_{OUT} = 1 mA	–	0.05	0.20	%/V
$Load_{Reg}$	Load Regulation	0 mA < I_{OUT} ≤ 150 mA, V_{IN} = 4 V	–20	1	20	mV
V_{DO}	Dropout Voltage	I_{OUT} = 150 mA (Note 28)	–	190	260	mV
I_{OUT}	Output Current	(Note 29)	150	–	–	mA
I_{SC}	Short Circuit Current Limit	V_{OUT} = 0 V	–	195	–	mA
I_Q	Quiescent Current	I_{OUT} = 0 mA	–	0.5	0.9	μA
I_{STB}	Standby Current	V_{EN} = 0 V, T_J = 25°C	–	0.1	0.5	μA
V_{ENH}	EN Pin Threshold Voltage	EN Input Voltage “H”	1.2	–	–	V
V_{ENL}	EN Pin Threshold Voltage	EN Input Voltage “L”	–	–	0.4	V
I_{EN}	EN Pull Down Current	V_{EN} ≤ V_{IN} ≤ 5.5 V (Note 30)	–	10	–	nA
PSRR	Power Supply Rejection Ratio	f = 1 kHz, V_{IN} = 4.0 V + 200 mVpp Modulation I_{OUT} = 150 mA	–	47	–	dB
V_{NOISE}	Output Noise Voltage	V_{IN} = 5.5 V, I_{OUT} = 1 mA f = 100 Hz to 1 MHz, C_{OUT} = 1 μF	–	120	–	μV_{rms}
R_{LOW}	Active Output Discharge Resistance (A option only)	V_{IN} = 5.5 V, V_{EN} = 0 V (Note 30)	–	100	–	Ω
T_{SD}	Thermal Shutdown Temperature	Temperature Increasing from T_J = +25°C (Note 30)	–	175	–	°C
T_{SDH}	Thermal Shutdown Hysteresis	Temperature Falling from T_{SD} (Note 30)	–	25	–	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

27. Performance guaranteed over the indicated operating temperature range by design and/or characterization production tested at T_J = T_A = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
28. Characterized when V_{OUT} falls 90 mV below the regulated voltage and only for devices with V_{OUT} = 3.0 V.
29. Respect SOA.
30. Guaranteed by design and characterization.

ELECTRICAL CHARACTERISTICS – VOLTAGE VERSION 3.3 V

(–40°C ≤ T_J ≤ 85°C; V_{IN} = 4.3 V; I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 1.0 μF, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 31)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Operating Input Voltage		2.2	–	5.5	V
V_{OUT}	Output Voltage	T_A = +25°C	3.267	3.3	3.333	V
		–40°C ≤ T_J ≤ 85°C	3.234	3.3	3.366	
$Line_{Reg}$	Line Regulation	4.3 V < V_{IN} ≤ 5.5 V, I_{OUT} = 1 mA	–	0.05	0.20	%/V
$Load_{Reg}$	Load Regulation	0 mA < I_{OUT} ≤ 150 mA, V_{IN} = 4.3 V	–20	1	20	mV
V_{DO}	Dropout Voltage	I_{OUT} = 150 mA (Note 32)	–	180	250	mV
I_{OUT}	Output Current	(Note 33)	150	–	–	mA
I_{SC}	Short Circuit Current Limit	V_{OUT} = 0 V	–	195	–	mA
I_Q	Quiescent Current	I_{OUT} = 0 mA	–	0.5	0.9	μA
I_{STB}	Standby Current	V_{EN} = 0 V, T_J = 25°C	–	0.1	0.5	μA
V_{ENH}	EN Pin Threshold Voltage	EN Input Voltage “H”	1.2	–	–	V
V_{ENL}	EN Pin Threshold Voltage	EN Input Voltage “L”	–	–	0.4	V
I_{EN}	EN Pull Down Current	V_{EN} ≤ V_{IN} ≤ 5.5 V (Note 34)	–	10	–	nA
PSRR	Power Supply Rejection Ratio	f = 1 kHz, V_{IN} = 4.3 V + 200 mVpp Modulation I_{OUT} = 150 mA	–	41	–	dB
V_{NOISE}	Output Noise Voltage	V_{IN} = 5.5 V, I_{OUT} = 1 mA f = 100 Hz to 1 MHz, C_{OUT} = 1 μF	–	125	–	μV_{rms}
R_{LOW}	Active Output Discharge Resistance (A option only)	V_{IN} = 5.5 V, V_{EN} = 0 V (Note 34)	–	100	–	Ω
T_{SD}	Thermal Shutdown Temperature	Temperature Increasing from T_J = +25°C (Note 34)	–	175	–	°C
T_{SDH}	Thermal Shutdown Hysteresis	Temperature Falling from T_{SD} (Note 34)	–	25	–	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

31. Performance guaranteed over the indicated operating temperature range by design and/or characterization production tested at T_J = T_A = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
32. Characterized when V_{OUT} falls 99 mV below the regulated voltage and only for devices with V_{OUT} = 3.3 V.
33. Respect SOA.
34. Guaranteed by design and characterization.

ELECTRICAL CHARACTERISTICS – VOLTAGE VERSION 3.6 V

(−40°C ≤ T_J ≤ 85°C; V_{IN} = 4.6 V; I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 1.0 μF, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 35)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Operating Input Voltage		2.2	–	5.5	V
V_{OUT}	Output Voltage	T_A = +25°C	3.564	3.6	3.636	V
		−40°C ≤ T_J ≤ 85°C	3.528	3.6	3.672	
$Line_{Reg}$	Line Regulation	4.6 V < V_{IN} ≤ 5.5 V, I_{OUT} = 1 mA	–	0.05	0.20	%/V
$Load_{Reg}$	Load Regulation	0 mA < I_{OUT} ≤ 150 mA, V_{IN} = 4.6 V	−20	1	20	mV
V_{DO}	Dropout Voltage	I_{OUT} = 150 mA (Note 36)	–	170	240	mV
I_{OUT}	Output Current	(Note 37)	150	–	–	mA
I_{SC}	Short Circuit Current Limit	V_{OUT} = 0 V	–	195	–	mA
I_Q	Quiescent Current	I_{OUT} = 0 mA	–	0.5	0.9	μA
I_{STB}	Standby Current	V_{EN} = 0 V, T_J = 25°C	–	0.1	0.5	μA
V_{ENH}	EN Pin Threshold Voltage	EN Input Voltage “H”	1.2	–	–	V
V_{ENL}	EN Pin Threshold Voltage	EN Input Voltage “L”	–	–	0.4	V
I_{EN}	EN Pull Down Current	V_{EN} ≤ V_{IN} ≤ 5.5 V (Note 38)	–	10	–	nA
PSRR	Power Supply Rejection Ratio	f = 1 kHz, V_{IN} = 4.6 V + 200 mVpp Modulation I_{OUT} = 150 mA	–	30	–	dB
V_{NOISE}	Output Noise Voltage	V_{IN} = 5.5 V, I_{OUT} = 1 mA f = 100 Hz to 1 MHz, C_{OUT} = 1 μF	–	130	–	μV_{rms}
R_{LOW}	Active Output Discharge Resistance (A option only)	V_{IN} = 5.5 V, V_{EN} = 0 V (Note 34)	–	100	–	
T_{SD}	Thermal Shutdown Temperature	Temperature Increasing from T_J = +25°C (Note 38)	–	175	–	°C
T_{SDH}	Thermal Shutdown Hysteresis	Temperature Falling from T_{SD} (Note 38)	–	25	–	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

35. Performance guaranteed over the indicated operating temperature range by design and/or characterization production tested at T_J = T_A = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
36. Characterized when V_{OUT} falls 108 mV below the regulated voltage and only for devices with V_{OUT} = 3.6 V.
37. Respect SOA.
38. Guaranteed by design and characterization.

TYPICAL CHARACTERISTICS

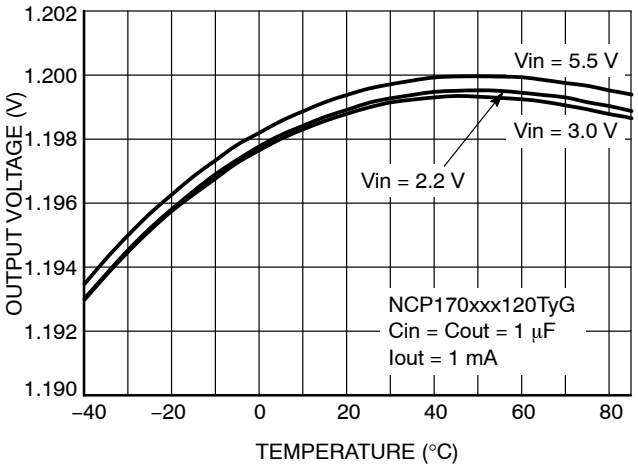


Figure 3. Output Voltage vs. Temperature, Vout = 1.2 V

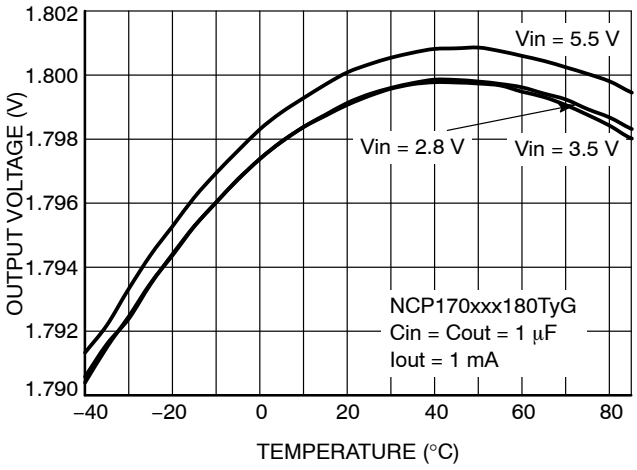


Figure 4. Output Voltage vs. Temperature, Vout = 1.8 V

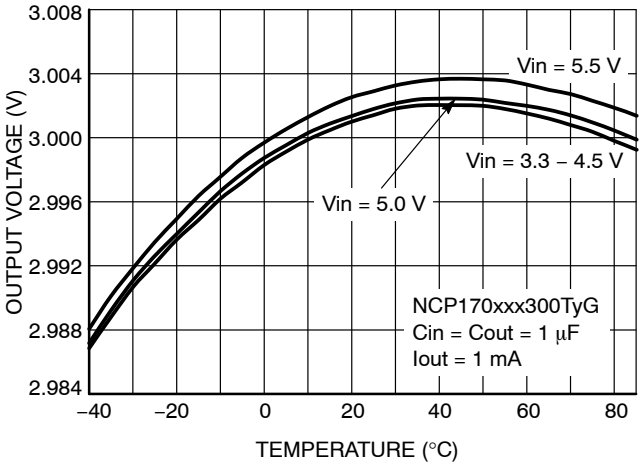


Figure 5. Output Voltage vs. Temperature, Vout = 3.0 V

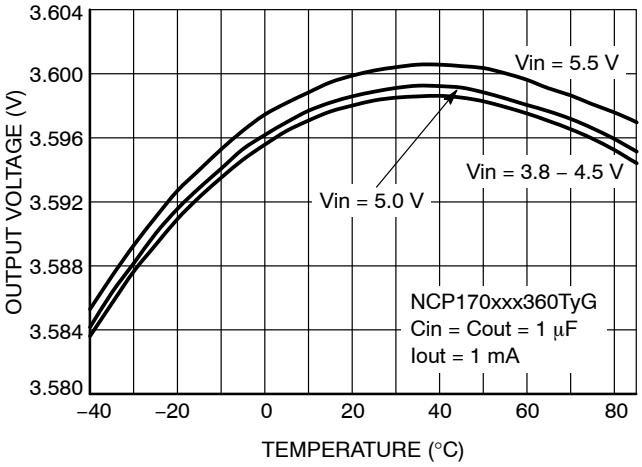


Figure 6. Output Voltage vs. Temperature, Vout = 3.6 V

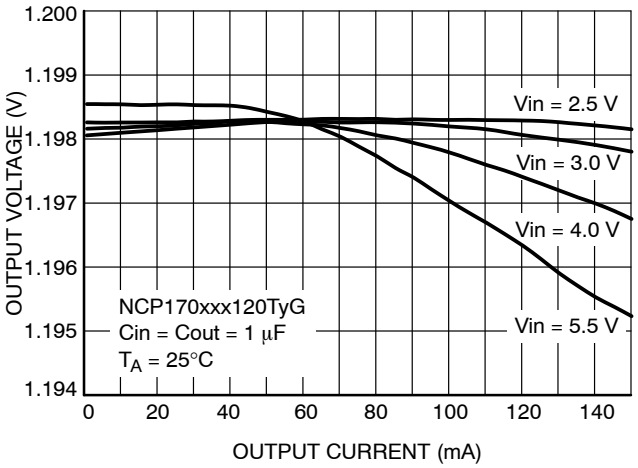


Figure 7. Output Voltage vs. Output Current, Vout = 1.2 V

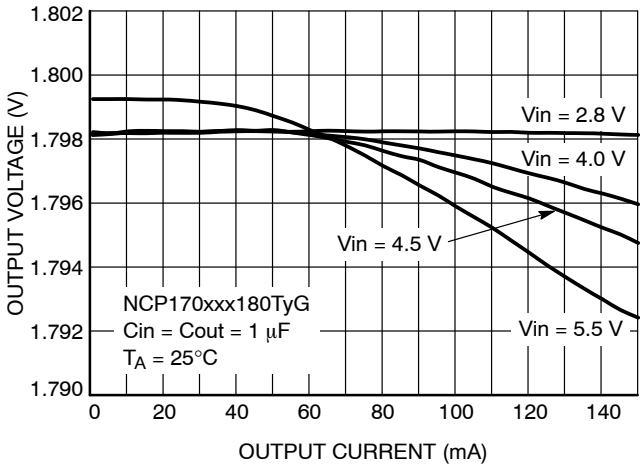


Figure 8. Output Voltage vs. Output Current, Vout = 1.8 V

TYPICAL CHARACTERISTICS

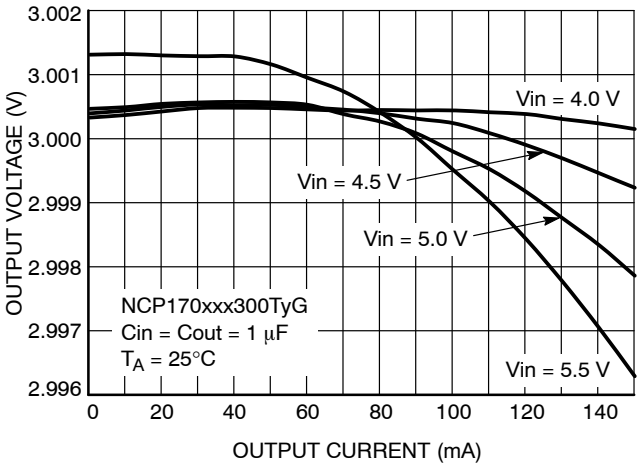


Figure 9. Output Voltage vs. Output Current, Vout = 3.0 V

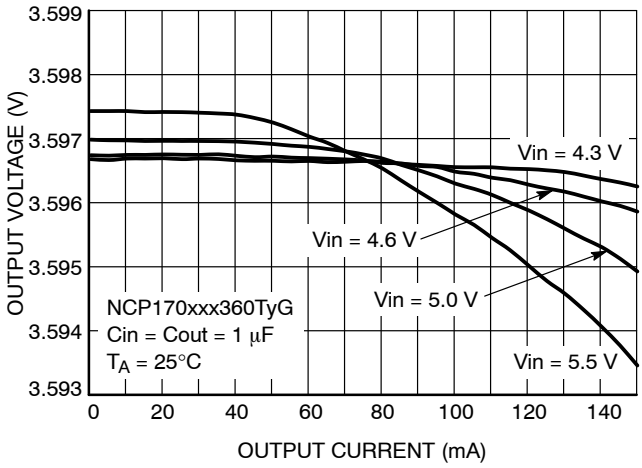


Figure 10. Output Voltage vs. Output Current, Vout = 3.6 V

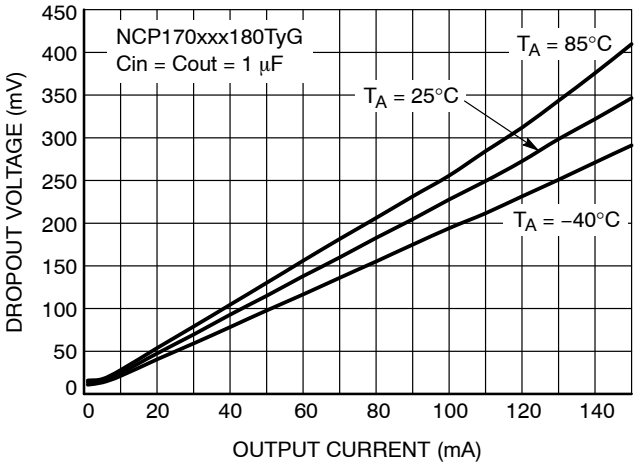


Figure 11. Dropout Voltage vs. Output Current, Vout = 1.8 V

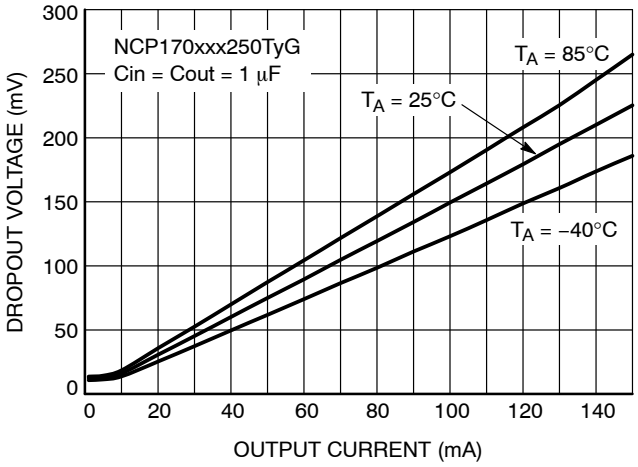


Figure 12. Dropout Voltage vs. Output Current, Vout = 2.5 V

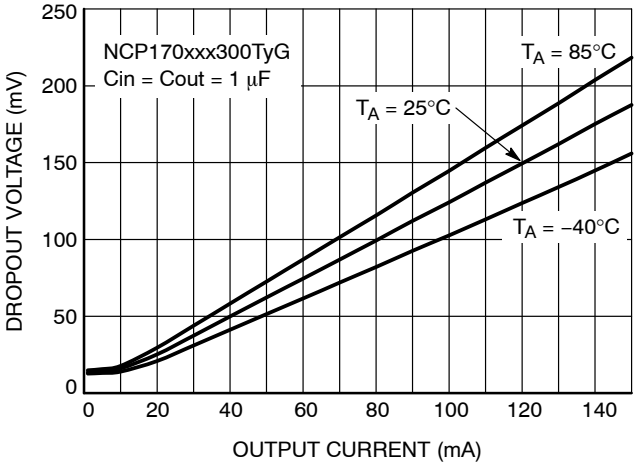


Figure 13. Dropout Voltage vs. Output Current, Vout = 3.0 V

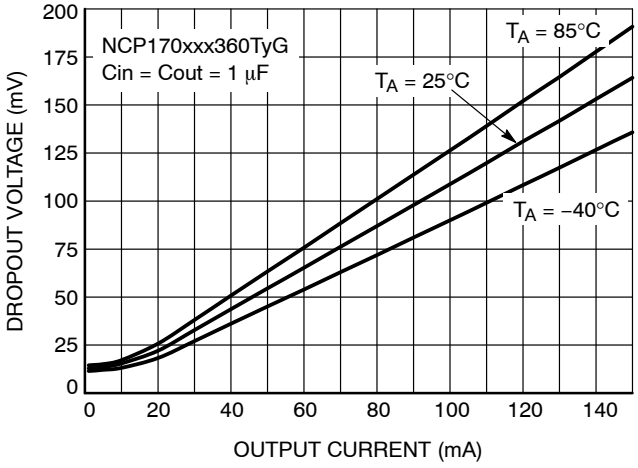


Figure 14. Dropout Voltage vs. Output Current, Vout = 3.6 V

TYPICAL CHARACTERISTICS

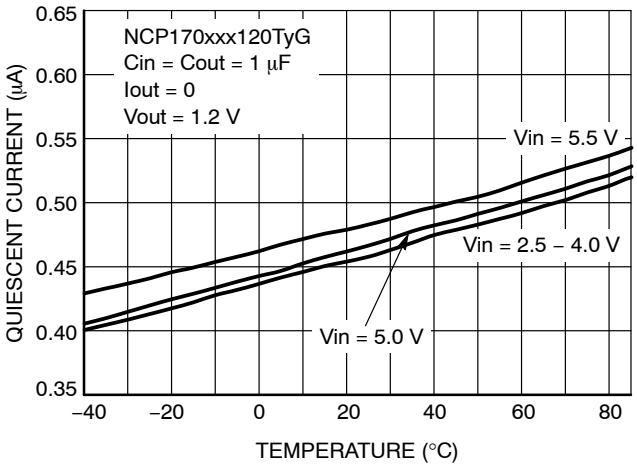


Figure 15. Quiescent Current vs. Temperature, Vout = 1.2 V

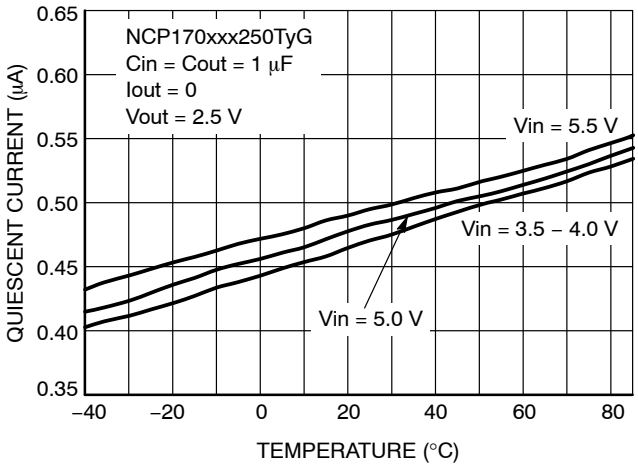


Figure 16. Quiescent Current vs. Temperature, Vout = 2.5 V

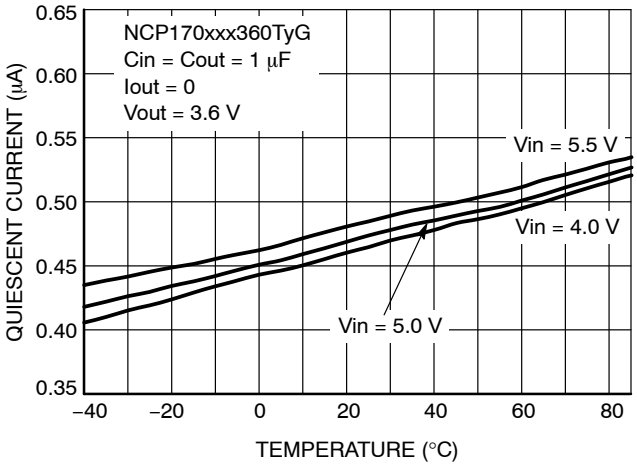


Figure 17. Quiescent Current vs. Temperature, Vout = 3.6 V

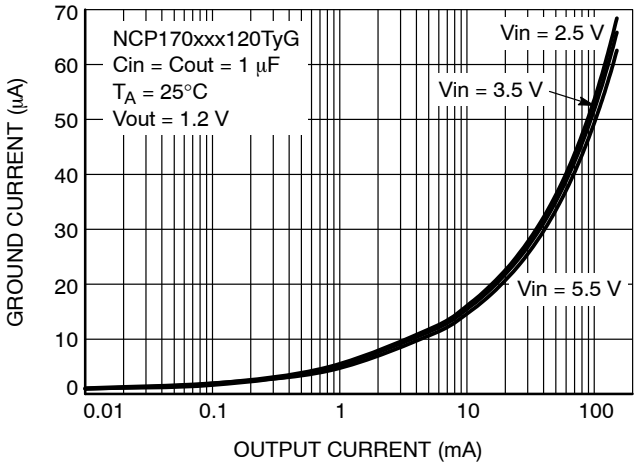


Figure 18. Ground Current vs. Output Current, Vout = 1.2 V

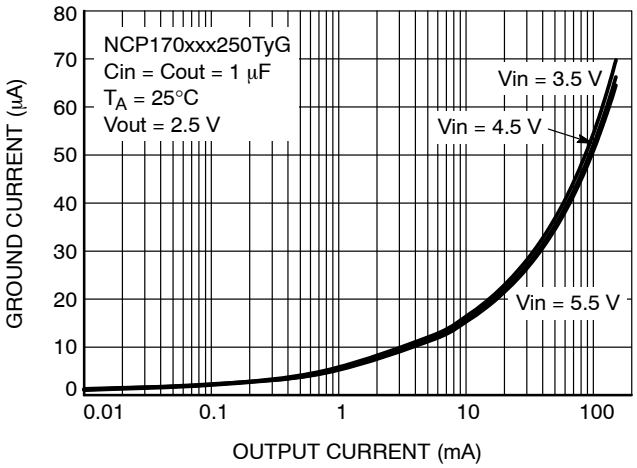


Figure 19. Ground Current vs. Output Current, Vout = 2.5 V

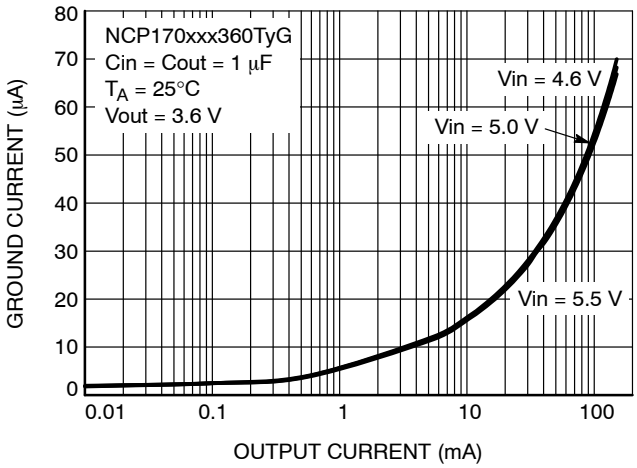


Figure 20. Ground Current vs. Output Current, Vout = 3.6 V

TYPICAL CHARACTERISTICS

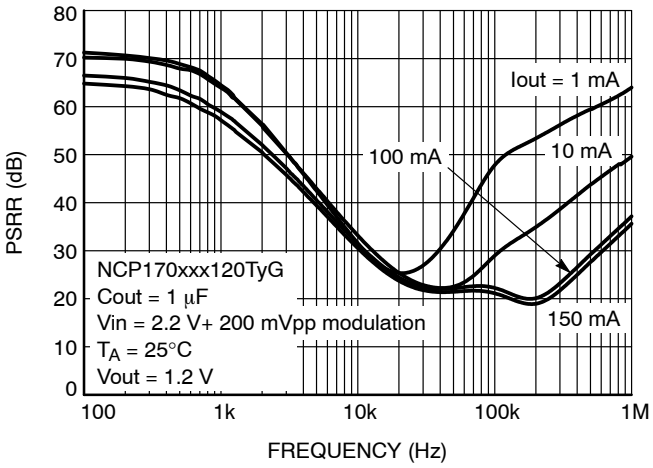


Figure 21. PSRR vs. Frequency, Vout = 1.2 V

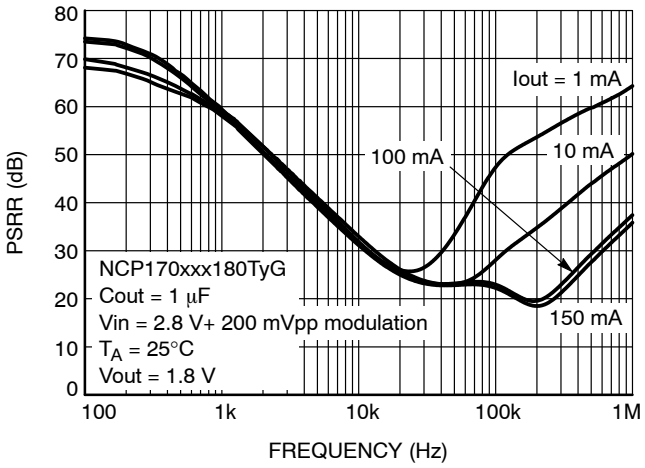


Figure 22. PSRR vs. Frequency, Vout = 1.8 V

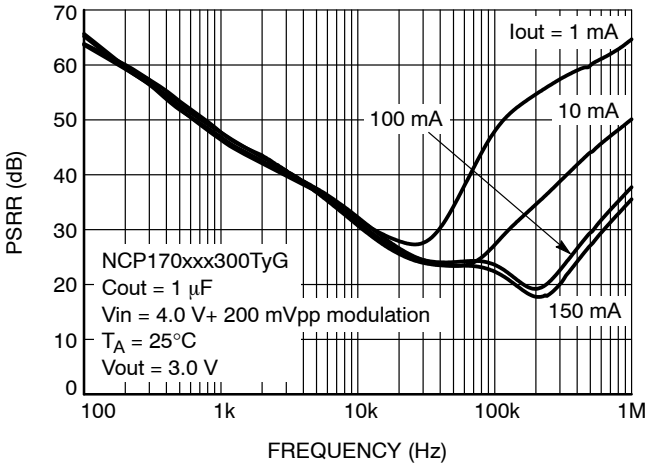


Figure 23. PSRR vs. Frequency, Vout = 3.0 V

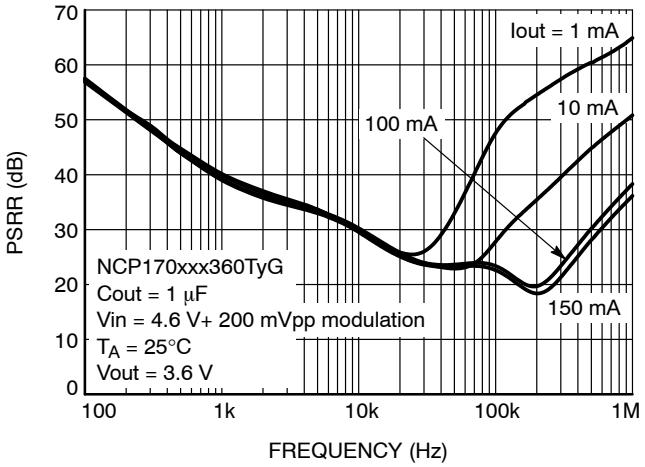


Figure 24. PSRR vs. Frequency, Vout = 3.6 V

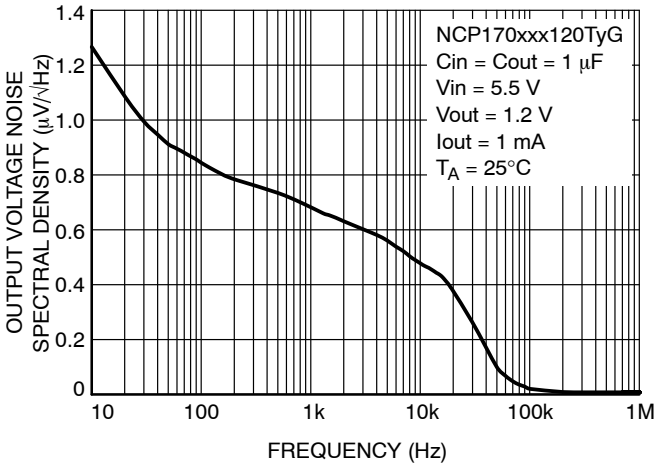


Figure 25. Output Voltage Noise Spectral Density, Vout = 1.2 V

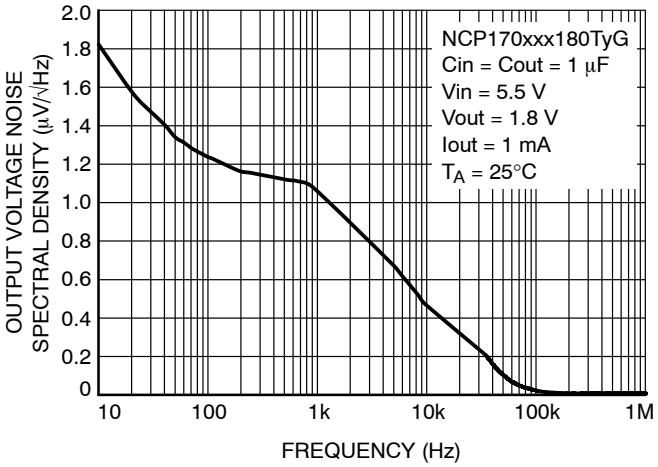


Figure 26. Output Voltage Noise Spectral Density, Vout = 1.8 V

TYPICAL CHARACTERISTICS

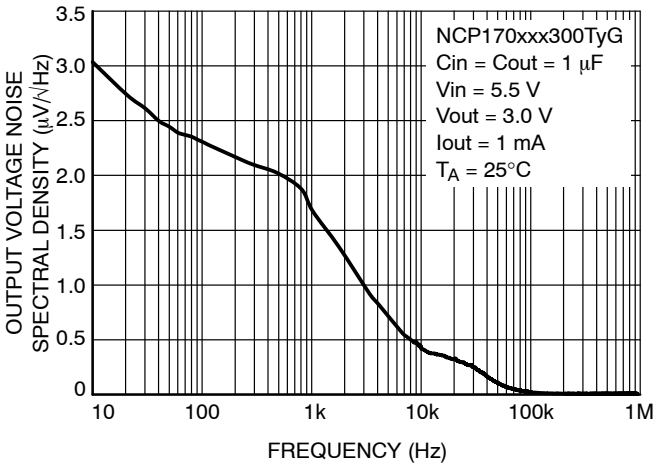


Figure 27. Output Voltage Noise Spectral Density, Vout = 3.0 V

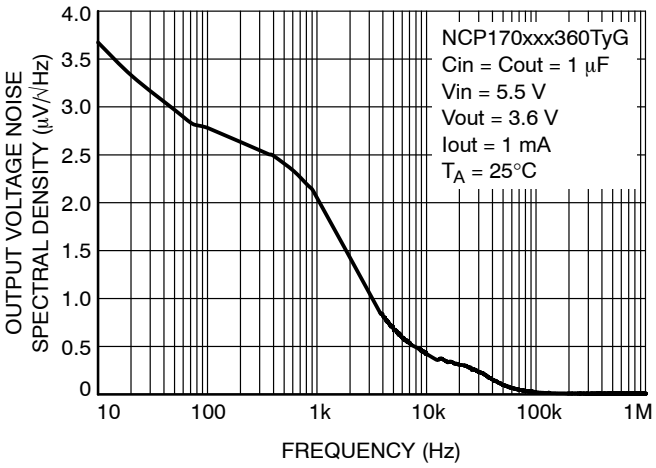


Figure 28. Output Voltage Noise Spectral Density, Vout = 3.6 V

TYPICAL CHARACTERISTICS

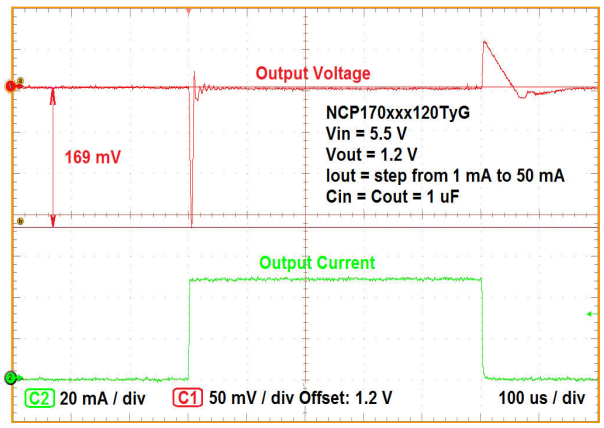


Figure 29. Load Transient Response at Load Step from 1 mA to 50 mA, Vout = 1.2 V

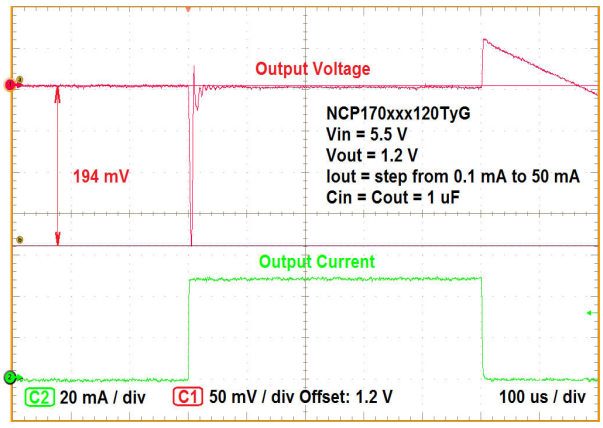


Figure 30. Load Transient Response at Load Step from 0.1 mA to 50 mA, Vout = 1.2 V

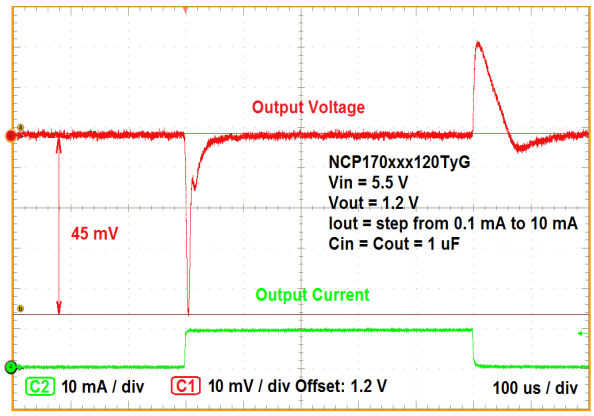


Figure 31. Load Transient Response at Load Step from 0.1 mA to 10 mA, Vout = 1.2 V

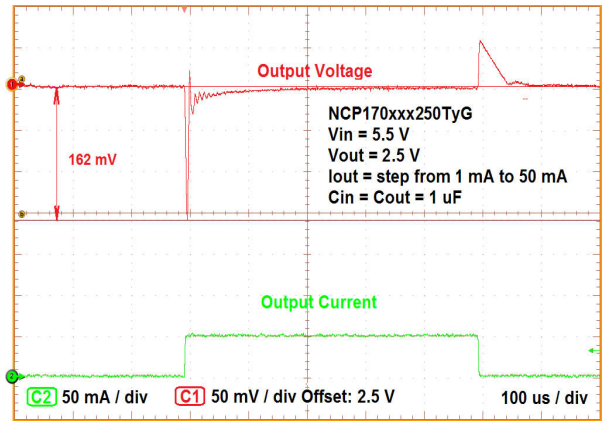


Figure 32. Load Transient Response at Load Step from 1 mA to 50 mA, Vout = 2.5 V

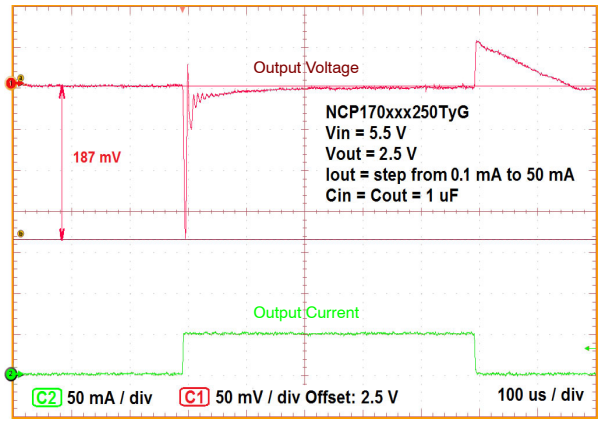


Figure 33. Load Transient Response at Load Step from 0.1 mA to 50 mA, Vout = 2.5 V

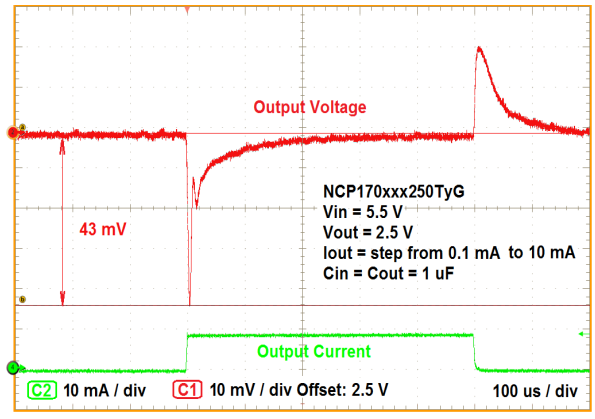


Figure 34. Load Transient Response at Load Step from 0.1 mA to 10 mA, Vout = 2.5 V

TYPICAL CHARACTERISTICS

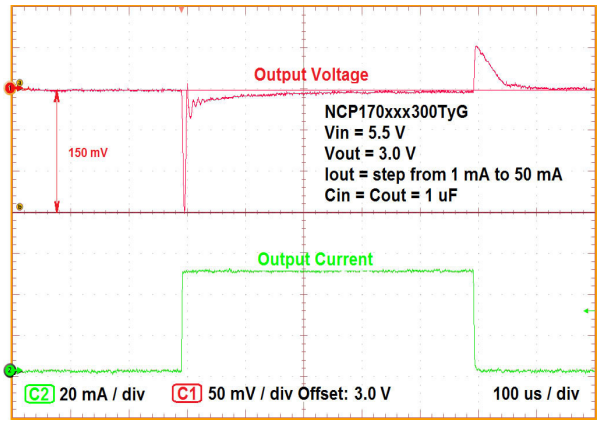


Figure 35. Load Transient Response at Load Step from 1mA to 50 mA, Vout= 3.0 V

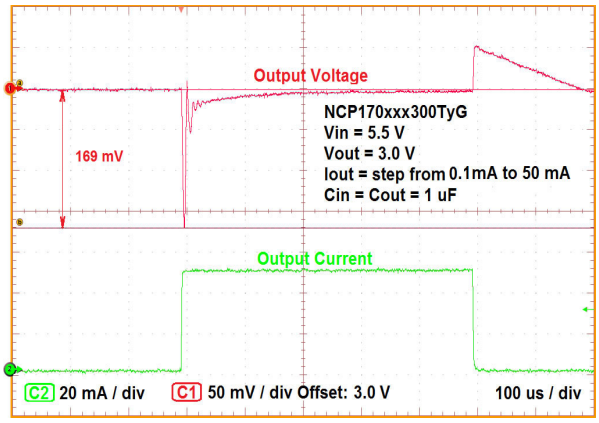


Figure 36. Load Transient Response at Load Step from 0.1 mA to 50 mA, Vout = 3.0 V

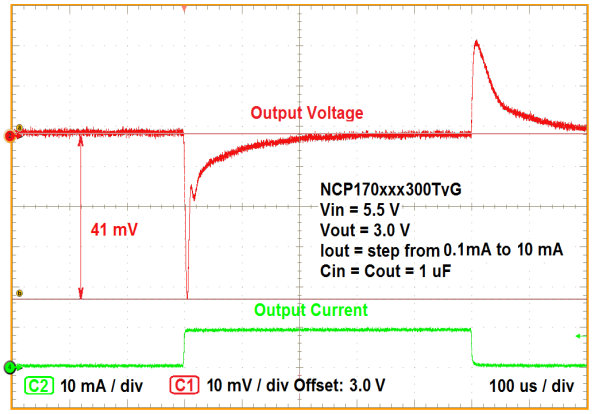


Figure 37. Load Transient Response at Load Step from 0.1 mA to 10 mA, Vout = 3.0 V

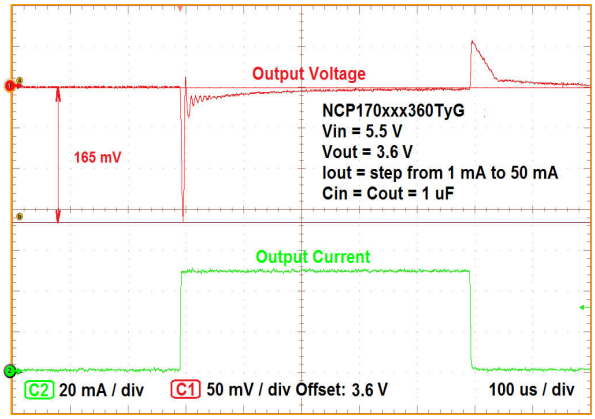


Figure 38. Load Transient Response at Load Step from 1 mA to 50 mA, Vout = 3.6 V

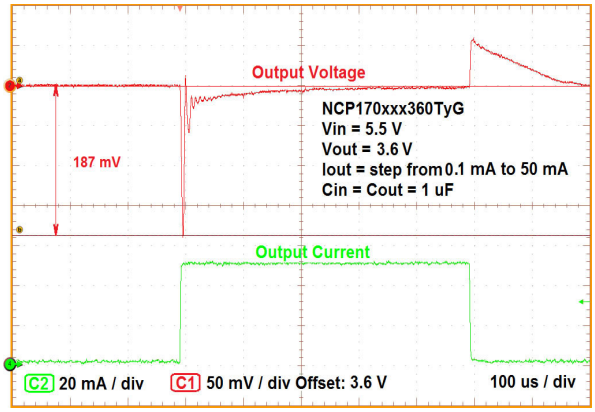


Figure 39. Load Transient Response at Load Step from 0.1 mA to 50 mA, Vout = 3.6 V

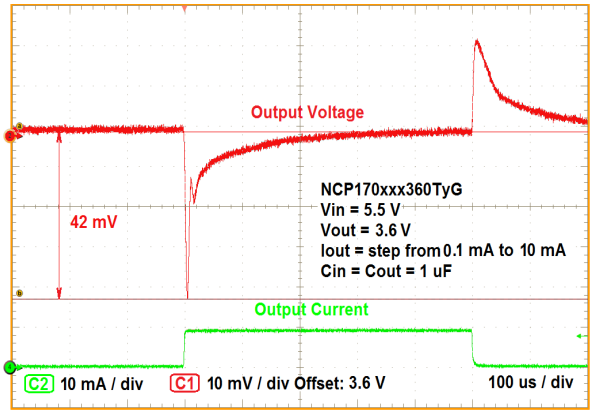


Figure 40. Load Transient Response at Load Step from 0.1 mA to 10 mA, Vout = 3.6 V

TYPICAL CHARACTERISTICS

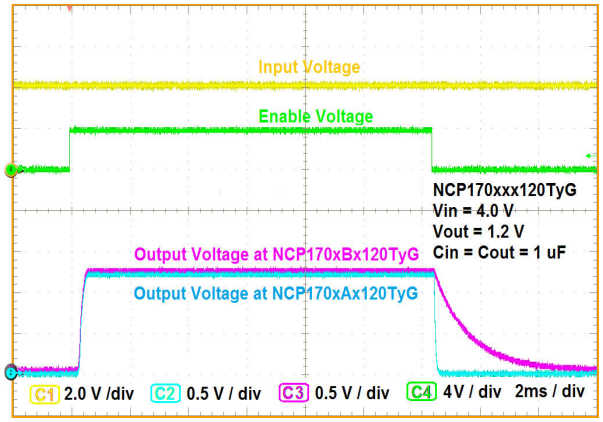


Figure 41. Output Voltage with and without Active Discharge Feature, Vout = 1.2 V

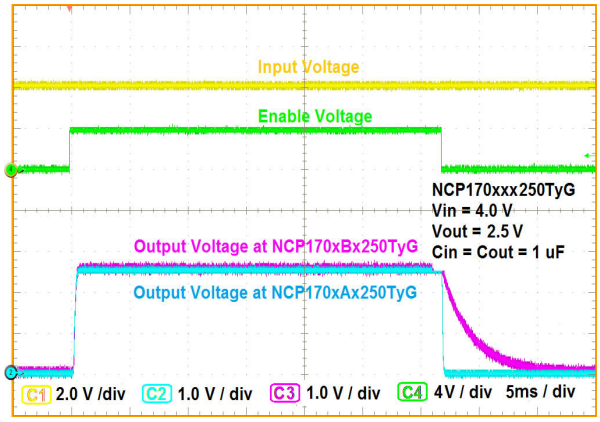


Figure 42. Output Voltage with and without Active Discharge Feature, Vout = 2.5 V

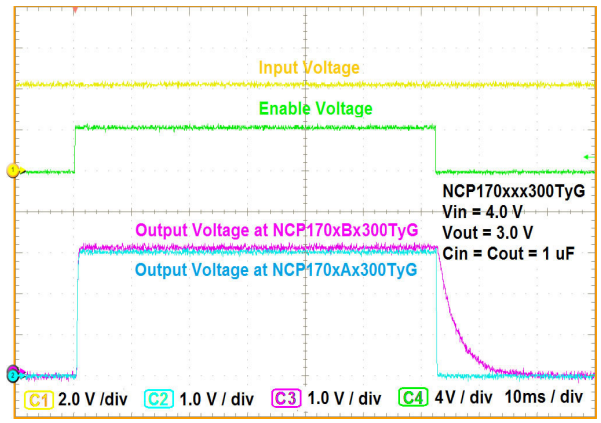


Figure 43. Output Voltage with and without Active Discharge Feature, Vout = 3.0 V

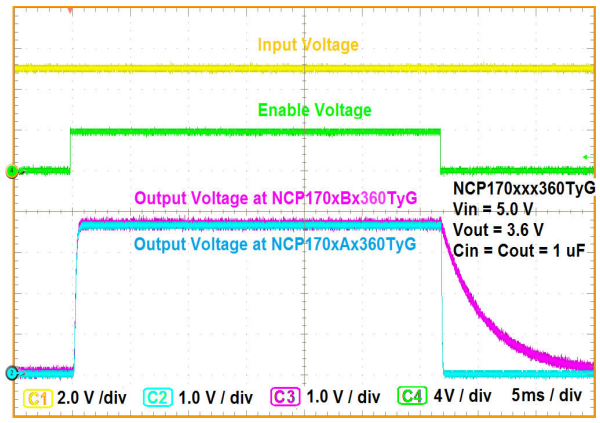


Figure 44. Output Voltage with and without Active Discharge Feature, Vout = 3.6 V

TYPICAL CHARACTERISTICS

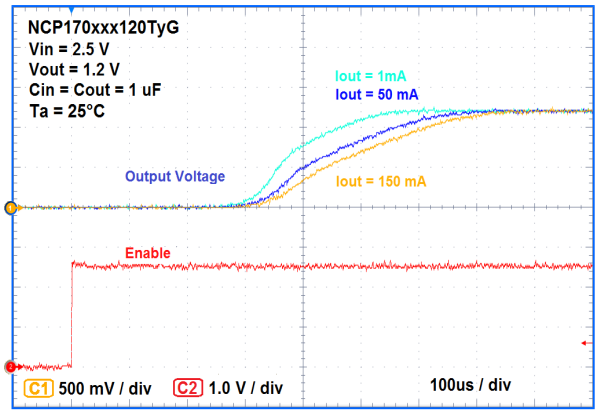


Figure 45. Enable Turn−on Response at Vout = 1.2 V

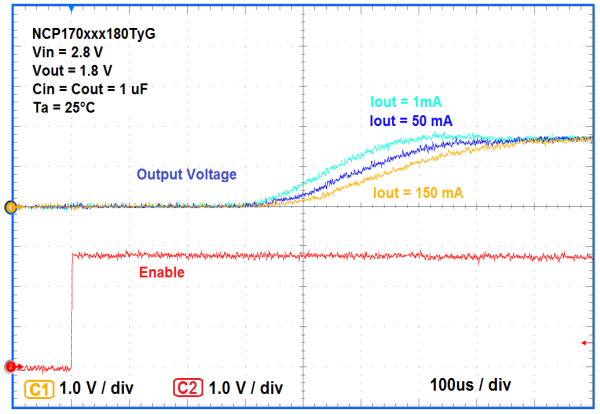


Figure 46. Enable Turn−on Response at Vout = 1.8 V

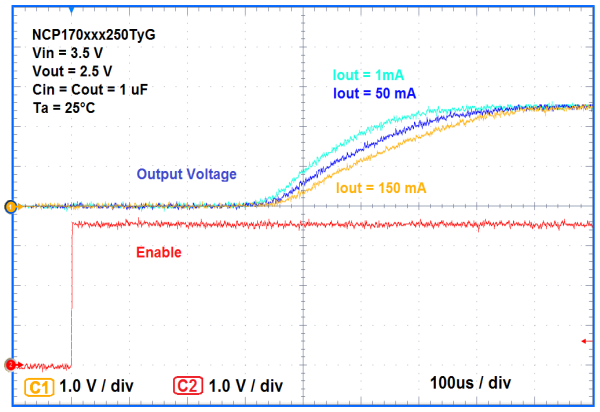


Figure 47. Enable Turn−on Response at Vout = 2.5 V

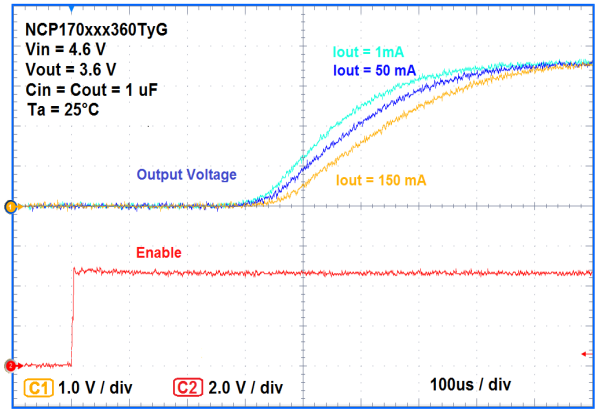


Figure 48. Enable Turn−on Response at Vout = 3.6 V

APPLICATIONS INFORMATION

General

The NCP170 is a high performance 150 mA Linear Regulator with Ultra Low IQ. This device delivers low Noise and high Power Supply Rejection Ratio with excellent dynamic performance due to employing the Dynamic Quiescent Current adjustment which assure ultra low I_Q consumption at no – load state. These parameters make this device very suitable for various battery powered applications.

Input Decoupling (C_{IN})

It is recommended to connect at least a 1 μF Ceramic X5R or X7R capacitor between IN and GND pins of the device. This capacitor will provide a low impedance path for any unwanted AC signals or Noise superimposed onto constant Input Voltage. The good input capacitor will limit the influence of input trace inductances and source resistance during sudden load current changes.

Higher capacitance and lower ESR Capacitors will improve the overall line transient response.

Output Decoupling (C_{OUT})

The NCP170 does not require a minimum Equivalent Series Resistance (ESR) for the output capacitor. The device is designed to be stable with standard ceramics capacitors with values of 1.0 μF or greater up to 10 μF. The X5R and X7R types have the lowest capacitance variations over temperature thus they are recommended. There is recommended connect the output capacitor as close as possible to the output pin of the regulator.

Enable Operation

The NCP170 uses the EN pin to enable /disable its device and to activate /deactivate the active discharge function at devices with this feature. If the EN pin voltage is pulled below 0.4 V the device is guaranteed to be disable. The active discharge transistor at the devices with Active Discharge Feature is activated and the output voltage VOUT is pulled to GND through an internal circuitry with effective resistance about 100 ohms.

If the EN pin voltage is higher than 1.2 V the device is guaranteed to be enabled. The internal active discharge circuitry is switched off and the desired output voltage is available at output pin. In case the Enable function is not required the EN pin should be connected directly to input pin.

Thermal Shutdown

When the die temperature exceeds the Thermal Shutdown point (TSD = 175°C typical) the device goes to disabled state and the output voltage is not delivered until the die temperature decreases to 150°C. The Thermal Shutdown feature provides a protection from a catastrophic device failure at accidental overheating. This protection is not intended to be used as a substitute for proper heat sinking.

Power Dissipation and Heat sinking

The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. For reliable operation, junction temperature should be limited to +125°C. The maximum power dissipation the NCP170 device can handle is given by:

$$P_{D(MAX)} = \frac{\left[T_{J(MAX)} - T_A\right]}{R_{\theta JA}} \quad \text{(eq. 1)}$$

The power dissipated by the NCP170 device for given application conditions can be calculated from the following equations:

$$P_D \approx V_{IN}\left(I_{GND}(I_{OUT})\right) + I_{OUT}\left(V_{IN} - V_{OUT}\right) \quad \text{(eq. 2)}$$

or

$$V_{IN(MAX)} \approx \frac{P_{D(MAX)} + \left(V_{OUT} \times I_{OUT}\right)}{I_{OUT} + I_{GND}} \quad \text{(eq. 3)}$$

Hints

VIN and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high, there is a chance to pick up noise or cause the regulator to malfunction. Place external components, especially the output capacitor, as close as possible to the NCP170, and make traces as short as possible.

ORDERING INFORMATION

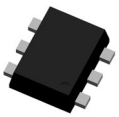
Device	Nominal Output Voltage	Marking	Active Discharge	Package	Shipping†
NCP170AMX120TCG (Note 39)	1.2	AC	Yes	XDFN4 1.0 × 1.0 (Pb-Free)	3000 or 5000 / Tape & Reel (Note 39)
NCP170AMX129TCG	1.29	AV			
NCP170AMX135TCG (Note 39)	1.35	AP			
NCP170AMX150TCG (Note 39)	1.5	AJ			
NCP170AMX170TCG	1.7	AT			
NCP170AMX180TBG (Note 39)	1.8	AD			
NCP170AMX180TCG (Note 39)	1.8	AD			
NCP170AMX190TCG	1.9	AL			
NCP170AMX250TCG (Note 39)	2.5	AE			
NCP170AMX280TBG (Note 39)	2.8	AF			
NCP170AMX280TCG (Note 39)	2.8	AF			
NCP170AMX285TCG (Note 39)	2.85	AK			
NCP170AMX300TBG (Note 39)	3.0	AA			
NCP170AMX300TCG (Note 39)	3.0	AA			
NCP170AMX310TCG	3.1	AN			
NCP170AMX320TCG	3.2	AQ			
NCP170AMX330TBG (Note 39)	3.3	AG			
NCP170AMX330TCG (Note 39)	3.3	AG			
NCP170AMX360TCG (Note 39)	3.6	AM			
NCP170BMX120TCG	1.2	2C	No		
NCP170BMX135TCG (Note 39)	1.35	2P			
NCP170BMX150TCG (Note 39)	1.5	2J			
NCP170BMX170TCG	1.7	2T			
NCP170BMX180TCG (Note 39)	1.8	2D			
NCP170BMX190TCG (Note 39)	1.9	2L			
NCP170BMX250TCG (Note 39)	2.5	2E			
NCP170BMX280TCG (Note 39)	2.8	2F			
NCP170BMX285TCG (Note 39)	2.85	2K			
NCP170BMX300TCG (Note 39)	3.0	2A			
NCP170BMX310TCG (Note 39)	3.1	2N			
NCP170BMX320TCG	3.2	2Q			
NCP170BMX330TCG (Note 39)	3.3	2G			
NCP170BMX360TCG (Note 39)	3.6	2M			

ORDERING INFORMATION

Device	Nominal Output Voltage	Marking	Active Discharge	Package	Shipping†
NCP170AXV120T2G	1.2	AC	Yes	SOT−563 (Pb-Free)	4000 / Tape & Reel (Available Soon)
NCP170AXV135T2G	1.35	AL			
NCP170AXV150T2G	1.5	AJ			
NCP170AXV180T2G	1.8	AD			
NCP170AXV190T2G	1.9	AM			
NCP170AXV210T2G	2.1	AK			
NCP170AXV250T2G	2.5	AE			
NCP170AXV280T2G	2.8	AF			
NCP170AXV300T2G	3.0	AA			
NCP170AXV310T2G	3.1	AN			
NCP170AXV330T2G	3.3	AH			
NCP170AXV360T2G	3.6	AG			
NCP170BXV120T2G	1.2	2C	No		
NCP170BXV135T2G	1.35	2L			
NCP170BXV150T2G	1.5	2J			
NCP170BXV180T2G	1.8	2D			
NCP170BXV190T2G	1.9	2M			
NCP170BXV250T2G	2.5	2E			
NCP170BXV280T2G	2.8	2F			
NCP170BXV300T2G	3.0	2A			
NCP170BXV310T2G	3.1	2N			
NCP170BXV330T2G	3.3	2H			
NCP170ASN120T2G	1.2	GCG	Yes	TSOP−5 (Pb-Free)	3000 / Tape & Reel (Available Soon)
NCP170ASN129T2G	1.29	GCJ			
NCP170ASN150T2G	1.5	GCH			
NCP170ASN180T2G	1.8	GCF			
NCP170ASN250T2G	2.5	GCE			
NCP170ASN280T2G	2.8	GCA			
NCP170ASN300T2G	3.0	GCC			
NCP170ASN330T2G	3.3	GCD			

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

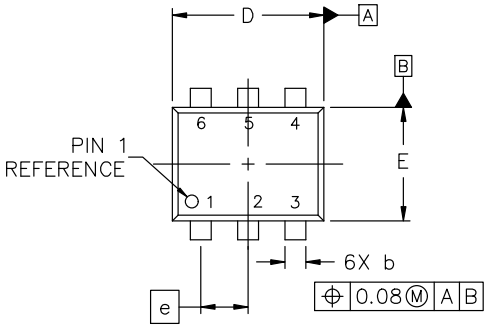
39. Product processed after October 1, 2022 are shipped with quantity 5000 units / tape & reel.



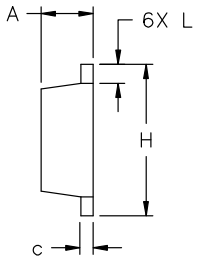
SOT−563−6 1.60x1.20x0.55, 0.50P
CASE 463A
ISSUE J

DATE 15 FEB 2024

NOTES:
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

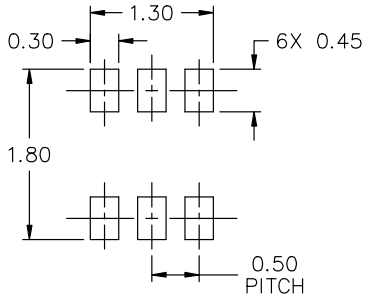


TOP VIEW



SIDE VIEW

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.50	0.55	0.60
b	0.17	0.22	0.27
c	0.08	0.13	0.18
D	1.50	1.60	1.70
E	1.10	1.20	1.30
e	0.50 BSC		
H	1.50	1.60	1.70
L	0.10	0.20	0.30



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

STYLE 1:
PIN 1. EMITTER 1
2. BASE 1
3. COLLECTOR 2
4. EMITTER 2
5. BASE 2
6. COLLECTOR 1

STYLE 2:
PIN 1. EMITTER 1
2. EMITTER 2
3. BASE 2
4. COLLECTOR 2
5. BASE 1
6. COLLECTOR 1

STYLE 3:
PIN 1. CATHODE 1
2. CATHODE 1
3. ANODE/ANODE 2
4. CATHODE 2
5. CATHODE 2
6. ANODE/ANODE 1

STYLE 4:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 5:
PIN 1. CATHODE
2. CATHODE
3. ANODE
4. ANODE
5. CATHODE
6. CATHODE

STYLE 6:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. ANODE
6. CATHODE

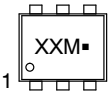
STYLE 8:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 9:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 10:
PIN 1. CATHODE 1
2. N/C
3. CATHODE 2
4. ANODE 2
5. N/C
6. ANODE 1

STYLE 11:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

GENERIC MARKING DIAGRAM*

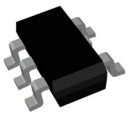


XX = Specific Device Code
M = Month Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

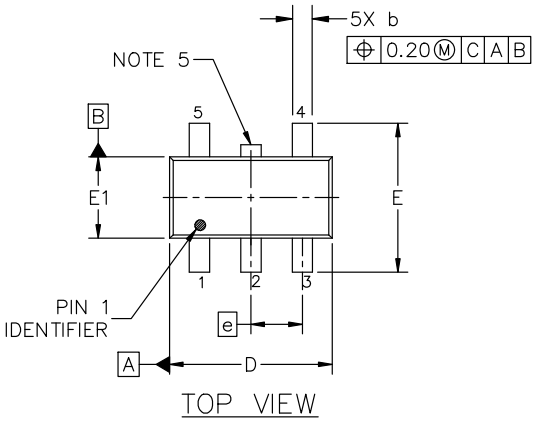
DOCUMENT NUMBER:	**98AON11126D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**SOT−563−6 1.60x1.20x0.55, 0.50P**		**PAGE 1 OF 1**

onsemi and ONSEMI are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

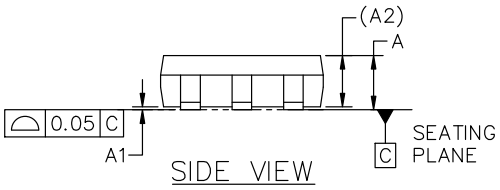


TSOP−5 3.00x1.50x0.95, 0.95P
CASE 483
ISSUE P

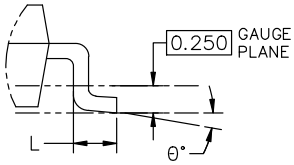
DATE 01 APR 2024



TOP VIEW



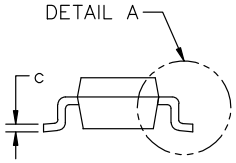
SIDE VIEW



DETAIL "A"
SCALE 2:1

NOTES:

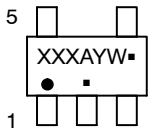
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS (ANGLES IN DEGREES).
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OF GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.



END VIEW

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.900	1.000	1.100
A1	0.010	0.055	0.100
A2		0.950 REF.	
b	0.250	0.375	0.500
c	0.100	0.180	0.260
D	2.850	3.000	3.150
E	2.500	2.750	3.000
E1	1.350	1.500	1.650
e		0.950 BSC	
L	0.200	0.400	0.600
θ	0°	5°	10°

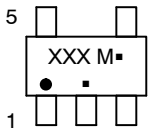
GENERIC
MARKING DIAGRAM*



Analog

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

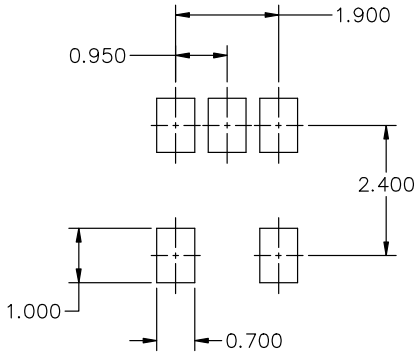
(Note: Microdot may be in either location)



Discrete/Logic

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DOCUMENT NUMBER:	**98ARB18753C**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**TSOP−5 3.00x1.50x0.95, 0.95P**	**PAGE 1 OF 1**

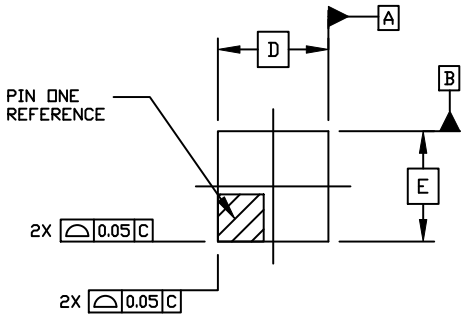
onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

© Semiconductor Components Industries, LLC, 2018

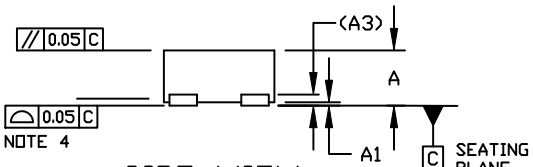


XDFN4 1.0x1.0, 0.65P
CASE 711AJ
ISSUE C

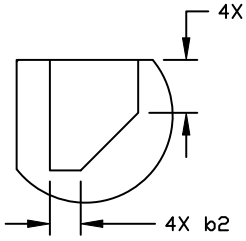
DATE 08 MAR 2022



TOP VIEW



SIDE VIEW

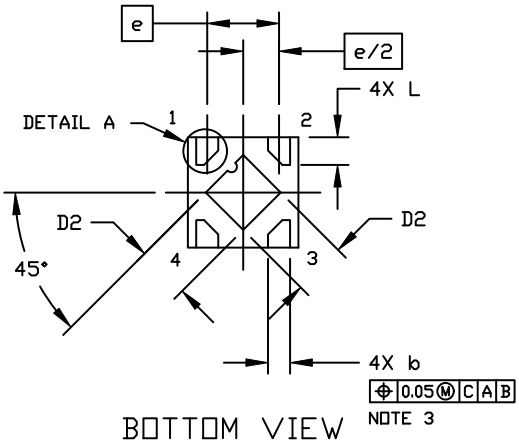


DETAIL A

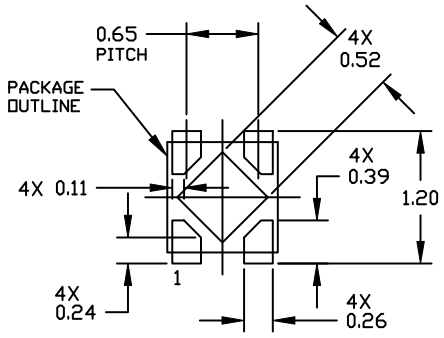
NOTES:

1. DIMENSIONING AND TOLERANCING PER. ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO THE PLATED TERMINALS AND IS MEASURED BETWEEN 0.15 AND 0.20 FROM THE TERMINAL TIPS.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.33	0.38	0.43
A1	0.00	---	0.05
A3		0.10 REF	
b	0.15	0.20	0.25
b2	0.02	0.07	0.12
D	0.90	1.00	1.10
D2	0.43	0.48	0.53
E	0.90	1.00	1.10
e		0.65 BSC	
L	0.20		0.30
L2	0.07		0.17



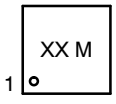
BOTTOM VIEW



RECOMMENDED
MOUNTING FOOTPRINT

* FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

GENERIC
MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON67179E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**XDFN4, 1.0X1.0, 0.65P**		**PAGE 1 OF 1**

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

© Semiconductor Components Industries, LLC, 2012

onsemi, , and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as−is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales