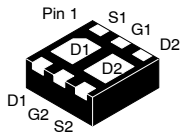
# MOSFET – Dual, P-Channel, POWERTRENCH®

## -20 V, -3.7 A, 72 mΩ

# FDMA1023PZ

| $V_{DS}$ | $R_{DS(on)}$ MAX | $I_D$ MAX |
|---|---|---|
| −20 V | 72 mΩ @ −4.5 V | −3.7 A |
| | 95 mΩ @ −2.5 V | |
| | 130 mΩ @ −1.8 V | |
| | 195 mΩ @ −1.5 V | |




**WDFN6 2x2, 0.65P**
**(MicroFET 2x2)**
**CASE 511DA**

### General Description

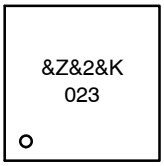
This device is designed specifically as a single package solution for the battery charge switch in cellular handset and other ultra−portable applications. It features two independent P−Channel MOSFETs with low on−state resistance for minimum conduction losses. When connected in the typical common source configuration, bi−directional current flow is possible.

The MicroFET 2x2 package offers exceptional thermal performance for its physical size and is well suited to linear mode applications.

### Features

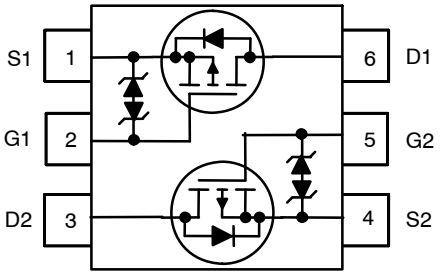
- Max $R_{DS(on)}$ = 72 mΩ at $V_{GS}$ = −4.5 V, $I_D$ = −3.7 A
- Max $R_{DS(on)}$ = 95 mΩ at $V_{GS}$ = −2.5 V, $I_D$ = −3.2 A
- Max $R_{DS(on)}$ = 130 mΩ at $V_{GS}$ = −1.8 V, $I_D$ = −2.0 A
- Max $R_{DS(on)}$ = 195 mΩ at $V_{GS}$ = −1.5 V, $I_D$ = −1.0 A
- Low Profile − 0.8 mm Maximum − In the New Package MicroFET 2x2 mm
- HBM ESD Protection Level > 2 kV (Note 3)
- Free from Halogenated Compounds and Antimony Oxides
- This Device is Pb−Free, Halide Free and is RoHS Compliant

### MARKING DIAGRAM




&Z = Assembly Plant Code
&2 = 2−Digit Date Code
&K = 2−Digits Lot Run Traceability Code
023 = Device Code

### PIN CONNECTIONS




### ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25°C unless otherwise noted)

| Symbol | Parameter | Ratings | Unit |
|---|---|---|---|
| $V_{DS}$ | Drain to Source Voltage | −20 | V |
| $V_{GS}$ | Gate to Source Voltage | ±8 | V |
| $I_D$ | Drain Current<br>−Continuous (Note 1a)<br>−Pulsed | <br>−3.7<br>−6 | A |
| $P_D$ | Power Dissipation<br>(Note 1a)<br>(Note 1b) | <br>1.5<br>0.7 | W |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | −55 to +150 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| FDMA1023PZ | WDFN6<br>(Pb−Free,<br>Halide Free) | 3000 /<br>Tape & Reel |

For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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## THERMAL CHARACTERISTICS

| Symbol | Parameter | Ratings | Unit |
|---|---|---|---|
| $R_{\theta JA}$ | Thermal Resistance for Single Operation, Junction to Ambient (Note 1a) | 86 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance for Single Operation, Junction to Ambient (Note 1b) | 173 | |
| $R_{\theta JA}$ | Thermal Resistance for Dual Operation, Junction to Ambient (Note 1c) | 69 | |
| $R_{\theta JA}$ | Thermal Resistance for Dual Operation, Junction to Ambient (Note 1d) | 151 | |

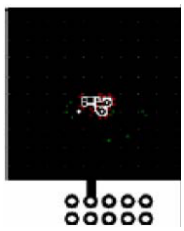
## ELECTRICAL CHARACTERISTICS ($T_J$ = 25°C unless otherwise noted)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| $BV_{DSS}$ | Drain−Source Breakdown Voltage | $I_D$ = −250 μA, $V_{GS}$ = 0 V | −20 | – | – | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = −250 μA, referenced to 25°C | – | −11 | – | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = −16 V, $V_{GS}$ = 0 V | – | – | −1 | μA |
| $I_{GSS}$ | Gate to Source Leakage Current | $V_{GS}$ = ±8 V, $V_{DS}$ = 0 V | – | – | ±10 | μA |
| **ON CHARACTERISTICS** | | | | | | |
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $I_D$ = −250 μA, $V_{GS}$ = $V_{DS}$ | −0.4 | −0.7 | −1.0 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D$ = −250 μA, referenced to 25°C | – | 2.5 | – | mV/°C |
| $R_{DS(on)}$ | Static Drain to Source On−Resistance | $V_{GS}$ = −4.5 V, $I_D$ = −3.7 A | – | 60 | 72 | mΩ |
| | | $V_{GS}$ = −2.5 V, $I_D$ = −3.2 A | – | 75 | 95 | |
| | | $V_{GS}$ = −1.8 V, $I_D$ = −2.0 A | – | 100 | 130 | |
| | | $V_{GS}$ = −1.5 V, $I_D$ = −1.0 A | – | 130 | 195 | |
| | | $V_{GS}$ = −4.5 V, $I_D$ = −3.7 A, $T_J$ = 125°C | – | 81 | 91 | |
| $g_{FS}$ | Forward Transconductance | $I_D$ = −3.7 A, $V_{DS}$ = −5 V | – | 12 | – | S |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = −10 V, $V_{GS}$ = 0 V, f = 1 MHz | – | 490 | 655 | pF |
| $C_{oss}$ | Output Capacitance | | – | 100 | 135 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | – | 90 | 135 | pF |
| **SWITCHING CHARACTERISTICS** | | | | | | |
| $t_{d(on)}$ | Turn−On Delay Time | $V_{DD}$ = −10 V, $I_D$ = −1 A, $V_{GS}$ = −4.5 V, $R_{GEN}$ = 6 Ω | – | 9 | 18 | ns |
| $t_r$ | Rise Time | | – | 12 | 22 | ns |
| $t_{d(off)}$ | Turn−Off Delay Time | | – | 64 | 103 | ns |
| $t_f$ | Fall Time | | – | 37 | 60 | ns |
| $Q_{g(TOT)}$ | Total Gate Charge | $V_{DD}$ = −10 V, $I_D$ = −3.7 A, $V_{GS}$ = −4.5 V | – | 8.6 | 12 | nC |
| $Q_{gs}$ | Gate to Source Gate Charge | | – | 0.7 | – | nC |
| $Q_{gd}$ | Gate to Drain “Miller” Charge | | – | 2.0 | – | nC |
| **SWITCHING CHARACTERISTICS** | | | | | | |
| $I_S$ | Maximum Continuous Source−Drain Diode Forward Current | | – | – | −1.1 | A |
| $V_{SD}$ | Source to Drain Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = −1.1 A (Note 2) | – | −0.8 | −1.2 | V |
| $t_{rr}$ | Reverse Recovery Time | $I_F$ = −3.7 A, di/dt = 100 A/μs | – | 32 | 48 | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | – | 15 | 23 | nC |

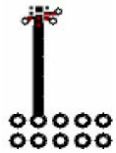
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

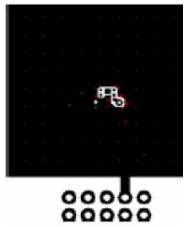
1. $R_{\theta JA}$ is determined with the device mounted on a 1 $in^2$ oz. copper pad on a 1.5 x 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.
   a. $R_{\theta JA}$ = 86°C/W when mounted on a 1 $in^2$ pad of 2 oz copper, 1.5" x 1.5" x 0.062" thick PCB. For single operation.
   b. $R_{\theta JA}$ = 173°C/W when mounted on a minimum pad of 2 oz copper. For single operation.
   c. $R_{\theta JA}$ = 69°C/W when mounted on a 1 $in^2$ pad of 2 oz copper, 1.5" x 1.5" x 0.062" thick PCB. For dual operation.
   d. $R_{\theta JA}$ = 151°C/W when mounted on a minimum pad of 2 oz copper. For dual operation.



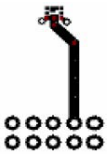
a. 86°C/W when mounted on a 1 $in^2$ pad of 2 oz copper.



b. 173°C/W when mounted on a minimum pad of 2 oz copper.



c. 69°C/W when mounted on a 1 $in^2$ pad of 2 oz copper.



d. 151°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%
3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

## TYPICAL CHARACTERISTICS ($T_J$ = 25°C unless otherwise noted)

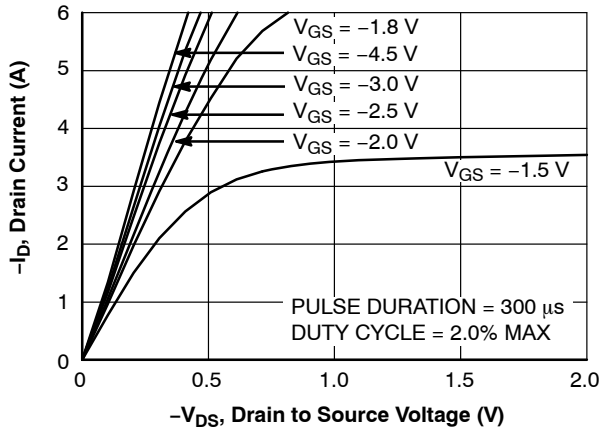



**Figure 1. On−Region Characteristics**

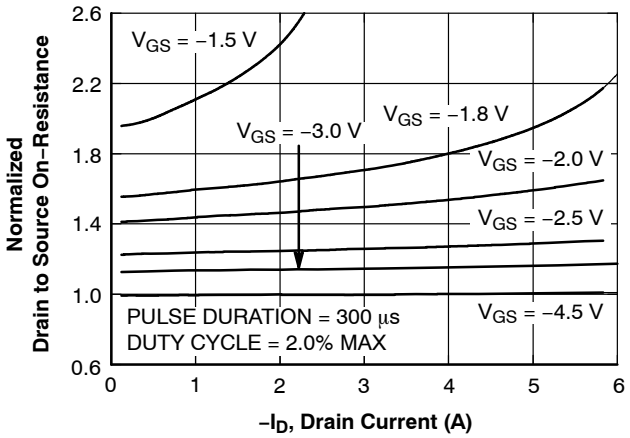



**Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage**

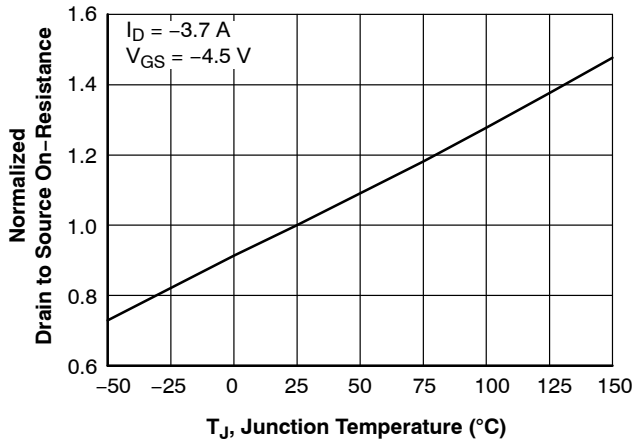



**Figure 3. Normalized On−Resistance vs. Junction Temperature**

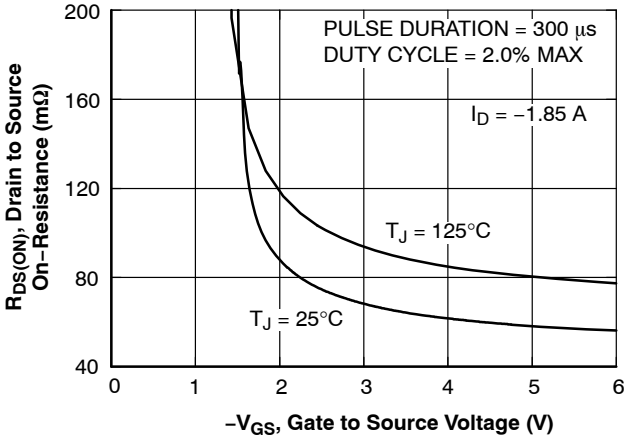



**Figure 4. On−Resistance vs. Gate to Source Voltage**

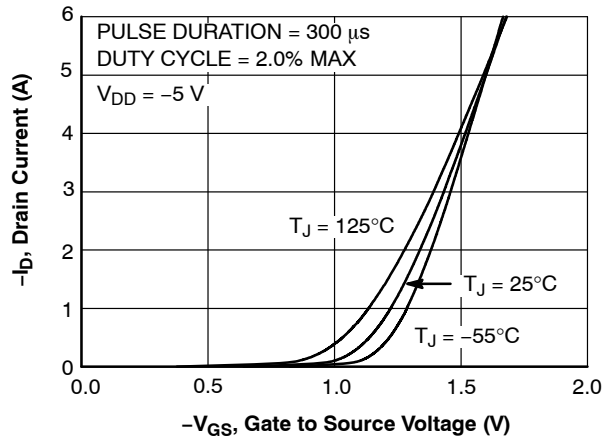



**Figure 5. Transfer Characteristics**

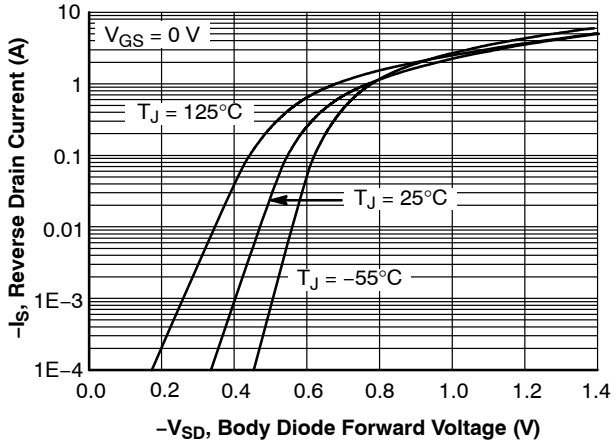



**Figure 6. Source to Drain Diode Forward Voltage vs. Source Current**

## TYPICAL CHARACTERISTICS ($T_J$ = 25°C unless otherwise noted) (continued)

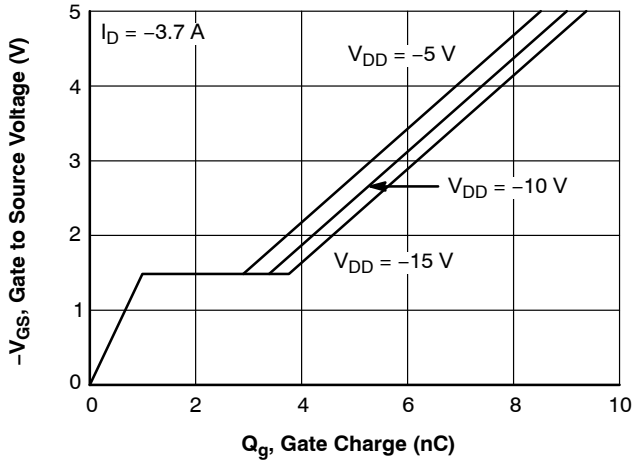



**Figure 7. Gate Charge Characteristics**

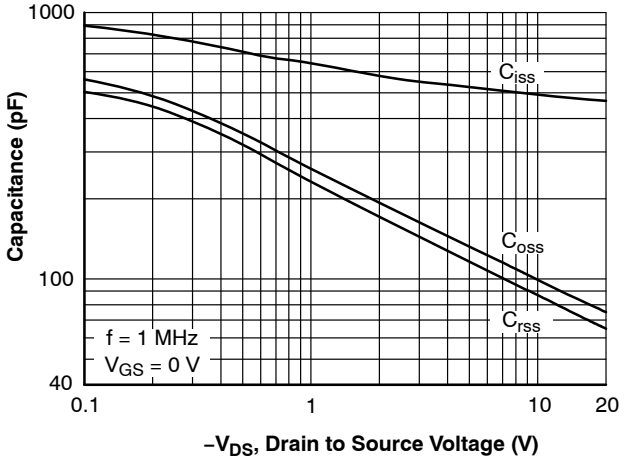



**Figure 8. Capacitance Characteristics**

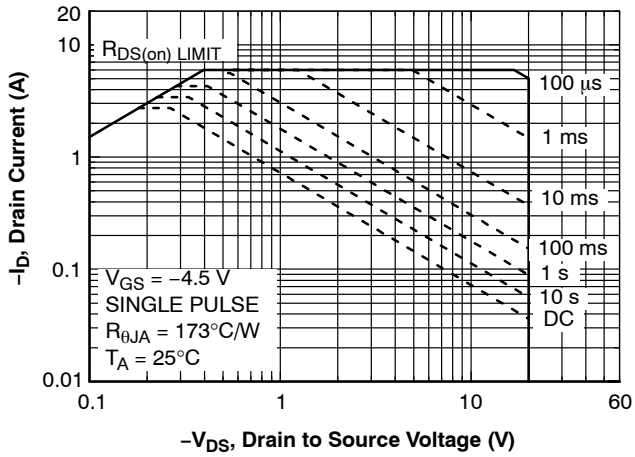



**Figure 9. Forward Bias Safe Operating Area**

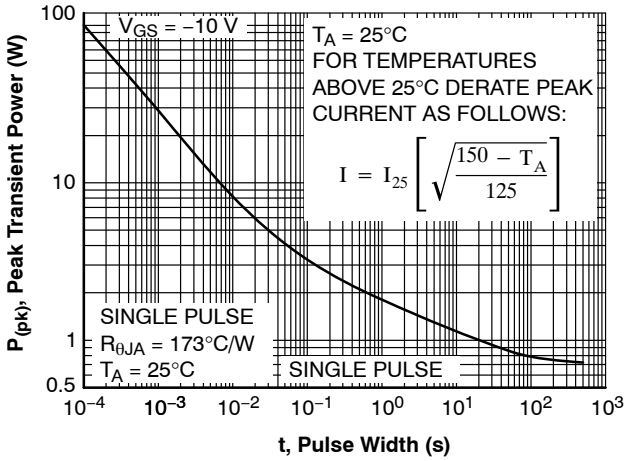



**Figure 10. Single Pulse Maximum Power Dissipation**

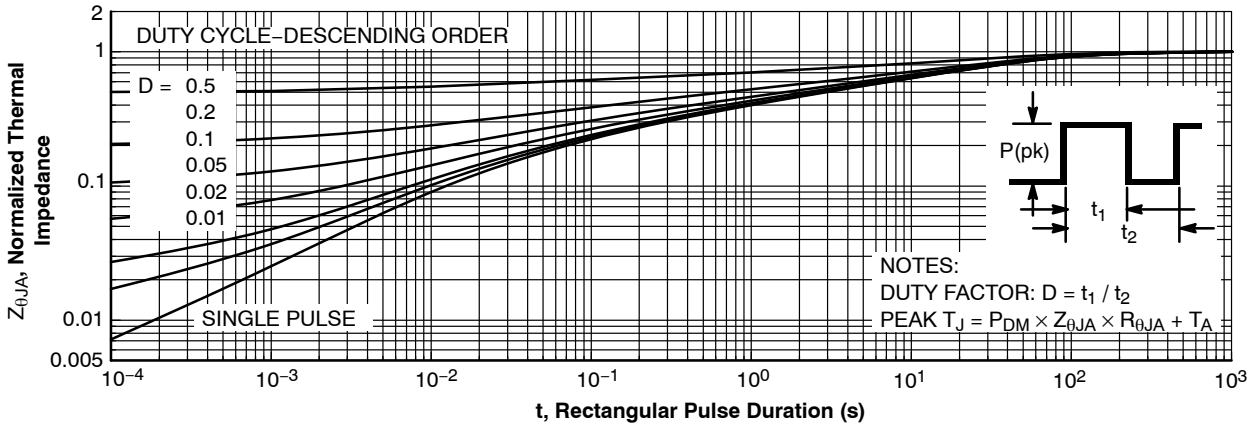
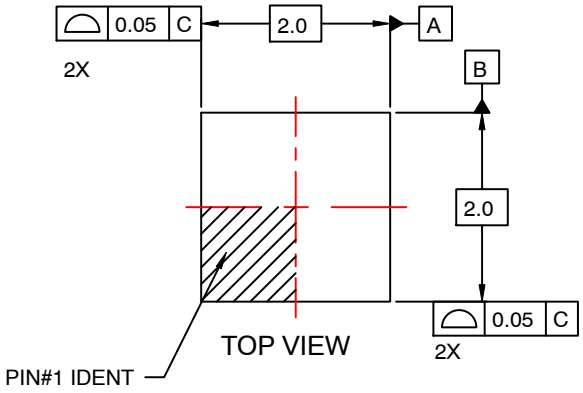


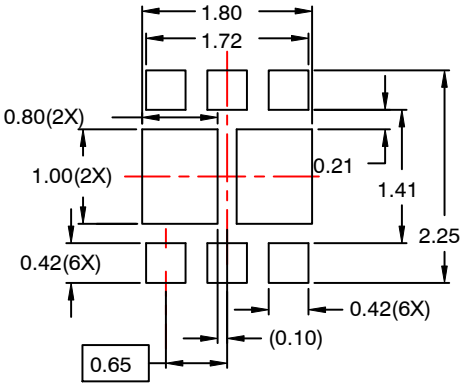

**Figure 11. Transient Thermal Response Curve**

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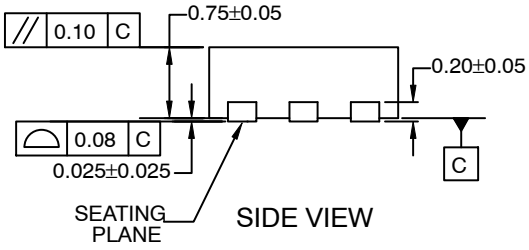
**WDFN6 2x2, 0.65P**
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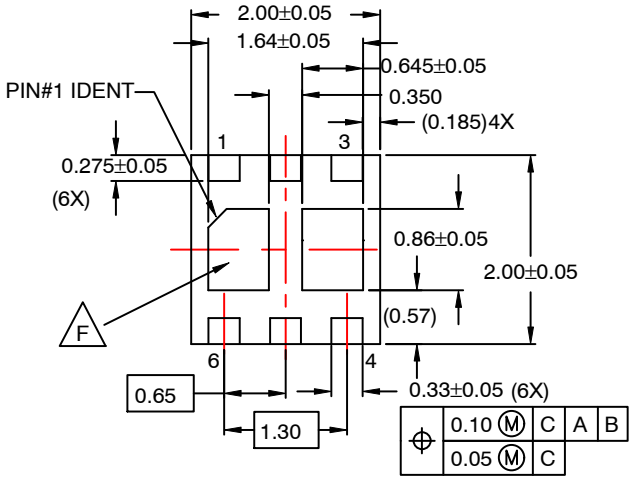
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B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

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