# TinyLogic UHS Dual Unbuffered Inverter

# NC7WZU04

## Description

The NC7WZU04 is a dual unbuffered inverter from **onsemi**'s Ultra High Speed Series of TinyLogic in the space saving SC−88 6−lead package. The special purpose unbuffered circuit design is intended for crystal oscillator or analog applications. The internal circuit consists of only one−stage, the output, to allow for this part to be used in these oscillator or analog applications. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive while maintaining low static power dissipation over a very broad $V_{CC}$ operating range. The device is specified to operate over the 1.65 V to 5.5 V $V_{CC}$ range. The inputs are high impedance when $V_{CC}$ is 0 V. Inputs tolerate voltages up to 5.5 V independent of $V_{CC}$ operating voltage.

## Features

- Space−Saving SC−88 6−Lead Package
- Ultra−Small MicroPak™ Leadless Packages
- Unbuffered for Crystal Oscillator and Analog Applications
- Balanced Output Drive: ±32 mA at 4.5 V $V_{CC}$
- Broad $V_{CC}$ Operating Range: 1.65 V to 5.5 V
- Low Quiescent Power: $I_{CC}$ < 1 μA at 5 V $V_{CC}$, $T_A$ = 25°C
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

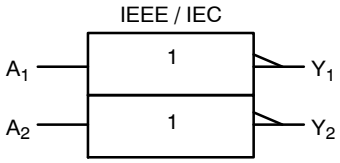
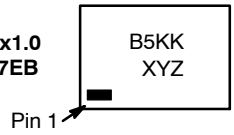


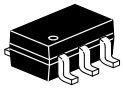

**Figure 1. Logic Symbol**

## MARKING DIAGRAMS

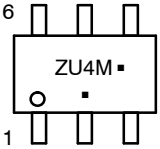


**SIP6 1.45x1.0**
**CASE 127EB**



**SC−88**
**CASE 419B−02**




| | |
|---|---|
| B5, ZU4 | = Specific Device Code |
| KK | = 2−Digit Lot Run Traceability Code |
| XY | = 2−Digit Date Code Format |
| Z | = Assembly Plant Code |
| M | = Data Code* |
| ▪ | = Pb−Free Package |

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

## ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 6 of this data sheet.

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## Pin Configurations

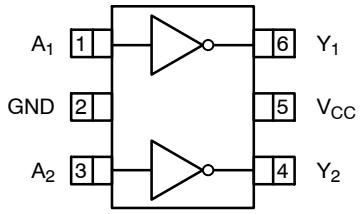



**Figure 2. SC−88 (Top View)**

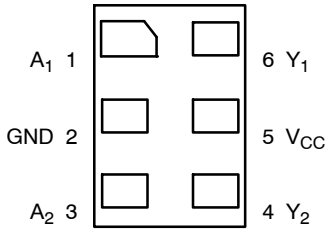
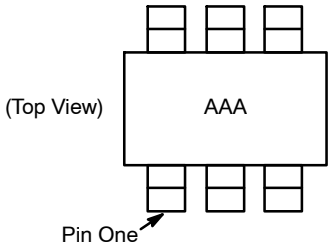



**Figure 3. MicroPak (Top Through View)**




AAA represents Product Code Top Mark − see ordering code

NOTE: Orientation of Top Mark determines Pin One location. Reading the top product code mark left to right, Pin One is the lower left pin (see diagram).

**Figure 4. SC−88 Pin 1 Orientation**

### PIN DEFINITIONS

| Pin Name | Description |
|---|---|
| $A_1$, $A_2$ | Data Inputs |
| $Y_1$, $Y_2$ | Outputs |

### FUNCTION TABLE ($Y = \overline{A}$)

| Input | Output |
|---|---|
| **A** | **Y** |
| L | H |
| H | L |

H = HIGH Logic Level
L = LOW Logic Level

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | −0.5 | 6.5 | V |
| $V_{IN}$ | DC Input Voltage | | −0.5 | 6.5 | V |
| $V_{OUT}$ | DC Output Voltage | | −0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | DC Input Diode Current | $V_{IN}$ < 0 V | − | −50 | mA |
| $I_{OK}$ | DC Output Diode Current | $V_{OUT}$ < 0 V | − | −50 | mA |
| | | $V_{OUT}$ > $V_{CC}$ | − | +50 | mA |
| $I_{OUT}$ | DC Output Current | | − | ±50 | mA |
| $I_{CC}$ or $I_{GND}$ | DC $V_{CC}$ / GND Current | | − | ±50 | mA |
| $T_{STG}$ | Storage Temperature | | −65 | +150 | °C |
| $T_J$ | Junction Temperature Under Bias | | − | 150 | °C |
| $T_L$ | Junction Lead Temperature (Soldering, 10 Seconds) | | − | 260 | °C |
| $P_D$ | Power Dissipation in Still Air | SC−88 | − | 332 | mW |
| | | MicroPak−6 | − | 812 | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage Operating | | 1.65 | 5.5 | V |
| | Supply Voltage Data Retention | | 1.5 | 5.5 | |
| $V_{IN}$ | Input Voltage | | 0 | 5.5 | V |
| $V_{OUT}$ | Output Voltage | | 0 | $V_{CC}$ | V |
| $T_A$ | Operating Temperature | | −40 | +85 | °C |
| $\theta_{JA}$ | Thermal Resistance | SC−88 | − | 377 | °C/W |
| | | MicroPak−6 | − | 154 | |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. Unused inputs must be held HIGH or LOW. They may not float.

## DC ELECTRICAL CHARACTERISTICS

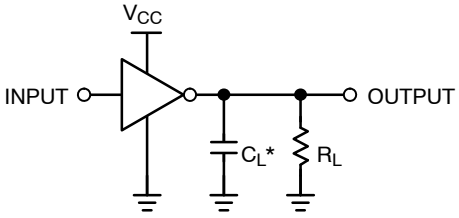
| Symbol | Parameter | Conditions | $V_{CC}$ (V) | $T_A$ = +25°C | | | $T_A$ = −40 to +85°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Max | |
| $V_{IH}$ | HIGH Level Input Voltage | | 1.8 to 2.7 | 0.85 $V_{CC}$ | – | – | 0.85 $V_{CC}$ | – | V |
| | | | 3.0 to 5.5 | 0.8 $V_{CC}$ | – | – | 0.8 $V_{CC}$ | – | |
| $V_{IL}$ | LOW Level Input Voltage | | 1.8 to 2.7 | – | – | 0.15 $V_{CC}$ | – | 0.15 $V_{CC}$ | V |
| | | | 3.0 to 5.5 | – | – | 0.2 $V_{CC}$ | – | 0.2 $V_{CC}$ | |
| $V_{OH}$ | High−Level Output Voltage | $V_{IN}$ = GND<br>$I_{OH}$ = −100 μA<br>$I_{OH}$ = −4 mA<br>$I_{OH}$ = −8 mA<br>$I_{OH}$ = −12 mA<br>$I_{OH}$ = −16 mA<br>$I_{OH}$ = −24 mA<br>$I_{OH}$ = −32 mA | <br>1.65 to 5.5<br>1.65<br>2.3<br>2.7<br>3.0<br>3.0<br>4.5 | <br>$V_{CC}$ − 0.1<br>1.29<br>1.9<br>2.2<br>2.4<br>2.3<br>3.8 | <br>$V_{CC}$<br>1.4<br>2.1<br>2.4<br>2.7<br>2.5<br>4.0 | <br>–<br>–<br>–<br>–<br>–<br>–<br>– | <br>$V_{CC}$ − 0.1<br>1.29<br>1.9<br>2.2<br>2.4<br>2.3<br>3.8 | <br>–<br>–<br>–<br>–<br>–<br>–<br>– | V |
| $V_{OL}$ | Low−Level Output Voltage | $V_{IN}$ = $V_{CC}$<br>$I_{OL}$ = 100 μA<br>$I_{OL}$ = 4 mA<br>$I_{OL}$ = 8 mA<br>$I_{OL}$ = 12 mA<br>$I_{OL}$ = 16 mA<br>$I_{OL}$ = 24 mA<br>$I_{OL}$ = 32 mA | <br>1.65 to 5.5<br>1.65<br>2.3<br>2.7<br>3.0<br>3.0<br>4.5 | <br>–<br>–<br>–<br>–<br>–<br>–<br>–<br>– | <br>–<br>0.08<br>0.2<br>0.22<br>0.28<br>0.38<br>0.42 | <br>0.1<br>0.24<br>0.3<br>0.4<br>0.4<br>0.55<br>0.55 | <br>–<br>–<br>–<br>–<br>–<br>–<br>– | <br>0.1<br>0.24<br>0.3<br>0.4<br>0.4<br>0.55<br>0.55 | V |
| $I_{IN}$ | Input Leakage Current | $V_{IN}$ = 5.5 V, GND | 1.65 to 5.5 | – | – | ±0.1 | – | ±1.0 | μA |
| $I_{CC}$ | Quiescent Supply Current | $V_{IN}$ = 5.5 V, GND | 1.65 to 5.5 | – | – | 1.0 | – | 10 | μA |

## AC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | $V_{CC}$ (V) | Conditions | $T_A$ = +25°C | | | $T_A$ = −40 to +85°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Max | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay (Figure 5, 6) | 1.65 | $C_L$ = 15 pF, $R_L$ = 1 MΩ | – | 5.5 | 9.8 | – | 11.0 | ns |
| | | 1.8 | | – | 4.6 | 8.1 | – | 8.9 | |
| | | 2.5 ±0.2 | | – | 3.3 | 5.7 | – | 6.3 | |
| | | 3.3 ±0.3 | | – | 2.7 | 4.1 | – | 4.5 | |
| | | 5.0 ±0.5 | | – | 2.2 | 3.3 | – | 3.6 | |
| | | 3.3 ±0.3 | $C_L$ = 50 pF, $R_L$ = 500 Ω | – | 4.0 | 6.4 | – | 7.0 | |
| | | 5.0 ±0.5 | | – | 3.4 | 5.6 | – | 6.2 | |
| $C_{IN}$ | Input Capacitance | 0 | | – | 3 | – | – | – | pF |
| $C_{PD}$ | Power Dissipation Capacitance (Figure 7) | 3.3 | (Note 2) | – | 3.5 | – | – | – | pF |
| | | 5.0 | | – | 5.5 | – | – | – | |

2. $C_{PD}$ is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption ($I_{CCD}$) at no output loading and operating at 50% duty cycle. $C_{PD}$ is related to $I_{CCD}$ dynamic operating current by the expression: $I_{CCD} = (C_{PD})\ (V_{CC})\ (f_{IN}) + (I_{CC}static)$.

### AC Loading and Waveforms




*$C_L$ includes load and stray capacitance.
Input PRR = 1.0 MHz, $t_W$ = 500 ns.

**Figure 5. AC Test Circuit**

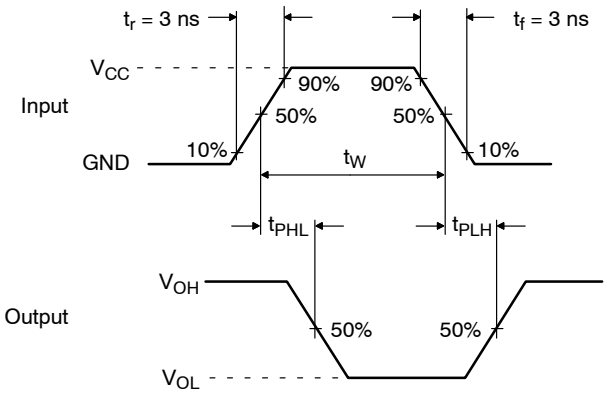
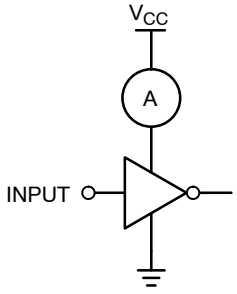



**Figure 6. AC Waveforms**




*Application Note:* When operating the NC7WZU04's unbuffered output stage in its linear range, as in oscillator applications, care must be taken to observe maximum power rating for the device and package. The high drive nature of the design of the output stage will result in substantial simultaneous conduction currents when the stage is in the linear region. See the $I_{CCPEAK}$ specification on page 4.

Input = AC Waveform; $t_r = t_f$ = 1.8 ns.
PRR = 10 MHz; Duty Cycle = 50%.

**Figure 7. $I_{CCD}$ Test Circuit**

## DEVICE ORDERING INFORMATION

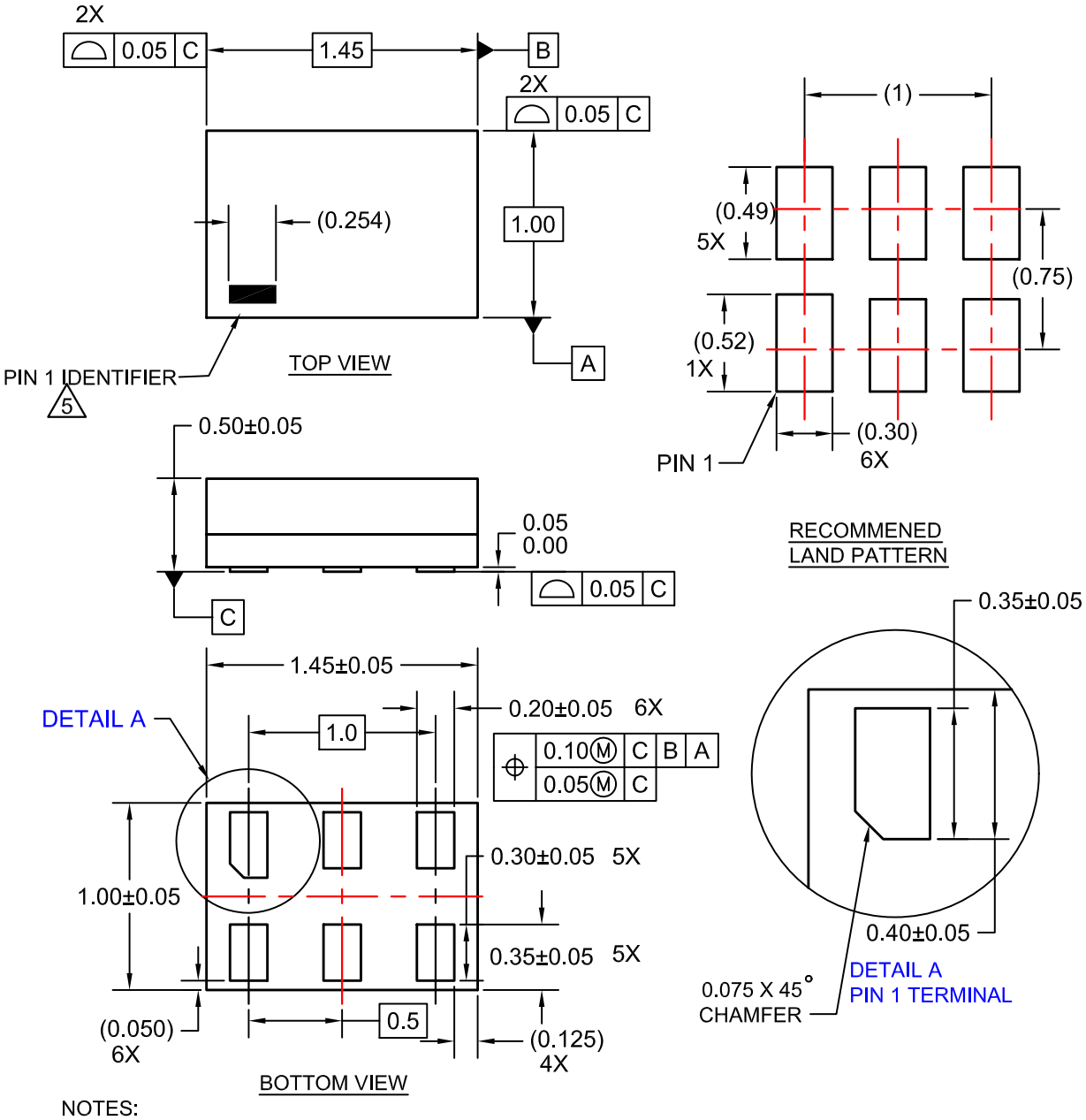
| Device | Top Mark | Packages | Shipping† |
|---|---|---|---|
| NC7WZU04P6X | ZU4 | SC−88 | 3000 / Tape & Reel |
| NC7WZU04L6X | B5 | MicroPak | 5000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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**SIP6 1.45X1.0**
CASE 127EB
ISSUE O

DATE 31 AUG 2016




NOTES:

1. CONFORMS TO JEDEC STANDARD MO-252 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-2009
4. PIN ONE IDENTIFIER IS 2X LENGTH OF ANY OTHER LINE IN THE MARK CODE LAYOUT.

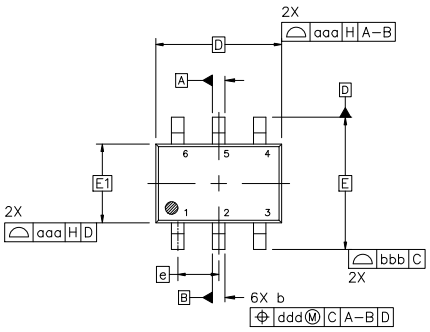
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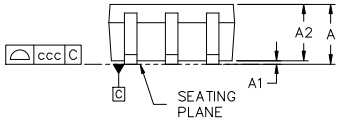


**SC−88 2.00x1.25x0.90, 0.65P**
CASE 419B−02
ISSUE Z

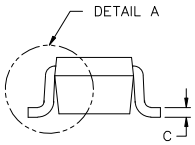
DATE 18 APR 2024



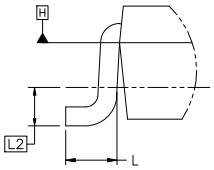

TOP VIEW




SIDE VIEW




END VIEW

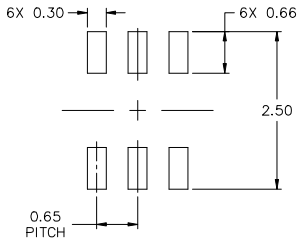



DETAIL A
SCALE 2:1

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

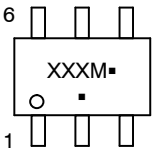
| | MILLIMETERS | | |
|---|---|---|---|
| DIM | MIN. | NOM. | MAX. |
| A | −−− | −−− | 1.10 |
| A1 | 0.00 | −−− | 0.10 |
| A2 | 0.70 | 0.90 | 1.00 |
| b | 0.15 | 0.20 | 0.25 |
| c | 0.08 | 0.15 | 0.22 |
| D | 2.00 BSC | | |
| E | 2.10 BSC | | |
| E1 | 1.25 BSC | | |
| e | 0.65 BSC | | |
| L | 0.26 | 0.36 | 0.46 |
| L2 | 0.15 BSC | | |
| aaa | 0.15 | | |
| bbb | 0.30 | | |
| ccc | 0.10 | | |
| ddd | 0.10 | | |




RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

## GENERIC MARKING DIAGRAM*




XXX = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

**STYLES ON PAGE 2**

| | | | |
|---|---|---|---|
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| **DESCRIPTION:** | **SC−88 2.00x1.25x0.90, 0.65P** | | **PAGE 1 OF 2** |

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**SC−88 2.00x1.25x0.90, 0.65P**
CASE 419B−02
ISSUE Z

DATE 18 APR 2024

STYLE 1:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 2:
CANCELLED

STYLE 3:
CANCELLED

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. COLLECTOR
4. EMITTER
5. BASE
6. ANODE

STYLE 5:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 6:
PIN 1. ANODE 2
2. N/C
3. CATHODE 1
4. ANODE 1
5. N/C
6. CATHODE 2

STYLE 7:
PIN 1. SOURCE 2
2. DRAIN 2
3. GATE 1
4. SOURCE 1
5. DRAIN 1
6. GATE 2

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. EMITTER 2
2. EMITTER 1
3. COLLECTOR 1
4. BASE 1
5. BASE 2
6. COLLECTOR 2

STYLE 10:
PIN 1. SOURCE 2
2. SOURCE 1
3. GATE 1
4. DRAIN 1
5. DRAIN 2
6. GATE 2

STYLE 11:
PIN 1. CATHODE 2
2. CATHODE 2
3. ANODE 1
4. CATHODE 1
5. CATHODE 1
6. ANODE 2

STYLE 12:
PIN 1. ANODE 2
2. ANODE 2
3. CATHODE 1
4. ANODE 1
5. ANODE 1
6. CATHODE 2

STYLE 13:
PIN 1. ANODE
2. N/C
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 14:
PIN 1. VREF
2. GND
3. GND
4. IOUT
5. VEN
6. VCC

STYLE 15:
PIN 1. ANODE 1
2. ANODE 2
3. ANODE 3
4. CATHODE 3
5. CATHODE 2
6. CATHODE 1

STYLE 16:
PIN 1. BASE 1
2. EMITTER 2
3. COLLECTOR 2
4. BASE 2
5. EMITTER 1
6. COLLECTOR 1

STYLE 17:
PIN 1. BASE 1
2. EMITTER 1
3. COLLECTOR 2
4. BASE 2
5. EMITTER 2
6. COLLECTOR 1

STYLE 18:
PIN 1. VIN1
2. VCC
3. VOUT2
4. VIN2
5. GND
6. VOUT1

STYLE 19:
PIN 1. I OUT
2. GND
3. GND
4. V CC
5. V EN
6. V REF

STYLE 20:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 21:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. N/C
6. CATHODE 1

STYLE 22:
PIN 1. D1 (i)
2. GND
3. D2 (i)
4. D2 (c)
5. VBUS
6. D1 (c)

STYLE 23:
PIN 1. Vn
2. CH1
3. Vp
4. N/C
5. CH2
6. N/C

STYLE 24:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 25:
PIN 1. BASE 1
2. CATHODE
3. COLLECTOR 2
4. BASE 2
5. EMITTER
6. COLLECTOR 1

STYLE 26:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 27:
PIN 1. BASE 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. EMITTER 2
6. COLLECTOR 2

STYLE 28:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 29:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE/ANODE
6. CATHODE

STYLE 30:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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| **DESCRIPTION:** | **SC−88 2.00x1.25x0.90, 0.65P** | | **PAGE 2 OF 2** |

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