2.5 V / 3.3 V 1:2 Differential CML Fanout Buffer

Multi−Level Inputs w/ Internal Termination

NB6L11M

Description

The NB6L11M is a differential 1:2 CML fanout buffer. The differential inputs incorporate internal 50 Ω termination resistors that are accessed through the V_T pins and will accept LVPECL, LVCMOS, LVTTL, CML, or LVDS logic levels.

The V_{REFAC} pin is an internally generated voltage supply available to this device only. V_{REFAC} is used as a reference voltage for single−ended PECL or NECL inputs. For all single−ended input conditions, the unused complementary differential input is connected to V_{REFAC} as a switching reference voltage. V_{REFAC} may also rebias capacitor−coupled inputs. When used, decouple V_{REFAC} with a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{REFAC} output should be left open.

The device is housed in a small 3x3 mm 16 pin QFN package.

The NB6L11M is a member of the ECLinPS MAX™ family of high performance clock products.

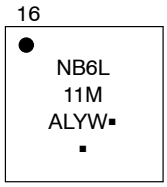
Features

- Maximum Input Clock Frequency > 4 GHz, Typical
- 225 ps Typical Propagation Delay
- 70 ps Typical Rise and Fall Times
- 0.5 ps maximum RMS Clock Jitter
- Differential CML Outputs, 380 mV peak−to−peak, typical
- LVPECL Operating Range: V_{CC} = 2.375 V to 3.63 V with V_{EE} = 0 V
- NECL Operating Range: V_{CC} = 0 V with V_{EE} = −2.375 V to −3.63 V
- Internal Input Termination Resistors, 50 Ω
- VREFAC Reference Output
- Functionally Compatible with Existing 2.5 V / 3.3V LVEL, LVEP, EP, and SG Devices
- −40°C to +85°C Ambient Operating Temperature
- These are Pb−Free Devices



QFN16 3 × 3, 0.5P
MN SUFFIX
CASE 485G

MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

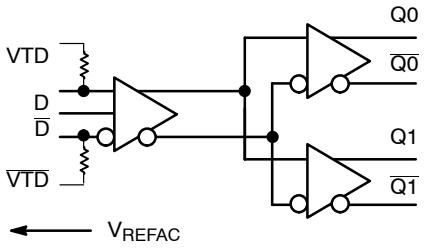


Figure 1. Simplified Logic Diagram

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

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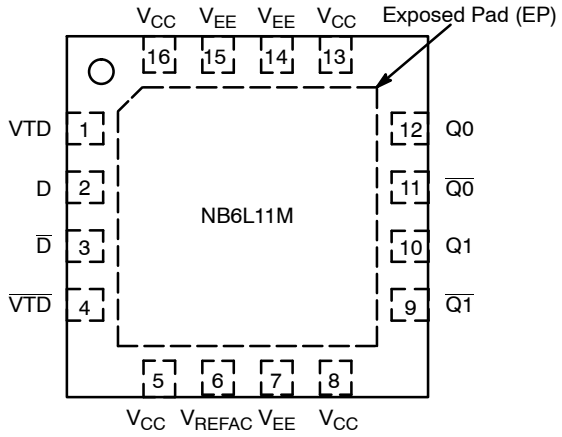


Figure 2. Pin Configuration (Top View)

Table 1. PIN DESCRIPTION

Pin	Name	I/O	Description
1	VTD	–	Internal 50 Ω Termination Pin for D input.
2	D	ECL, CML, LVCMOS, LVDS, LVTTL Input	Noninverted Differential Input. Note 1. Internal 50 Ω Resistor to Termination Pin, VTD.
3	$\overline{D}$	ECL, CML, LVCMOS, LVDS, LVTTL Input	Inverted Differential Input. Note 1. Internal 50 Ω Resistor to Termination Pin, $\overline{VTD}$.
4	$\overline{VTD}$	–	Internal 50 Ω Termination Pin for $\overline{D}$ input.
5	V_{CC}	–	Positive Supply Voltage
6	V_{REFAC}		Output Reference Voltage for direct or capacitor coupled inputs
7	V_{EE}	–	Negative Supply Voltage
8	V_{CC}	–	Positive Supply Voltage
9	$\overline{Q1}$	CML Output	Inverted Differential Output. Typically Terminated with 50 Ω Resistor to V_{CC}.
10	Q1	CML Output	Noninverted Differential Output. Typically Terminated with 50 Ω Resistor to V_{CC}.
11	$\overline{Q0}$	CML Output	Inverted Differential Output. Typically Terminated with 50 Ω Resistor to V_{CC}.
12	Q0	CML Output	Noninverted Differential Output. Typically Terminated with 50 Ω Resistor to V_{CC}.
13	V_{CC}	–	Positive Supply Voltage
14	V_{EE}	–	Negative Supply Voltage
15	V_{EE}	–	Negative Supply Voltage
16	V_{CC}	–	Positive Supply Voltage
–	EP	–	The Exposed Pad (EP) on the QFN−16 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat−sinking conduit. The pad is not electrically connected to the die, but is recommended to be electrically and thermally connected to VEE on the PC board.

1. In the differential configuration when the input termination pins (VTD, $\overline{VTD}$) are connected to a common termination voltage or left open, and if no signal is applied on D/$\overline{D}$ input, then, the device will be susceptible to self−oscillation.
2. All V_{CC} and V_{EE} pins must be externally connected to a power supply for proper operation.

Table 2. ATTRIBUTES

Characteristics		Value
ESD Protection	Human Body Model Machine Model	> 2 kV > 200V
Moisture Sensitivity	16−QFN	Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count		
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

For additional information, see Application Note AND8003/D.

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Positive Power Supply	V_{EE} = 0 V		4.0	V
V_{EE}	Negative Power Supply	V_{CC} = 0 V		−4.0	V
V_{IO}	Positive Input/Output Voltage Negative Input/Output Voltage	V_{EE} = 0 V V_{CC} = 0 V	$-0.5 \le V_{Io} \le V_{CC} + 0.5$ $+0.5 \le V_{Io} \le V_{EE} - 0.5$	4.0 −4.0	V V
V_{INPP}	Differential Input Voltage $\|D - \overline{D}\|$			$V_{CC} - V_{EE}$	V
I_{IN}	Input Current Through R_T (50 Ω Resistor)	Static Surge		45 80	mA mA
I_{OUT}	Output Current (CML Output)	Continuous Surge		25 50	mA mA
I_{VREFAC}	VREFAC Sink/Source Current			±0.5	mA
T_A	Operating Temperature Range	16 QFN		−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient) (Note 3)	0 lfmp 500 lfmp	QFN−16 QFN−16	42 35	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	(Note 3)	QFN−16	4	°C/W
T_{sol}	Wave Solder Pb−Free			265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3. JEDEC standard multilayer board − 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

Table 4. DC CHARACTERISTICS, Multi−Level Inputs V_{CC} = 2.375 V to 3.63 V, V_{EE} = 0 V, or V_{CC} = 0 V, V_{EE} = −2.375 V to −3.63 V, T_A = −40°C to +85°C

Symbol	Characteristic	Min	Typ	Max	Unit
POWER SUPPLY CURRENT					
I_{CC}	Power Supply Current (Inputs and Outputs Open)	45	60	75	mA
CML OUTPUTS (Notes 4 and 5)					
V_{OH}	Output HIGH Voltage V_{CC} = 3.3 V V_{CC} = 2.5 V	V_{CC} − 40 3260 2460	V_{CC} − 10 3290 2490	V_{CC} 3300 2500	mV
V_{OL}	Output LOW Voltage V_{CC} = 3.3V V_{CC} = 2.5V	V_{CC} − 500 2800 2000	V_{CC} − 400 2900 2100	V_{CC} − 300 3000 2200	mV
DIFFERENTIAL INPUT DRIVEN SINGLE−ENDED (see Figures 4 and 5) (Note 6)					
V_{th}	Input Threshold Reference Voltage Range (Note 7)	1125		V_{CC} − 75	mV
V_{IH}	Single−ended Input HIGH Voltage	V_{th} + 75		V_{CC}	mV
V_{IL}	Single−ended Input LOW Voltage	V_{EE}		V_{th} − 75	mV
V_{ISE}	Single−ended Input Voltage Amplitude (V_{IH} − V_{IL})	150		2800	mV
VREFAC					
V_{REFAC}	Output Reference Voltage (V_{CC} ≥ 2.5 V)	V_{CC} − 1525	V_{CC} − 1425	V_{CC} − 1325	mV
DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (see Figures 6, 7 and 8) (Note 8)					
V_{IHD}	Differential Input HIGH Voltage	V_{EE} + 1200		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage	V_{EE}		V_{CC} − 100	mV
V_{ID}	Differential Input Voltage (V_{IHD} − V_{ILD})	V_{EE} + 100		V_{CC} − V_{EE}	mV
V_{CMR}	Input Common Mode Range (Differential Configuration) (Note 9)	V_{EE} + 950		V_{CC} − 50	mV
I_{IH}	Input HIGH Current D / $\overline{D}$, (VTD/$\overline{VTD}$ Open)	−150		150	uA
I_{IL}	Input LOW Current D / $\overline{D}$, (VTD/$\overline{VTD}$ Open)	−150		150	uA
TERMINATION RESISTORS					
R_{TIN}	Internal Input Termination Resistor	40	50	60	Ω
R_{TOUT}	Internal Output Termination Resistor	40	50	60	Ω

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

4. CML outputs loaded with 50 Ω to V_{CC} for proper operation.
5. Input and output parameters vary 1:1 with V_{CC}.
6. V_{th}, V_{IH}, $V_{IL,}$, and V_{ISE} parameters must be complied with simultaneously.
7. V_{th} is applied to the complementary input when operating in single−ended mode.
8. V_{IHD}, V_{ILD}, V_{ID} and V_{CMR} parameters must be complied with simultaneously.
9. V_{CMR} min varies 1:1 with V_{EE}, V_{CMR} maximum varies 1:1 with V_{CC}. The V_{CMR} range is referenced to the most positive side of the differential input signal.

Table 5. AC CHARACTERISTICS V_{CC} = 2.375 V to 3.63 V, V_{EE} = 0 V, or V_{CC} = 0 V, V_{EE} = −2.375 V to −3.63 V, T_A = −40°C to +85°C; (Note 10)

Symbol	Characteristic		Min	Typ	Max	Unit
V_{OUTPP}	Output Voltage Amplitude (@ $V_{INPP(MIN)}$ (Note 15) (See Figure 9)	$f_{in} \le 3.0$GHz $f_{in} \le 3.5$ GHz $f_{in} \le 4.0$ GHz	230 190 150	380 320 270		mV
t_{PD}	Propagation Delay	D to Q	175	225	325	ps
t_{SKEW}	Duty Cycle Skew (Note 11) Within Device Skew Device to Device Skew (Note 12)			5.0 3.0	15 15 80	ps
t_{DC}	Output Clock Duty Cycle (Reference Duty Cycle = 50%)	$f_{in} \le 4.0$GHz	40	50	60	%
t_{JITTER}	RMS Random Clock Jitter (Note 13) Peak−to−Peak Data Dependent Jitter (Note 14)	$f_{in} \le 4$GHz $f_{in} \le 4$Gb/s		0.2 40	0.5	ps
V_{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 15)		150		2800	mV
t_r t_f	Output Rise/Fall Times @ 0.5 GHz (20% − 80%)	Q, $\overline{Q}$		70	120	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

10. Measured by forcing V_{INPP} (MIN) from a 50% duty cycle clock source. All loading with an external R_L = 50 Ω to V_{CC}. Input edge rates 40 ps (20% − 80%).
11. Duty cycle skew is measured between differential outputs using the deviations of the sum of Tpw− and Tpw+ @ 0.5GHz.
12. Device to device skew is measured between outputs under identical transition @ 0.5 GHz.
13. Additive RMS jitter with 50% duty cycle clock signal.
14. Additive peak−to−peak data dependent jitter with input NRZ data at PRBS23.
15. Input and output voltage swing is a single−ended measurement operating in differential mode.

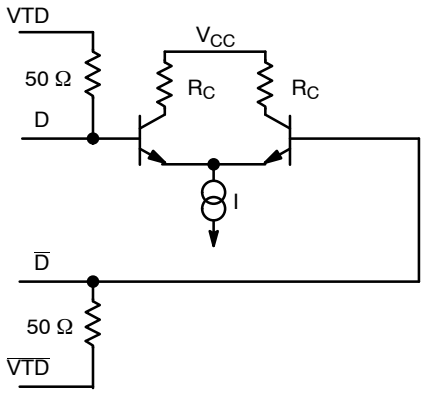


Figure 3. Input Structure

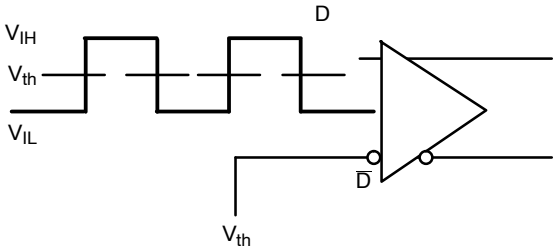


Figure 4. Differential Input Driven Single−Ended

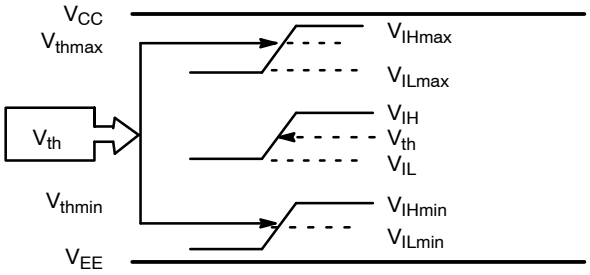


Figure 5. V_{th} Diagram

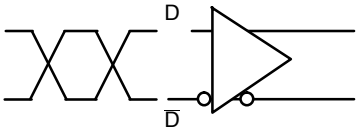


Figure 6. Differential Inputs Driven Differentially

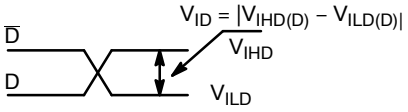


Figure 7. Differential Inputs Driven Differentially

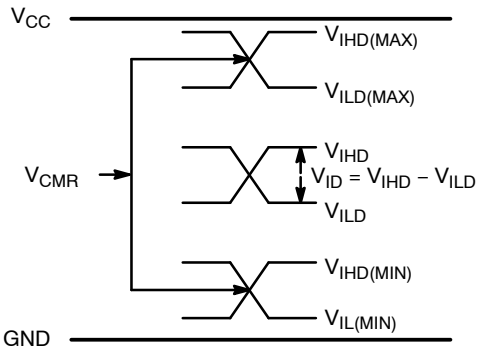


Figure 8. V_{CMR} Diagram

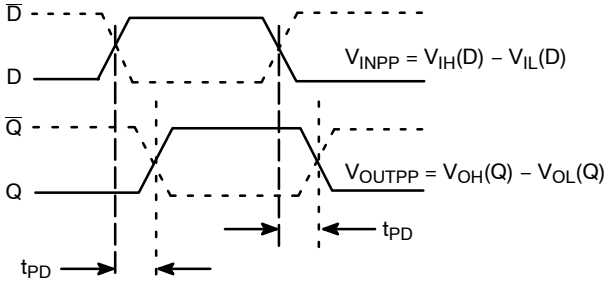


Figure 9. AC Reference Measurement

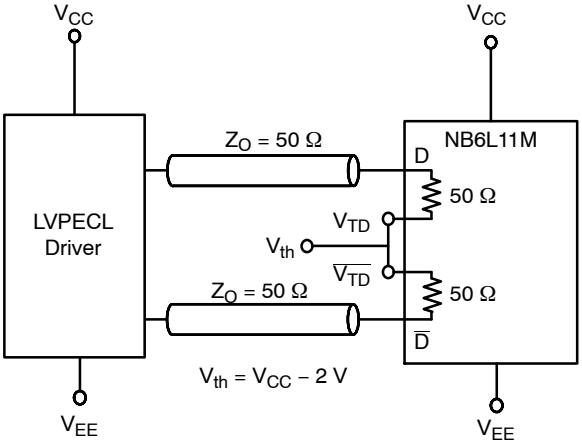


Figure 10. LVPECL Interface

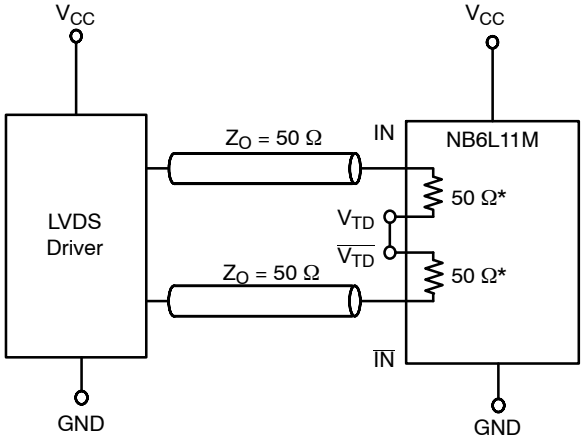


Figure 11. LVDS Interface

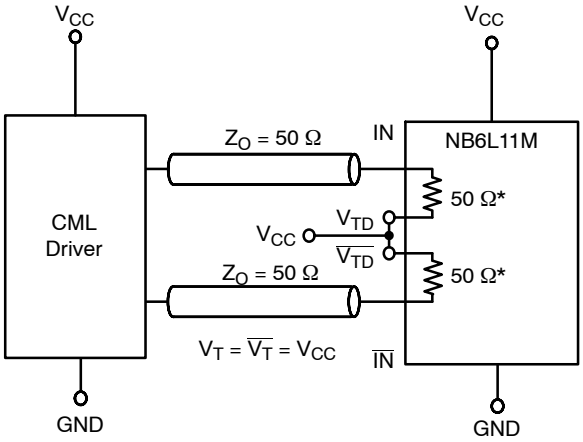


Figure 12. Standard 50 Ω Load CML Interface

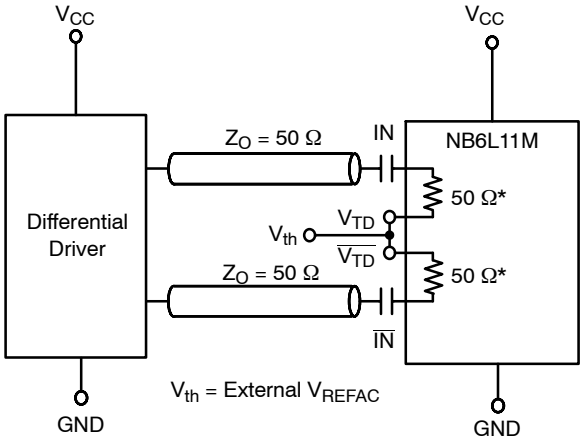


Figure 13. Capacitor−Coupled Differential Interface ($V_{TD}/\overline{V_{TD}}$ Connected to V_{REFAC}; V_{REFAC} Bypassed to Ground with 0.1 μF Capacitor)

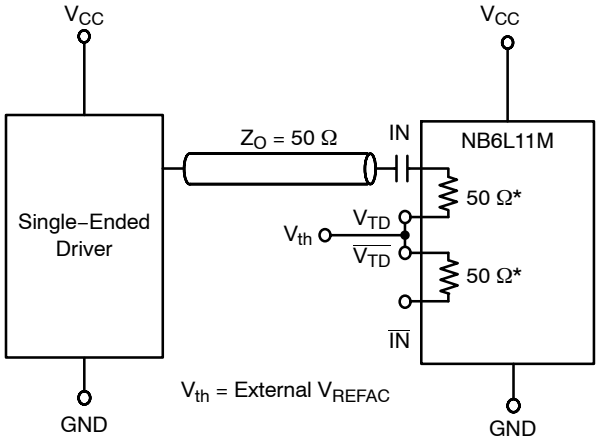


Figure 14. Capacitor−Coupled Single−Ended Interface ($V_T/\overline{V_T}$ Connected to V_{REFAC}; V_{REFAC} Bypassed to Ground with 0.1 μF Capacitor)

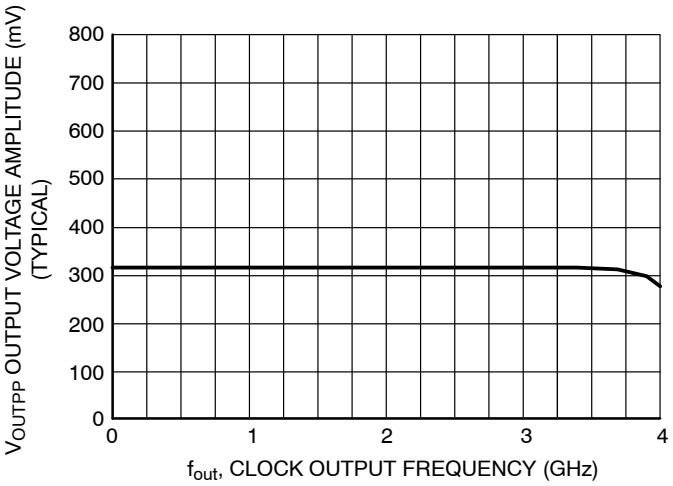


Figure 15. Output Voltage Amplitude (V_{OUTPP}) versus Output Frequency at Ambient Temperature (Typical)

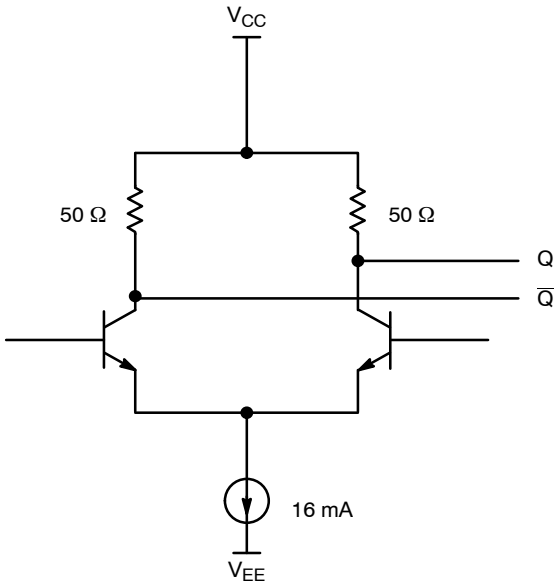


Figure 16. CML Output Structure

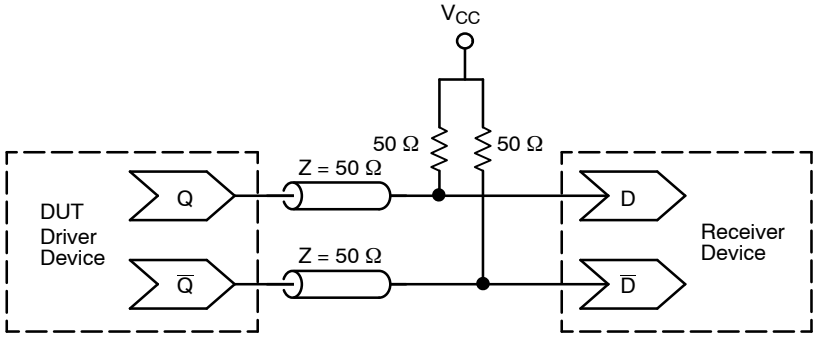


Figure 17. Typical CML Termination for Output Driver and Device Evaluation

ORDERING INFORMATION

Device	Package	Shipping†
NB6L11MMNG	QFN16 3 × 3, 0.5P (Pb−Free)	123 Units / Rail
NB6L11MMNR2G	QFN16 3 × 3, 0.5P (Pb−Free)	3000 / Tape & Reel

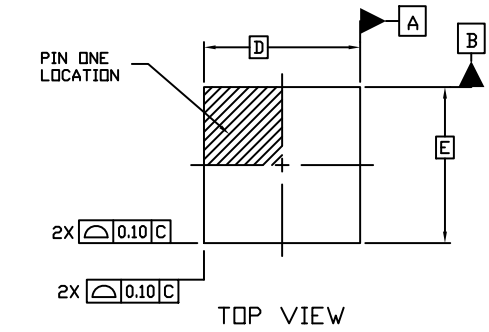
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

The products described herein (NB4L16M), may be covered by U.S. patents including 6,362,644. There may be other patents pending.
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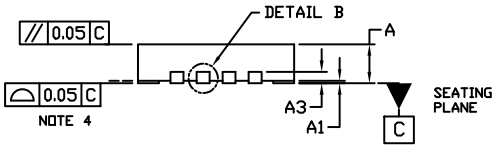
QFN16 3x3, 0.5P
CASE 485G
ISSUE G

DATE 08 OCT 2021

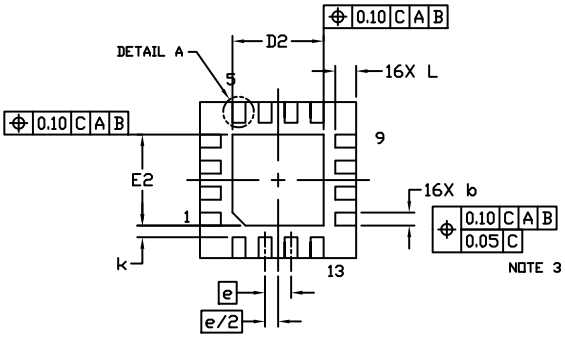
SCALE 2:1



TOP VIEW



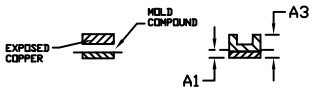
SIDE VIEW



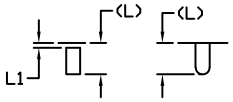
BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.



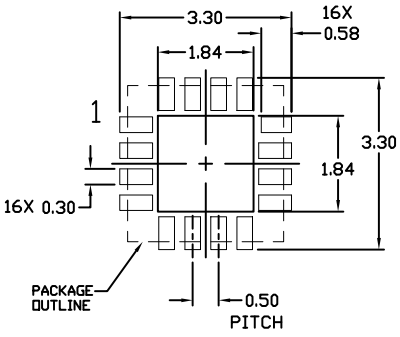
DETAIL B
ALTERNATE CONSTRUCTIONS



DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	0.03	0.05
A3		0.20 REF	
b	0.18	0.24	0.30
D		3.00 BSC	
D2	1.65	1.75	1.85
E		3.00 BSC	
E2	1.65	1.75	1.85
e		0.50 BSC	
k		0.18 TYP	
L	0.30	0.40	0.50
L1	0.00	0.08	0.15

MOUNTING FOOTPRINT



GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**QFN16 3X3, 0.5P**	**PAGE 1 OF 1**

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