

# Low-Voltage CMOS Octal Transceiver

With 5 V-Tolerant Inputs and Outputs  
(3-State, Non-Inverting)

## MC74LCX245

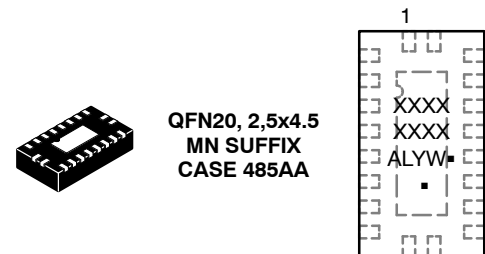
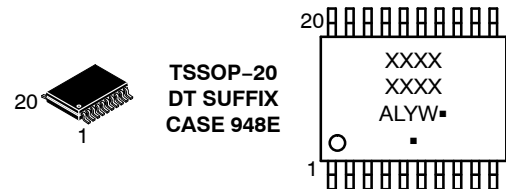
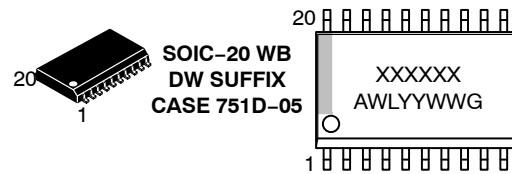
The MC74LCX245 is a high performance, non-inverting octal transceiver operating from a 1.65 to 5.5 V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A  $V_I$  specification of 5.5 V allows MC74LCX245 inputs to be safely driven from 5 V devices if  $V_{CC}$  is less than 5.0 V. The MC74LCX245 is suitable for memory address driving and all TTL level bus oriented transceiver applications.

Current drive capability is 24 mA at both A and B ports at  $V_{CC} = 3.0$  V. The Transmit/Receive (T/R) input determines the direction of data flow through the bi-directional transceiver. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a HIGH Z condition.

### Features

- Designed for 1.65 to 5.5 V  $V_{CC}$  Operation
- 5 V Tolerant – Interface Capability With 5 V TTL Logic
- Supports Live Insertion and Withdrawal
- $I_{OFF}$  Specification Guarantees High Impedance When  $V_{CC} = 0$  V
- LVTTL Compatible
- LVC MOS Compatible
- 24 mA Balanced Output Sink and Source Capability at  $V_{CC} = 3.0$  V
- Near Zero Static Supply Current in All Three Logic States (10  $\mu$ A) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 100 mA
- ESD Performance: Human Body Model > 2000 V
- Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### MARKING DIAGRAMS



XXXXXXXX = Specific Device Code  
 A = Assembly Location  
 L, WL = Wafer Lot  
 Y, YY = Year  
 W, WW = Work Week  
 G or ▪ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 7.

\*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC74LCX245

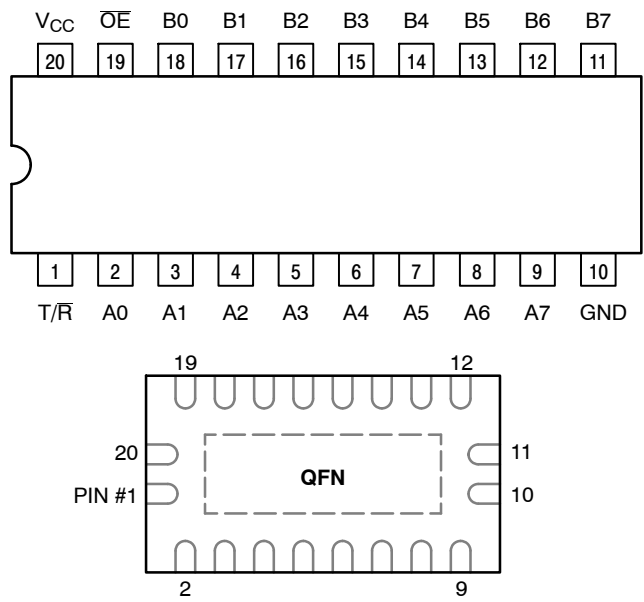


Figure 1. Pinout (Top View)

PIN NAMES

PINS	FUNCTION
OE	Output Enable Input
T/R	Transmit/Receive Input
A0–A7	Side A 3–State Inputs or 3–State Outputs
B0–B7	Side B 3–State Inputs or 3–State Outputs

TRUTH TABLE

INPUTS		OPERATING MODE Non-Inverting
OE	T/R	
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	Z

H = High Voltage Level  
L = Low Voltage Level  
Z = High Impedance State  
X = High or Low Voltage Level and Transitions are Acceptable  
For I<sub>CC</sub> reasons, Do Not Float Inputs

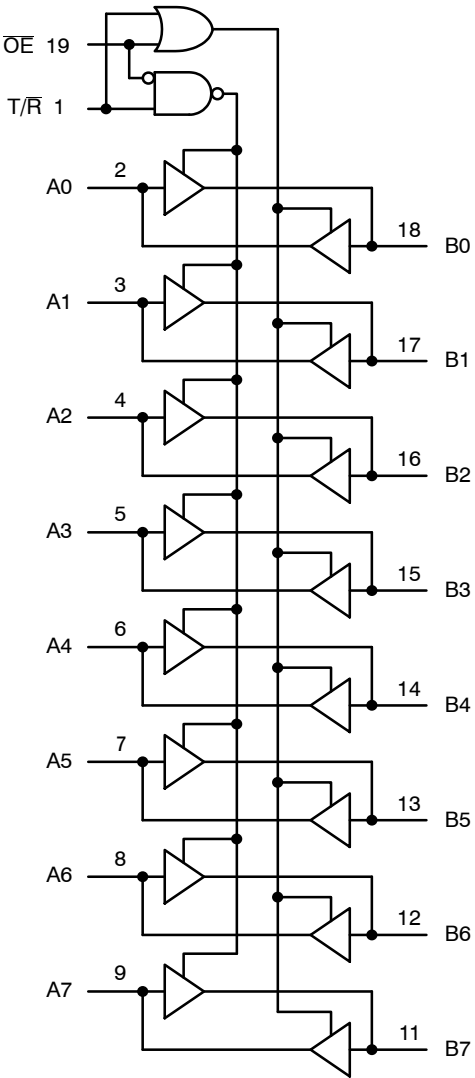


Figure 2. Logic Diagram

# MC74LCX245

## MAXIMUM RATINGS

Symbol	Parameter	Condition	Value	Unit
$V_{CC}$	DC Supply Voltage		-0.5 to +6.5	V
$V_I$	DC Input Voltage (Note 1)		-0.5 to +6.5	V
$V_O$	DC Output Voltage (Note 1)	Active-Mode (High or Low State)	-0.5 to $V_{CC} + 0.5$	V
		Tri-State Mode	-0.5 to +6.5	
		Power-Down Mode ( $V_{CC} = 0$ V)	-0.5 to +6.5	
$I_{IK}$	DC Input Diode Current	$V_{IN} < GND$	-50	mA
$I_{OK}$	DC Output Diode Current	$V_{OUT} < GND$	-50	mA
$I_O$	DC Output Source/Sink Current		$\pm 50$	mA
$I_{CC}$ or $I_{GND}$	DC Supply Current per Supply Pin or Ground Pin		$\pm 100$	mA
$T_{STG}$	Storage Temperature Range		-65 to +150	°C
$T_L$	Lead Temperature, 1 mm from Case for 10 secs		260	°C
$T_J$	Junction Temperature under Bias		+150	°C
$\theta_{JA}$	Thermal Resistance (Note 2)	SOIC-20W	96	°C/W
		WQFN20	99	
		QFN20	111	
		TSSOP-20	150	
$P_D$	Power Dissipation in Still Air	SOIC-20W	1302	mW
		WQFN20	1256	
		QFN20	1127	
		TSSOP-20	833	
MSL	Moisture Sensitivity	SOIC-20W	Level 3	-
		All other packages	Level 1	
$F_R$	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	-
$V_{ESD}$	ESD Withstand Voltage (Note 3)	Human Body Model	>2000	V
		Charged Device Model	N/A	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- $I_O$  absolute maximum rating must be observed.
- Measured with minimum pad spacing on an FR4 board, using 76 mm-by-114 mm, 2-ounce copper trace no air flow per JESD51-7.
- HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD20-A115A (Machine Model) be discontinued.

# MC74LCX245

## RECOMMENDED OPERATING CONDITIONS (Note 4)

Symbol	Parameter		Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	Operating	1.65	2.5, 3.3	5.5	V
		Data Retention Only	1.5	2.5, 3.3	5.5	
V <sub>I</sub>	Digital Input Voltage		0	–	5.5	V
V <sub>O</sub>	Output Voltage	Active-Mode (High or Low State)	0	–	V <sub>CC</sub>	V
		Tri-State Mode	0	–	5.5	
		Power-Down Mode (V <sub>CC</sub> = 0 V)	0	–	5.5	
T <sub>A</sub>	Operating Free-Air Temperature		–55		+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise or Fall Rate	V <sub>CC</sub> = 1.65 V to 1.95 V	0	–	20	ns/V
		V <sub>CC</sub> = 2.3 V to 2.7 V	0	–	20	
		V <sub>IN</sub> from 0.8 V to 2.0 V, V <sub>CC</sub> = 3.0 V	0	–	10	
		V <sub>CC</sub> = 4.5 V to 5.5 V	0	–	5	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = –40°C to +85°C		T <sub>A</sub> = –55°C to +125°C		Unit
				Min	Max	Min	Max	
V <sub>IH</sub>	High-Level Input Voltage		1.65 to 1.95	0.65 × V <sub>CC</sub>		0.65 × V <sub>CC</sub>		V
			2.3 to 2.7	1.7		1.7		
			2.7 to 3.6	2.0		2.0		
			4.5 to 5.5	0.7 × V <sub>CC</sub>		0.7 × V <sub>CC</sub>		
V <sub>IL</sub>	Low-Level Input Voltage		1.65 to 1.95		0.35 × V <sub>CC</sub>		0.35 × V <sub>CC</sub>	V
			2.3 to 2.7		0.7		0.7	
			2.7 to 3.6		0.8		0.8	
			4.5 to 5.5		0.3 × V <sub>CC</sub>		0.3 × V <sub>CC</sub>	
V <sub>OH</sub>	High-Level Output Voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						V
		I <sub>OH</sub> = –100 μA	1.65 to 5.5	V <sub>CC</sub> – 0.1	–	V <sub>CC</sub> – 0.1	–	
		I <sub>OH</sub> = –4 mA	1.65	1.2	–	1.2	–	
		I <sub>OH</sub> = –8 mA	2.3	1.8	–	1.8	–	
		I <sub>OH</sub> = –12 mA	2.7	2.2	–	2.2	–	
		I <sub>OH</sub> = –16 mA	3.0	2.4	–	2.4	–	
		I <sub>OH</sub> = –24 mA	3.0	2.2	–	2.2	–	
		I <sub>OH</sub> = –32 mA	4.5	3.8	–	3.8	–	
V <sub>OL</sub>	Low-Level Output Voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						V
		I <sub>OL</sub> = 100 μA	1.65 to 5.5	–	0.1	–	0.1	
		I <sub>OL</sub> = 4 mA	1.65	–	0.45	–	0.45	
		I <sub>OL</sub> = 8 mA	2.3	–	0.6	–	0.6	
		I <sub>OL</sub> = 12 mA	2.7	–	0.4	–	0.4	
		I <sub>OL</sub> = 16 mA	3.0	–	0.4	–	0.4	
		I <sub>OL</sub> = 24 mA	3.0	–	0.55	–	0.55	
		I <sub>OL</sub> = 32 mA	4.5	–	0.6	–	0.6	
I <sub>I</sub>	Input Leakage Current	V <sub>I</sub> = 0 to 5.5 V	3.6	–	±5.0	–	±5.0	μA
I <sub>OZ</sub>	3-State Output Leakage Current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> , V <sub>O</sub> = 0 V to 5.5 V	3.6	–	±5.0	–	±5.0	μA
I <sub>OFF</sub>	Power Off Leakage Current	V <sub>I</sub> = 5.5 V or V <sub>O</sub> = 5.5 V	0	–	10	–	10	μA

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## DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C		T <sub>A</sub> = -55°C to +125°C		Unit
				Min	Max	Min	Max	
I <sub>CC</sub>	Quiescent Supply Current	V <sub>I</sub> = 5.5 V or GND	3.6	–	10	–	10	μA
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	V <sub>IH</sub> = V <sub>CC</sub> – 0.6 V	2.3 to 3.6	–	500	–	500	μA

## AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C		T <sub>A</sub> = -55°C to +125°C		Unit
				Min	Max	Min	Max	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay, D to O	See Figures 3 and 4	1.65 to 1.95	–	10.3	–	10.3	ns
			2.3 to 2.7	–	8.4	–	8.4	
			2.7	–	8.0	–	8.0	
			3.0 to 3.6	–	7.0	–	7.0	
			4.5 to 5.5	–	5.0	–	5.0	
t <sub>PZH</sub> , t <sub>PZL</sub>	Output Enable Time, $\overline{OE}$ to O	See Figures 3 and 4	1.65 to 1.95	–	13.0	–	13.0	ns
			2.3 to 2.7	–	10.5	–	10.5	
			2.7	–	9.5	–	9.5	
			3.0 to 3.6	–	8.5	–	8.5	
			4.5 to 5.5	–	7.0	–	7.0	
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Output Disable Time, $\overline{OE}$ to O	See Figures 3 and 4	1.65 to 1.95	–	11.0	–	11.0	ns
			2.3 to 2.7	–	9.0	–	9.0	
			2.7	–	8.5	–	8.5	
			3.0 to 3.6	–	7.5	–	7.5	
			4.5 to 5.5	–	6.0	–	6.0	
t <sub>OSHL</sub> , t <sub>OSLH</sub>	Output to Output Skew (Note 5)		1.65 to 1.95	–	–	–	–	ns
			2.3 to 2.7	–	1.0	–	1.0	
			2.7	–	1.0	–	1.0	
			3.0 to 3.6	–	1.0	–	1.0	
			5.0	–	1.0	–	1.0	

5. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSHL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>); parameter guaranteed by design.

# MC74LCX245

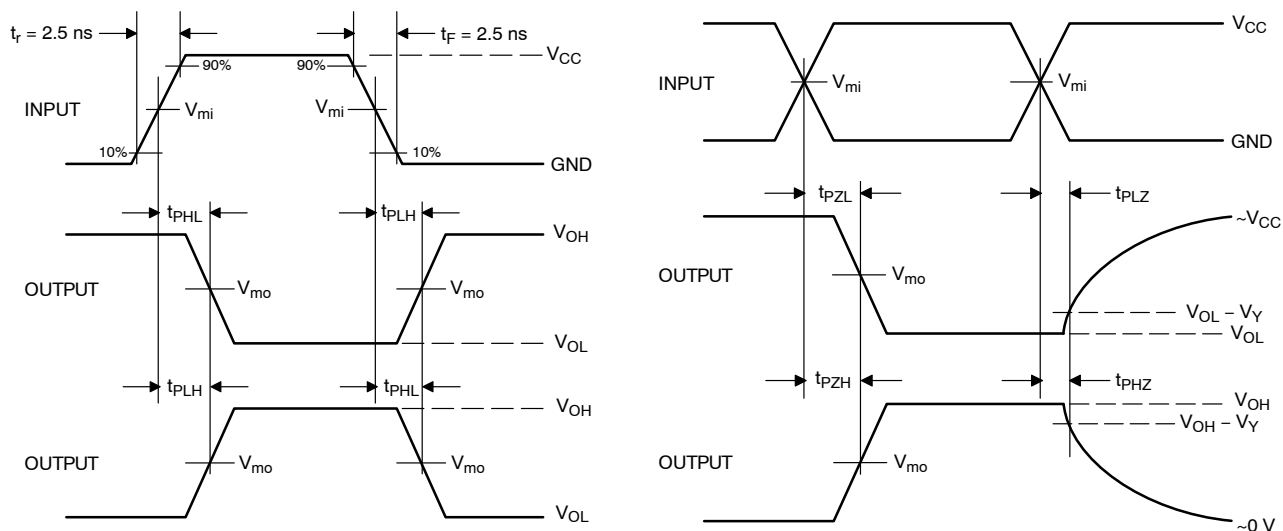
## DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	T <sub>A</sub> = +25°C			Unit
			Min	Typ	Max	
V <sub>OLP</sub>	Dynamic LOW Peak Voltage (Note 6)	V <sub>CC</sub> = 3.3 V, C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3 V, V <sub>IL</sub> = 0 V V <sub>CC</sub> = 2.5 V, C <sub>L</sub> = 30 pF, V <sub>IH</sub> = 2.5 V, V <sub>IL</sub> = 0 V		0.8 0.6		V V
V <sub>OLV</sub>	Dynamic LOW Valley Voltage (Note 6)	V <sub>CC</sub> = 3.3 V, C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3 V, V <sub>IL</sub> = 0 V V <sub>CC</sub> = 2.5 V, C <sub>L</sub> = 30 pF, V <sub>IH</sub> = 2.5 V, V <sub>IL</sub> = 0 V		-0.8 -0.6		V V

6. Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

## CAPACITIVE CHARACTERISTICS

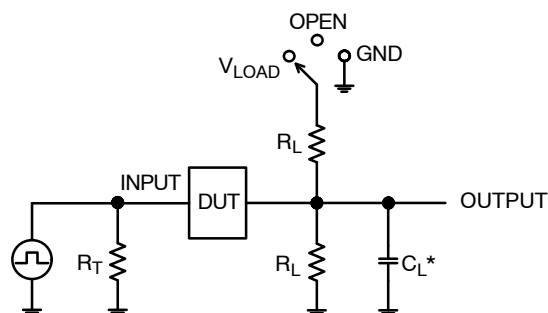
Symbol	Parameter	Condition	Typical	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = 3.3 V, V <sub>I</sub> = 0 V or V <sub>CC</sub>	7	pF
C <sub>I/O</sub>	Input/Output Capacitance	V <sub>CC</sub> = 3.3 V, V <sub>I</sub> = 0 V or V <sub>CC</sub>	8	pF
C <sub>PD</sub>	Power Dissipation Capacitance	10 MHz, V <sub>CC</sub> = 3.3 V, V <sub>I</sub> = 0 V or V <sub>CC</sub>	25	pF



V <sub>CC</sub> , V	R <sub>L</sub> , Ω	C <sub>L</sub> , pF	V <sub>LOAD</sub>	V <sub>mi</sub> , V	V <sub>mo</sub> , V	V <sub>Y</sub> , V
1.65 to 1.95	500	30	2 × V <sub>CC</sub>	V <sub>CC</sub> /2	V <sub>CC</sub> /2	0.15
2.3 to 2.7	500	30	2 × V <sub>CC</sub>	V <sub>CC</sub> /2	V <sub>CC</sub> /2	0.15
2.7	500	50	6 V	1.5	V <sub>CC</sub> /2	0.3
3.0 to 3.6	500	50	6 V	1.5	V <sub>CC</sub> /2	0.3
4.5 to 4.5	500	50	2 × V <sub>CC</sub>	V <sub>CC</sub> /2	V <sub>CC</sub> /2	0.3

Figure 3. Switching Waveforms

## MC74LCX245



$C_L$  includes probe and jig capacitance  
 $R_T$  is  $Z_{OUT}$  of pulse generator (typically 50  $\Omega$ )  
 $f = 1 \text{ MHz}$

Test	Switch Position
$t_{PLH} / t_{PHL}$	Open
$t_{PLZ} / t_{PZL}$	$V_{LOAD}$
$t_{PHZ} / t_{PZH}$	GND

Figure 4. Test Circuit

### ORDERING INFORMATION

Device	Marking	Package	Shipping <sup>†</sup>
MC74LCX245DWG	LCX245	SOIC-20 WB	38 Units / Rail
MC74LCX245DWR2G	LCX245	SOIC-20 WB	1000 / Tape & Reel
MC74LCX245DTG	LCX 245	TSSOP-20	75 Units / Rail
MC74LCX245DTR2G	LCX 245	TSSOP-20	2500 / Tape & Reel
MC74LCX245DTR2G-Q*	LCX 245	TSSOP-20	2500 / Tape & Reel
MC74LCX245MNTWG	LCX 245	QFN20, 2.5x4.5	3000 / Tape & Reel (4mm pitch carrier tape)

### DISCONTINUED (Note 7)

NLV74LCX245DTR2G*	LCX 245	TSSOP-20 (Pb-Free)	2500 Tape & Reel
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<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

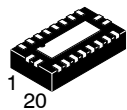
\*-Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

7. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on [www.onsemi.com](http://www.onsemi.com).

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

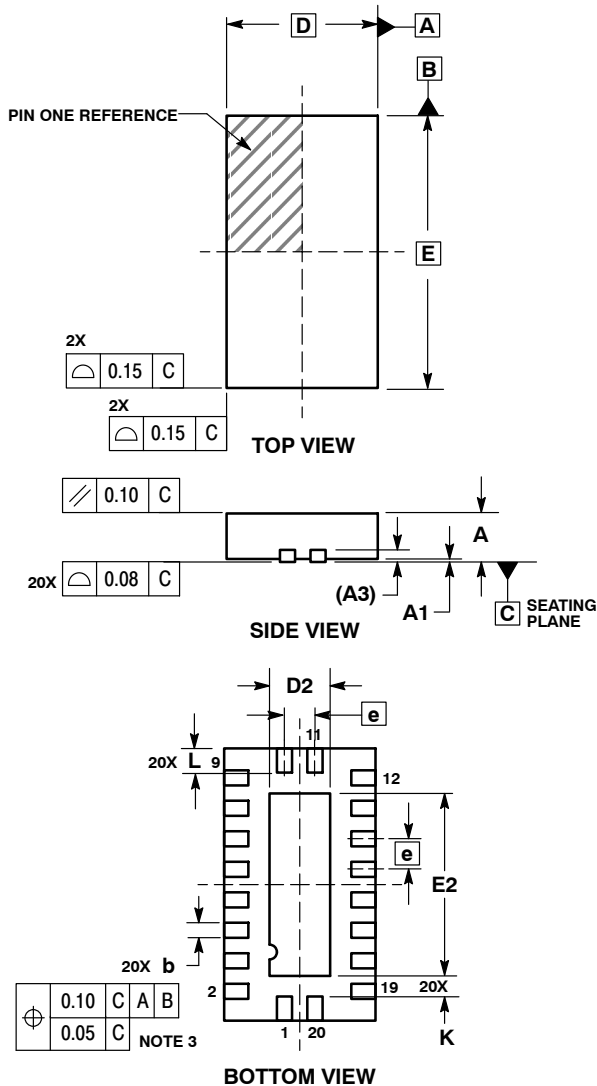
ON Semiconductor®



SCALE 2:1

**QFN20, 2.5x4.5 MM**  
CASE 485AA-01  
ISSUE B

DATE 30 APR 2010

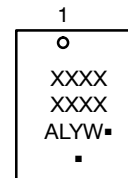


### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.50 BSC	
D2	0.85	1.15
E	4.50 BSC	
E2	2.85	3.15
e	0.50 BSC	
K	0.20	---
L	0.35	0.45

### GENERIC MARKING DIAGRAM\*



XXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

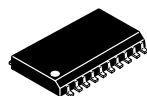
(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

<b>DOCUMENT NUMBER:</b>	<b>98AON12653D</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>QFN20. 2.5X4.5 MM</b>	<b>PAGE 1 OF 1</b>

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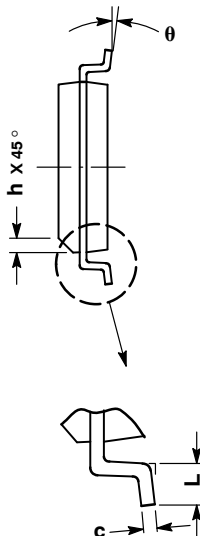
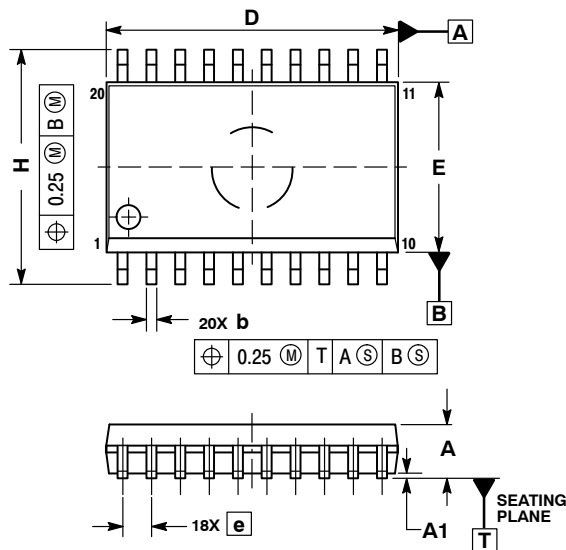




SCALE 1:1

SOIC-20 WB  
CASE 751D-05  
ISSUE H

DATE 22 APR 2015

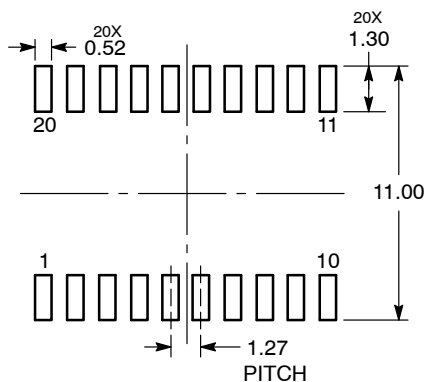


NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

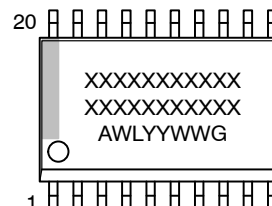
RECOMMENDED  
SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC  
MARKING DIAGRAM\*

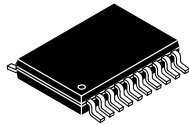


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WW = Work Week  
G = Pb-Free Package

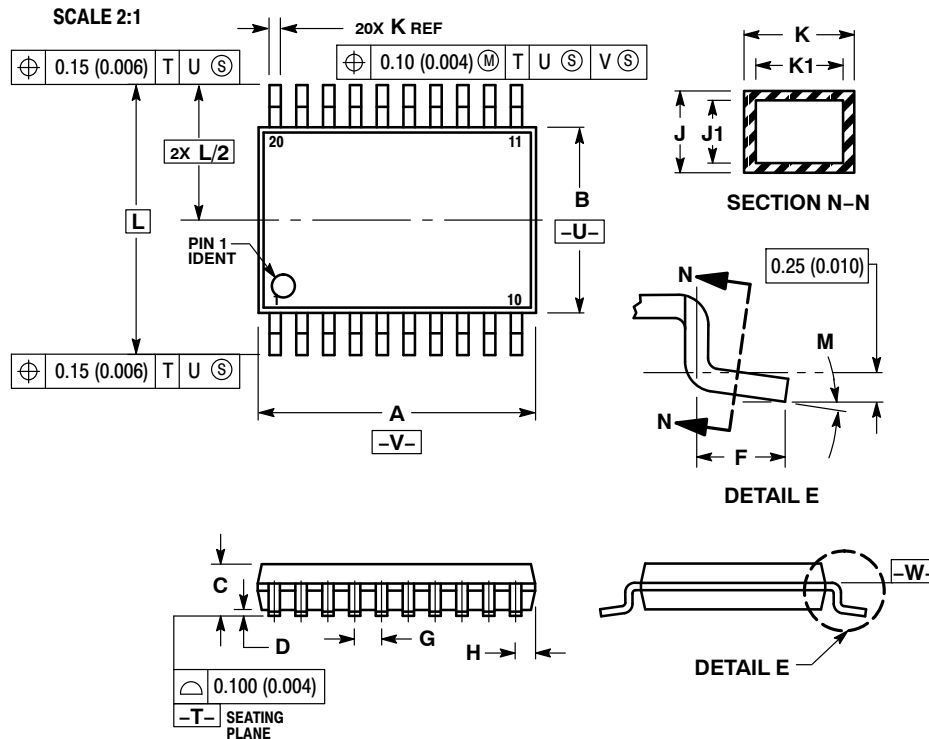
\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	SOIC-20 WB	PAGE 1 OF 1

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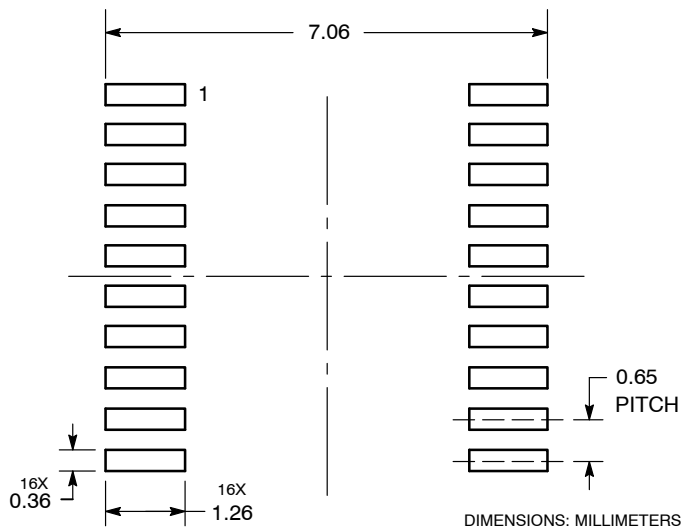

**TSSOP-20 WB**  
**CASE 948E**  
**ISSUE D**

DATE 17 FEB 2016

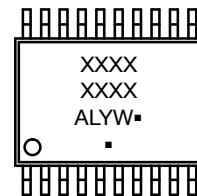

**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

**RECOMMENDED  
SOLDERING FOOTPRINT\***


\*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC  
MARKING DIAGRAM\***


A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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