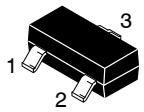
NPN High-Voltage Transistor

FJV42



SOT−23 (TO−236)
CASE 318

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{CEO}	Collector−Emitter Voltage	350	V
V_{CBO}	Collector−Base Voltage	350	V
V_{EBO}	Emitter−Base Voltage	6	V
I_C	Collector Current	500	mA
T_{STG}	Storage Temperature Range	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

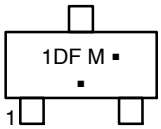
THERMAL CHARACTERISTICS (Note 1)

(T_A = 25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
P_D	Power Dissipation	350	mW
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient	357	°C/W

1. PCB size: FR−4, 76 mm x 114 mm x 1.57 mm (3.0 inch x 4.5 inch x 0.062 inch) with minimum land pattern size.

MARKING DIAGRAM



1DF = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
FJV42MTF	SOT−23 (Pb−Free)	3,000 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{(BR)CEO}$	Collector−Emitter Breakdown Voltage (Note 2)	I_C = 5.0 mA, I_B = 0	350		V
$V_{(BR)CBO}$	Collector−Base Breakdown Voltage	I_C = 100 μA, I_E = 0	350		V
$V_{(BR)EBO}$	Emitter−Base Breakdown Voltage	I_E = 100 μA, I_C = 0	6		V
I_{CBO}	Collector Cut−Off Current	V_{CB} = 200 V, I_E = 0		0.1	μA
I_{EBO}	Emitter Cut−Off Current	V_{EB} = 5.0 V, I_C = 0		0.1	μA
h_{FE}	DC Current Gain (Note 2)	I_C = 1.0 mA, V_{CE} = 10 V	25		
		I_C = 10 mA, V_{CE} = 10 V	40		
		I_C = 30 mA, V_{CE} = 10 V	40		
V_{CE}(sat)	Collector−Emitter Saturation Voltage (Note 2)	I_C = 20 mA, I_B = 2.0 mA		0.5	V
V_{BE}(sat)	Base−Emitter Saturation Voltage (Note 2)	I_C = 20 mA, I_B = 2.0 mA		0.9	V
f_T	Current Gain − Bandwidth Product	I_C = 10 mA, V_{CE} = 20 V, f = 100 MHz	50		MHz
C_{cb}	Output Capacitance	V_{CB} = 20 V, I_E = 0, f = 1.0 MHz		3	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse test: Pulse width ≤ 300 μs, duty cycle ≤ 2%

TYPICAL PERFORMANCE CHARACTERISTICS

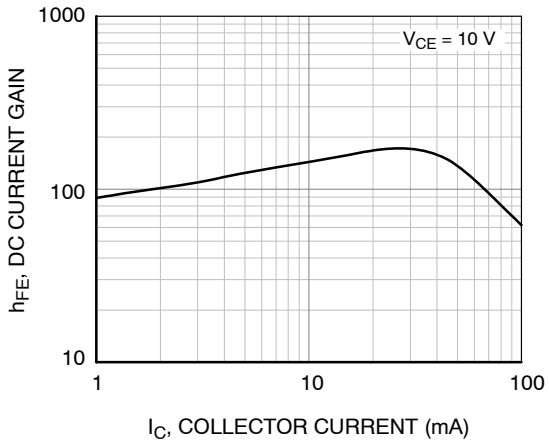


Figure 1. DC Current Gain

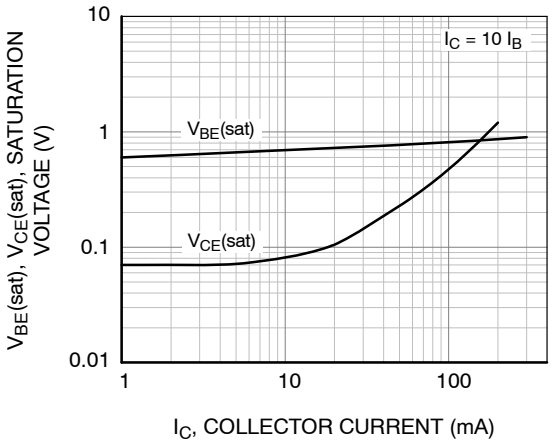


Figure 2. Collector−Emitter Saturation Voltage and Base−Emitter Saturation Voltage

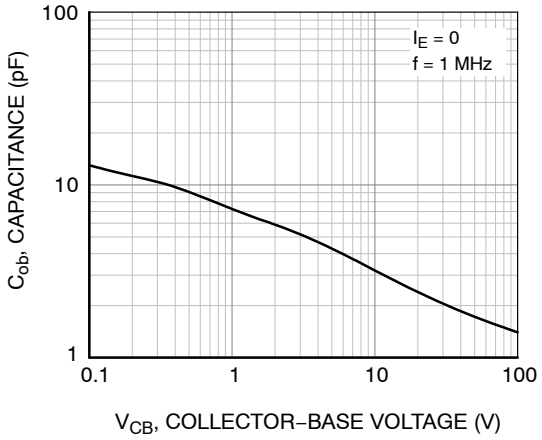


Figure 3. Collector−Base Capacitance

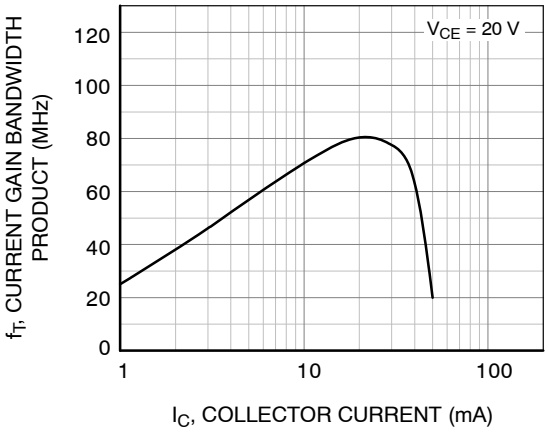
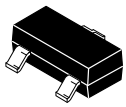


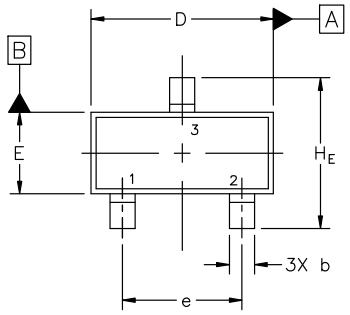
Figure 4. Current Gain Bandwidth Product



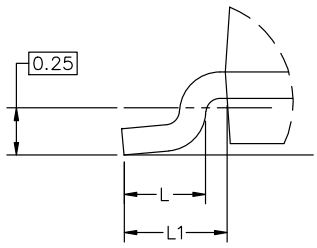
SCALE 4:1

SOT−23 (TO−236) 2.90x1.30x1.00 1.90P
CASE 318
ISSUE AU

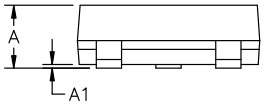
DATE 14 AUG 2024



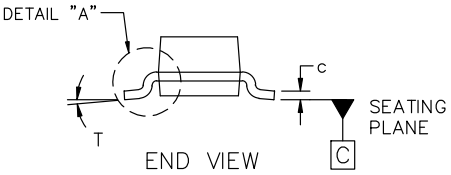
TOP VIEW



DETAIL "A"
Scale 3:1



SIDE VIEW

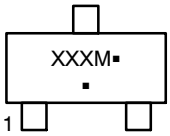


END VIEW

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.89	1.00	1.11
A1	0.01	0.06	0.10
b	0.37	0.44	0.50
c	0.08	0.14	0.20
D	2.80	2.90	3.04
E	1.20	1.30	1.40
e	1.78	1.90	2.04
L	0.30	0.43	0.55
L1	0.35	0.54	0.69
H_E	2.10	2.40	2.64
T	0°	−−−	10°

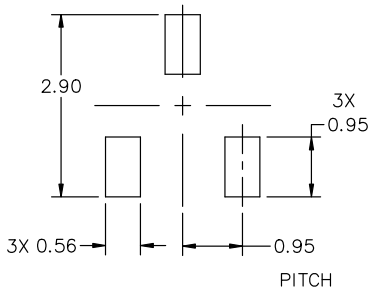
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

GENERIC
MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb−Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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CASE 318
ISSUE AU

DATE 14 AUG 2024

STYLE 1 THRU 5:
CANCELLED

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 7:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

STYLE 12:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 13:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 15:
PIN 1. GATE
2. CATHODE
3. ANODE

STYLE 16:
PIN 1. ANODE
2. CATHODE
3. CATHODE

STYLE 17:
PIN 1. NO CONNECTION
2. ANODE
3. CATHODE

STYLE 18:
PIN 1. NO CONNECTION
2. CATHODE
3. ANODE

STYLE 19:
PIN 1. CATHODE
2. ANODE
3. CATHODE−ANODE

STYLE 20:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 22:
PIN 1. RETURN
2. OUTPUT
3. INPUT

STYLE 23:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 24:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 25:
PIN 1. ANODE
2. CATHODE
3. GATE

STYLE 26:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION

STYLE 27:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

STYLE 28:
PIN 1. ANODE
2. ANODE
3. ANODE

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