Low Voltage Buffer/Line Driver with 5V Tolerant Inputs and Outputs

74LCX244

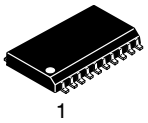
The LCX244 contains eight non−inverting buffers with 3−STATE outputs. The device may be employed as a memory address driver, clock driver and bus−oriented transmitter/receiver. The LCX244 is designed for low voltage (2.5 V or 3.3 V) V_{CC} applications with capability of interfacing to a 5 V signal environment.

The LCX244 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

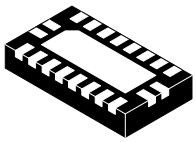
Features

- 5 V Tolerant Inputs and Outputs
- 1.65 V to 5.5 V V_{CC} Specifications Provided
- 6.5 ns t_{PD} max. (V_{CC} = 3.3 V), 10 μA I_{CC} max.
- Power Down High Impedance Inputs and Outputs
- Supports Live Insertion/Withdrawal (Note 1)
- ±24 mA Output Drive (V_{CC} = 3.0 V)
- Implements Proprietary Noise/EMI Reduction Circuitry
- Latch−up Performance Exceeds 500 mA
- ESD Performance:
  - Human Body Model > 2000 V
- Leadless DQFN Package

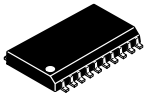
1. To ensure the high−impedance state during power up or down, $\overline{OE}$ should be tied to V_{CC} through a pull−up resistor: the minimum value or the resistor is determined by the current−sourcing capability of the driver.



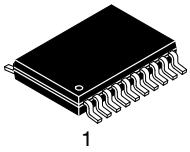
SOIC−20W
CASE 751D



WQFN−20
CASE 510CD



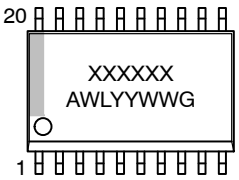
SOIC−20W
CASE 751BJ



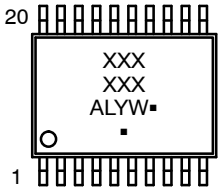
TSSOP−20
CASE 948AQ

MARKING DIAGRAMS

SOIC−20W



TSSOP−20



XXXXXX = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ▪ = Pb−Free Package

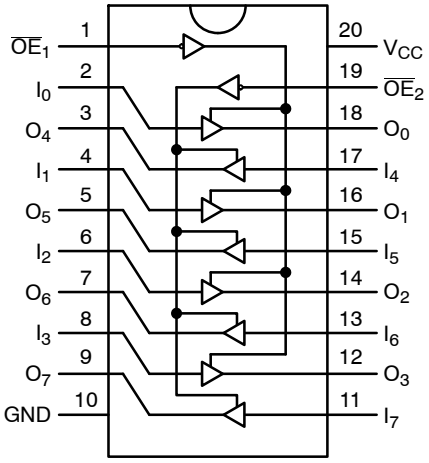
(Note: Microdot may be in either location)

ORDERING INFORMATION

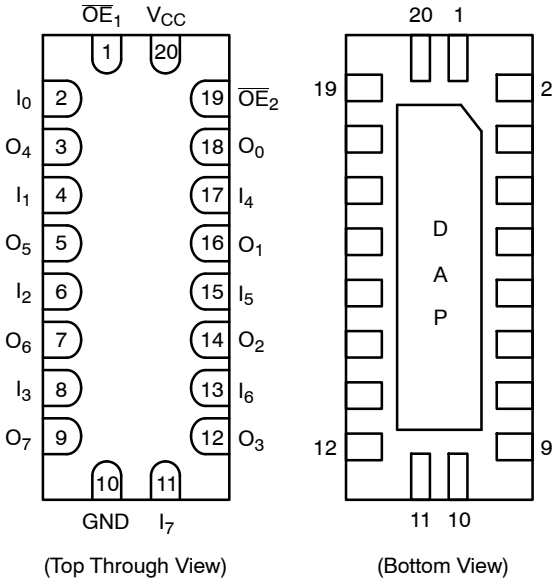
See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

Connection Diagram

Pin Assignments for SOIC, SOP, SSOP, and TSSOP

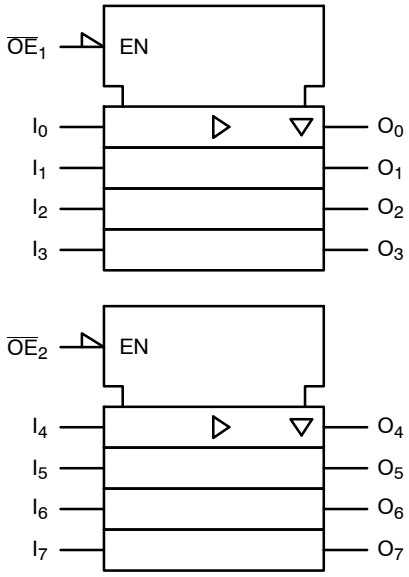


Pad Assignments for DQFN



(Top Through View) (Bottom View)

Logic Diagram



Truth Tables

Inputs		Outputs
$\overline{OE}_1$	I_n	(Pins 12, 14, 16, 18)
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_2$	I_n	(Pins 3, 5, 7, 9)
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	3−STATE Output Enable Inputs
I_0−I_7	Inputs
$\overline{O}_0$−$\overline{O}_7$	Outputs
DAP	No Connect

2. DAP (Die Attach Pad)

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +6.5	V
V_I	DC Input Voltage (Note 3)		−0.5 to +6.5	V
V_O	DC Output Voltage (Note 3)	Active−Mode (High or Low State) Tri−State Mode Power−Down Mode (V_{CC} = 0 V)	−0.5 to V_{CC}+0.5 −0.5 to +6.5 −0.5 to +6.5	V
I_{IK}	DC Input Diode Current	V_{IN} < GND	−50	mA
I_{OK}	DC Output Diode Current	V_{OUT} < GND	−50	mA
I_O	DC Output Source/Sink Current		±50	mA
I_{CC} or I_{GND}	DC Supply Current per Supply Pin or Ground Pin		±100	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 secs		260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 4)	SOIC−20W WQFN20 TSSOP−20	96 99 150	°C/W
P_D	Power Dissipation in Still Air	SOIC−20W WQFN20 TSSOP−20	1302 1256 833	mW
MSL	Moisture Sensitivity	SOIC−20W All Other Packages	Level 3 Level 1	−
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	−
V_{ESD}	ESD Withstand Voltage (Note 5)	Human Body Model Charged Device Model	2000 N/A	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3. I_O absolute maximum rating must be observed.
4. Measured with minimum pad spacing on an FR4 board, using 76mm−by−114mm, 2−ounce copper trace no air flow per JESD51−7.
5. HBM tested to EIA / JESD22−A114−A. CDM tested to JESD22−C101−A.

RECOMMENDED OPERATING CONDITIONS (Note 6)

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage	Operating Data Retention Only	1.65 1.5	5.5 5.5	V
V_I	Digital Input Voltage		0	5.5	V
V_O	Output Voltage	Active Mode (High or Low State) Tri−State Mode Power Down Mode (V_{CC} = 0 V)	0 0 0	V_{CC} 5.5 5.5	V
T_A	Operating Free−Air Temperature		−40	+125	°C
t_r, t_f	Input Rise or Fall Rate	V_{CC} = 1.65 V to 1.95 V V_{CC} = 2.3 V to 2.7 V V_{IN} from 0.8 V to 2.0 V, V_{CC} = 3.0 V V_{CC} = 4.5 V to 5.5 V	0 0 0 0	20 20 10 5	nS/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

6. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		T_A = −40°C to +125°C		Unit
				Min	Max	Min	Max	
V_{IH}	High−Level Input Voltage		1.65 to 1.95	0.65 x V_{CC}		0.65 x V_{CC}		V
			2.3 to 2.7	1.7		1.7		
			2.7 to 3.6	2.0		2.0		
			4.5 to 5.5	0.7 x V_{CC}		0.7 x V_{CC}		
V_{IL}	Low−Level Input Voltage		1.65 to 1.95		0.35 x V_{CC}		0.35 x V_{CC}	V
			2.3 to 2.7		0.7		0.7	
			2.7 to 3.6		0.8		0.8	
			4.5 to 5.5		0.3 x V_{CC}		0.3 x V_{CC}	
V_{OH}	High−Level Output Voltage	V_I = V_{IH} or V_{IL}						V
		I_{OH} = −100 μA	1.65 to 5.5	V_{CC} − 0.1	−	V_{CC} − 0.1	−	
		I_{OH} = −4 mA	1.65	1.2	−	1.2	−	
		I_{OH} = −8 mA	2.3	1.8	−	1.8	−	
		I_{OH} = −12 mA	2.7	2.2	−	2.2	−	
		I_{OH} = −16 mA	3.0	2.4	−	2.4	−	
		I_{OH} = −24 mA	3.0	2.2	−	2.2	−	
		I_{OH} = −32 mA	4.5	3.8		3.8		
V_{OL}	Low−Level Output Voltage	V_I = V_{IH} or V_{IL}						V
		I_{OL} = 100 μA	1.65 to 5.5	−	0.1	−	0.1	
		I_{OL} = 4 mA	1.65	−	0.45	−	0.45	
		I_{OL} = 8 mA	2.3	−	0.6	−	0.6	
		I_{OL} = 12 mA	2.7	−	0.4	−	0.4	
		I_{OL} = 16 mA	3.0	−	0.4	−	0.4	
		I_{OL} = 24 mA	3.0	−	0.55	−	0.55	
		I_{OL} = 32 mA	4.5		0.6		0.6	
I_I	Input Leakage Current	V_I = 0 to 5.5 V	3.6	−	±5.0	−	±5.0	μA
I_{OZ}	3−State Output Leakage Current	V_I = V_{IH} or V_{IL}, V_O = 0 V to 5.5 V	3.6	−	±5.0	−	±5.0	μA
I_{OFF}	Power Off Leakage Current	V_I = 5.5 V or V_O = 5.5 V	0	−	10	−	10	μA
I_{CC}	Quiescent Supply Current	V_I = 5.5 V or GND	2.3 to 3.6	−	10	−	10	μA
		3.6 V ≤ V_I, V_O ≤ 5.5 V (Note 7)			±10.0		±10.0	
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} − 0.6 V	2.3 to 3.6	−	500	−	500	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Outputs disabled or 3−STATE only.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	V_{CC} (V)	T_A = −40°C to +85°C		T_A = −40°C to +125°C		Unit
				Min	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay, D to O	See Figures 1 and 2	1.65 to 1.95	–	10.3	–	10.3	ns
			2.3 to 2.7	–	7.8	–	7.8	
			2.7	–	7.5	–	7.5	
			3.0 to 3.6	–	6.5	–	6.5	
			4.5 to 5.5	–	5.9	–	5.9	
t_{PZH}, t_{PZL}	Output Enable Time, $\overline{OE}$ to O	See Figures 1 and 2	1.65 to 1.95	–	13.0	–	13.0	ns
			2.3 to 2.7	–	10.0	–	10.0	
			2.7	–	9.0	–	9.0	
			3.0 to 3.6	–	8.0	–	8.0	
			4.5 to 5.5	–	7.3	–	7.3	
t_{PHZ}, t_{PLZ}	Output Disable Time, $\overline{OE}$ to O	See Figures 1 and 2	1.65 to 1.95	–	11.0	–	11.0	ns
			2.3 to 2.7	–	8.4	–	8.4	
			2.7	–	8.0	–	8.0	
			3.0 to 3.6	–	7.0	–	7.0	
			4.5 to 5.5	–	6.0	–	6.0	
t_{OSHL}, t_{OSLH}	Output to Output Skew (Note 8)		1.65 to 1.95	–	–	–	–	ns
			2.3 to 2.7	–	–	–	–	
			2.7	–	–	–	–	
			3.0 to 3.6	–	1.0	–	1.0	

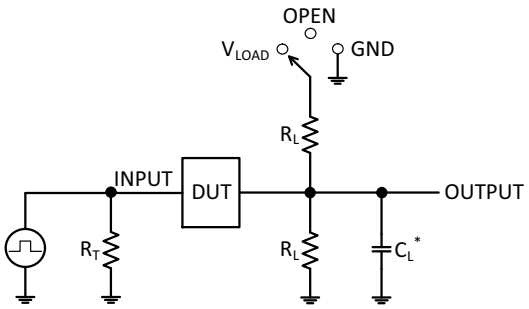
8. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the dynamic operating current consumption without load. Average operating current can be obtained by the equation $I_{CC(OPR)} = C_{PD} \times V_{CC} \times f_{in} + I_{CC}$. C_{PD} is used to determine the no−load dynamic power consumption: $P_D = C_{PD} \times V_{CC}^2 \times f_{in} + I_{CC} \times V_{CC}$.

DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = 25°C	Unit
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	3.3	C_L = 50 pF, V_{IH} = 3.3 V, V_{IL} = 0 V	0.8	V
		2.5	C_L = 30 pF, V_{IH} = 2.5 V, V_{IL} = 0 V	0.6	
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	3.3	C_L = 50 pF, V_{IH} = 3.3 V, V_{IL} = 0 V	−0.8	V
		2.5	C_L = 30 pF, V_{IH} = 2.5 V, V_{IL} = 0 V	−0.6	

CAPACITANCE

Symbol	Parameter	Conditions	Typical	Unit
C_{IN}	Input Capacitance	V_{CC} = Open, V_I = 0 V or V_{CC}	7.0	pF
C_{OUT}	Output Capacitance	V_{CC} = 3.3 V, V_I = 0 V or V_{CC}	8.0	pF
C_{PD}	Power Dissipation Capacitance	V_{CC} = 3.3 V, V_I = 0 V or V_{CC}, f = 10 MHz	25.0	pF



Test	Switch Position
t_{PLH} / t_{PHL}	Open
t_{PLZ} / t_{PZL}	V_{LOAD}
t_{PHZ} / t_{PZH}	GND

*C_L includes probe and jig capacitance
R_T is Z_{OUT} of pulse generator (typically 50 Ω)
f = 1 MHz

Figure 1. Test Circuit

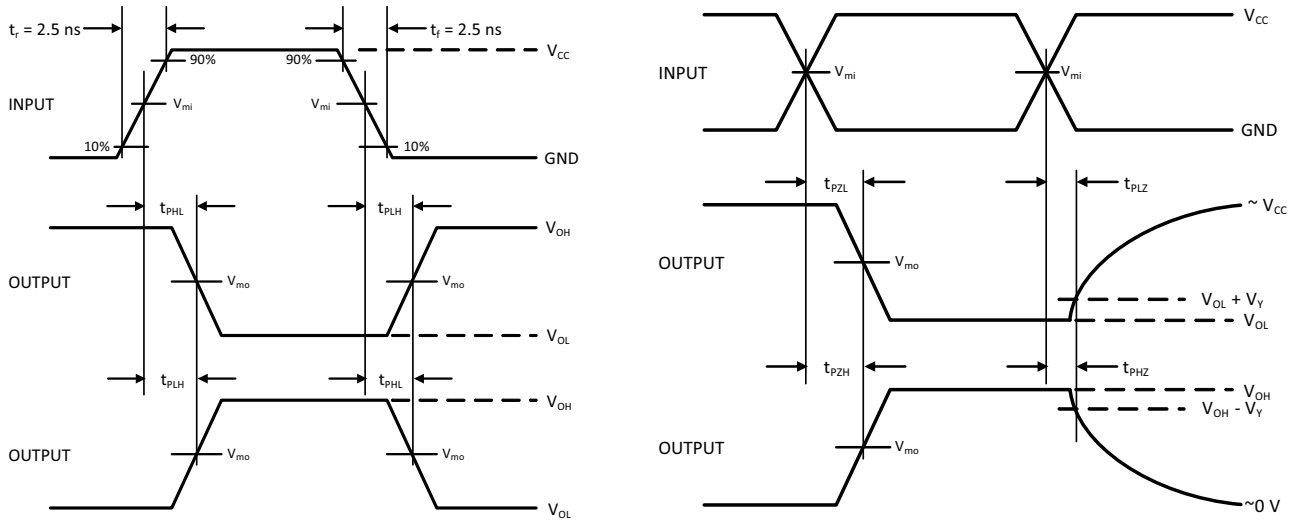
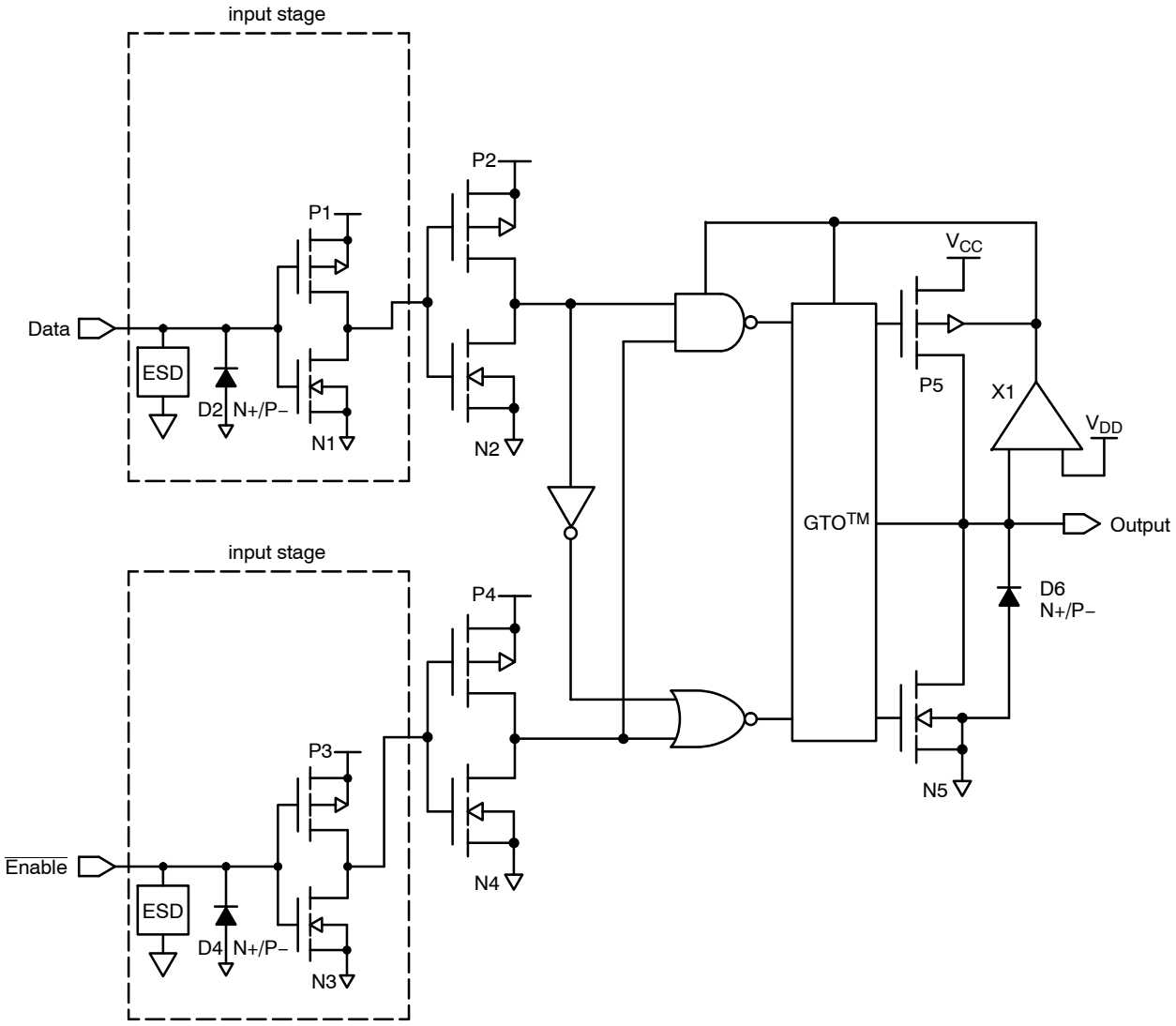


Figure 2. Switching Waveforms

V_{CC}, V	R_L, Ω	C_L, pF	V_{LOAD}	V_{mi}, V	V_{mo}, V	V_Y, V
1.65 to 1.95	500	30	2 x V_{CC}	V_{CC}/2	V_{CC}/2	0.15
2.3 to 2.7	500	30	2 x V_{CC}	V_{CC}/2	V_{CC}/2	0.15
2.7	500	50	6 V	1.5	V_{CC}/2	0.3
3.0 to 3.6	500	50	6 V	1.5	V_{CC}/2	0.3
4.5 to 4.5	500	50	2 x V_{CC}	V_{CC}/2	V_{CC}/2	0.3

Schematic Diagram (Generic for LCX Family)



ORDERING INFORMATION

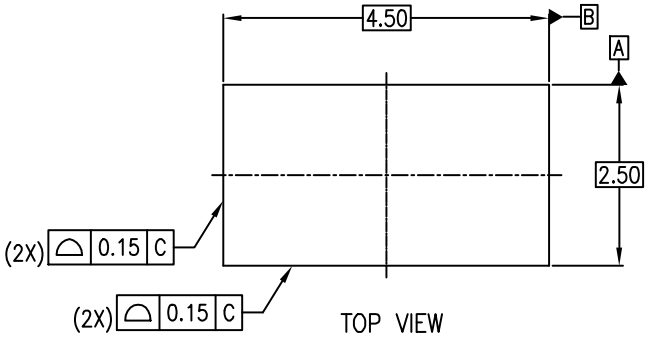
Device	Marking	Package	Shipping†
74LCX244WM	LCX244	SOIC−20 WB	38 Units / Tube
74LCX244WMX	LCX244	SOIC−20 WB	1000 / Tape & Reel
74LCX244MTC	LCX 244	TSSOP−20	75 Units / Tube
74LCX244MTCX	LCX 244	TSSOP−20	2500 / Tape & Reel
74LCX244BQX	LCX244	WQFN20, 2.5x4.5	3000 / Tape & Reel

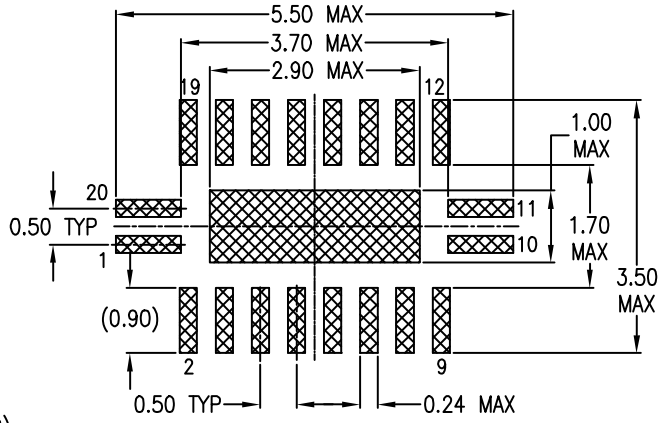
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*−Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

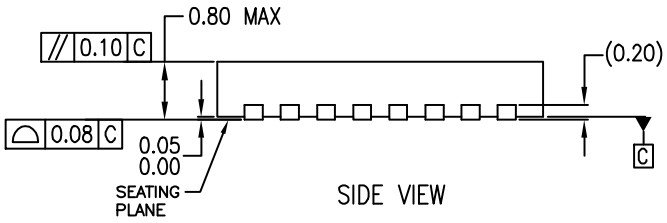
PACKAGE DIMENSIONS

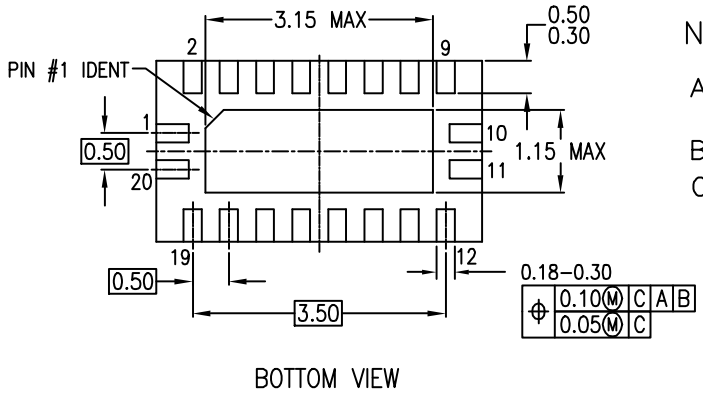
WQFN20 4.5x2.5, 0.5P
CASE 510CD
ISSUE O





RECOMMENDED LAND PATTERN



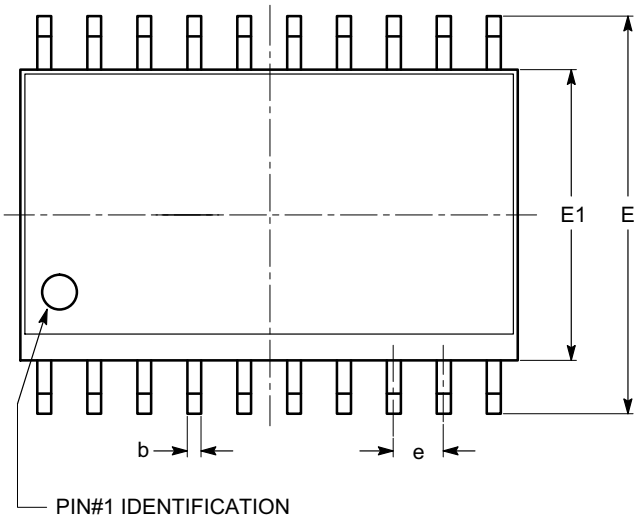


NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO−241, VARIATION AC
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

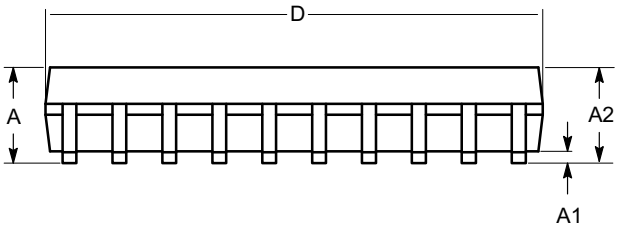
PACKAGE DIMENSIONS

SOIC−20, 300 mils
CASE 751BJ
ISSUE O

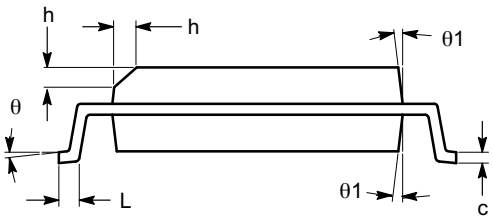


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	2.36	2.49	2.64
A1	0.10		0.30
A2	2.05		2.55
b	0.31	0.41	0.51
c	0.20	0.27	0.33
D	12.60	12.80	13.00
E	10.01	10.30	10.64
E1	7.40	7.50	7.60
e	1.27 BSC		
h	0.25		0.75
L	0.40	0.81	1.27
θ	0°		8°
θ1	5°		15°



SIDE VIEW

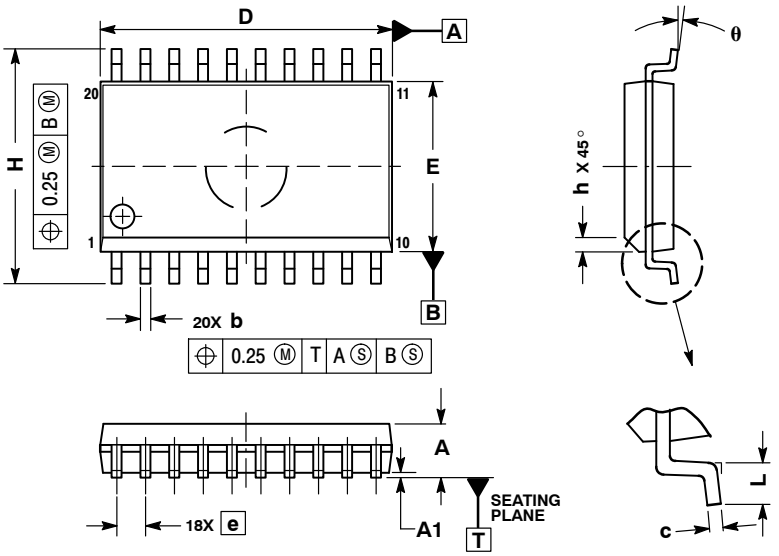


END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-013.

PACKAGE DIMENSIONS

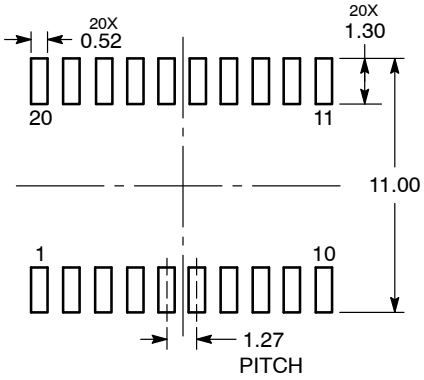
SOIC−20 WB
CASE 751D−05
ISSUE H



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

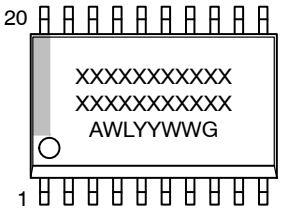
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

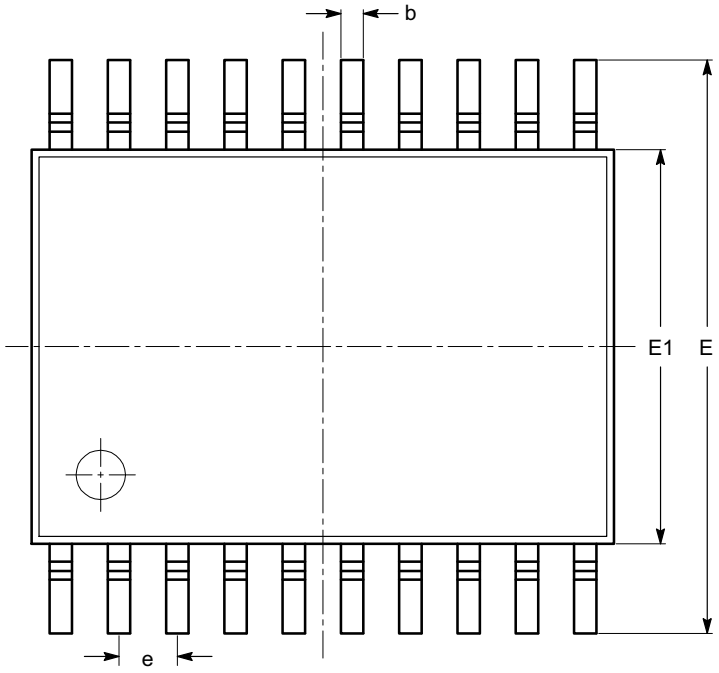


XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

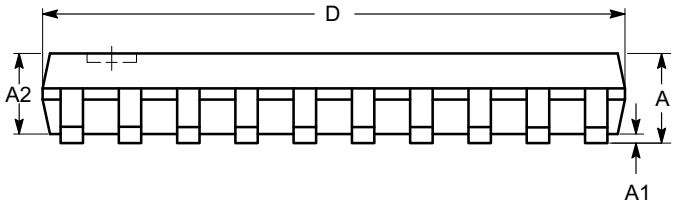
PACKAGE DIMENSIONS

TSSOP20, 4.4x6.5
CASE 948AQ
ISSUE A

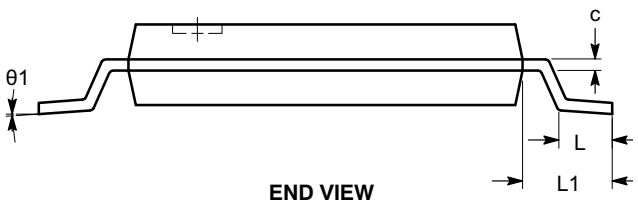


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80		1.05
b	0.19		0.30
c	0.09		0.20
D	6.40	6.50	6.60
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e		0.65 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0°		8°



SIDE VIEW



END VIEW

Notes:

(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales

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