

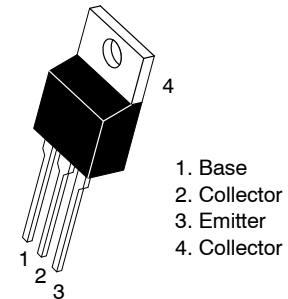
Complementary Silicon Transistors, Plastic, Medium-Power

TIP100, TIP101, TIP102 (NPN); TIP105, TIP106, TIP107 (PNP)

Designed for general-purpose amplifier and low-speed switching applications.

Features

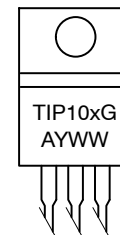
- High DC Current Gain –
 $h_{FE} = 2500 \text{ (Typ) @ } I_C$
 $= 4.0 \text{ Adc}$
- Collector–Emitter Sustaining Voltage – @ 30 mAdc
 $V_{CEO(sus)} = 60 \text{ Vdc (Min) – TIP100, TIP105}$
 $= 80 \text{ Vdc (Min) – TIP101, TIP106}$
 $= 100 \text{ Vdc (Min) – TIP102, TIP107}$
- Low Collector–Emitter Saturation Voltage –
 $V_{CE(sat)} = 2.0 \text{ Vdc (Max) @ } I_C$
 $= 3.0 \text{ Adc}$
 $= 2.5 \text{ Vdc (Max) @ } I_C = 8.0 \text{ Adc}$
- Monolithic Construction with Built-in Base–Emitter Shunt Resistors
- These Devices are Pb–Free and are RoHS Compliant



TO-220AB
CASE 221A
STYLE 1

DARLINGTON 8 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 60–80–100 VOLTS, 80 WATTS

MARKING DIAGRAM



TIP10x = Device Code
x = 0, 1, 2, 5, 6, or 7
A = Assembly Location
Y = Year
WW = Work Week
G = Pb–Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

TIP100, TIP101, TIP102 (NPN); TIP105, TIP106, TIP107 (PNP)

MAXIMUM RATINGS

Symbol	Rating	TIP100, TIP105	TIP101, TIP106	TIP102, TIP107	Unit
V_{CEO}	Collector – Emitter Voltage	60	80	100	Vdc
V_{CB}	Collector – Base Voltage	60	80	100	Vdc
V_{EB}	Emitter – Base Voltage	5.0			Vdc
I_C	Collector Current – Continuous – Peak	8.0 15			Adc
I_B	Base Current	1.0			Adc
P_D	Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	80 0.64			W W/ $^\circ\text{C}$
E	Unclamped Inductive Load Energy (Note 1)	30			mJ
P_D	Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	2.0 0.016			W W/ $^\circ\text{C}$
T_J, T_{stg}	Operating and Storage Junction Temperature Range	–65 to +150			$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Characteristic	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.56	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	$^\circ\text{C}/\text{W}$

1. $I_C = 1.1\text{ A}$, $L = 50\text{ mH}$, P.R.F. = 10 Hz, $V_{CC} = 20\text{ V}$, $R_{BE} = 100\ \Omega$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Characteristic	Min	Max	Unit
--------	----------------	-----	-----	------

OFF CHARACTERISTICS

$V_{CEO(sus)}$	Collector–Emitter Sustaining Voltage (Note 1) ($I_C = 30\text{ mAdc}$, $I_B = 0$)	TIP100, TIP105 TIP101, TIP106 TIP102, TIP107	60 80 100	– – –	Vdc
I_{CEO}	Collector Cutoff Current ($V_{CE} = 30\text{ Vdc}$, $I_B = 0$) ($V_{CE} = 40\text{ Vdc}$, $I_B = 0$) ($V_{CE} = 50\text{ Vdc}$, $I_B = 0$)	TIP100, TIP105 TIP101, TIP106 TIP102, TIP107	– – –	50 50 50	μAdc
I_{CBO}	Collector Cutoff Current ($V_{CB} = 60\text{ Vdc}$, $I_E = 0$) ($V_{CB} = 80\text{ Vdc}$, $I_E = 0$) ($V_{CB} = 100\text{ Vdc}$, $I_E = 0$)	TIP100, TIP105 TIP101, TIP106 TIP102, TIP107	– – –	50 50 50	μAdc
I_{EBO}	Emitter Cutoff Current ($V_{BE} = 5.0\text{ Vdc}$, $I_C = 0$)		–	8.0	mAdc

ON CHARACTERISTICS (Note 1)

h_{FE}	DC Current Gain ($I_C = 3.0\text{ Adc}$, $V_{CE} = 4.0\text{ Vdc}$) ($I_C = 8.0\text{ Adc}$, $V_{CE} = 4.0\text{ Vdc}$)	1000 200	20,000 –	–
$V_{CE(sat)}$	Collector–Emitter Saturation Voltage ($I_C = 3.0\text{ Adc}$, $I_B = 6.0\text{ mAdc}$) ($I_C = 8.0\text{ Adc}$, $I_B = 80\text{ mAdc}$)	– –	2.0 2.5	Vdc
$V_{BE(on)}$	Base–Emitter On Voltage ($I_C = 8.0\text{ Adc}$, $V_{CE} = 4.0\text{ Vdc}$)	–	2.8	Vdc

DYNAMIC CHARACTERISTICS

h_{fe}	Small-Signal Current Gain ($I_C = 3.0\text{ Adc}$, $V_{CE} = 4.0\text{ Vdc}$, $f = 1.0\text{ MHz}$)	4.0	–	–
C_{ob}	Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f = 0.1\text{ MHz}$)	TIP105, TIP106, TIP107 TIP100, TIP101, TIP102	– –	300 200
				pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

TIP100, TIP101, TIP102 (NPN); TIP105, TIP106, TIP107 (PNP)

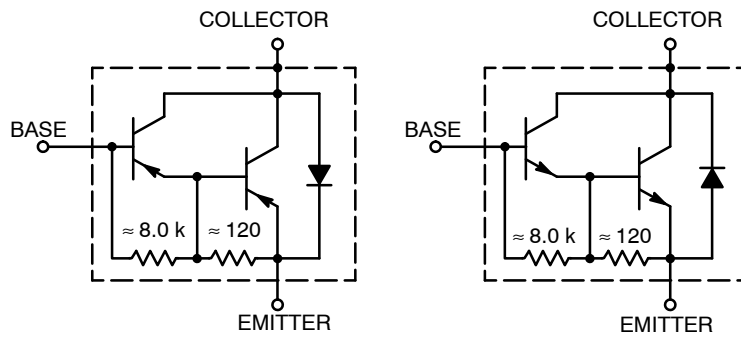


Figure 1. Darlington Circuit Schematic

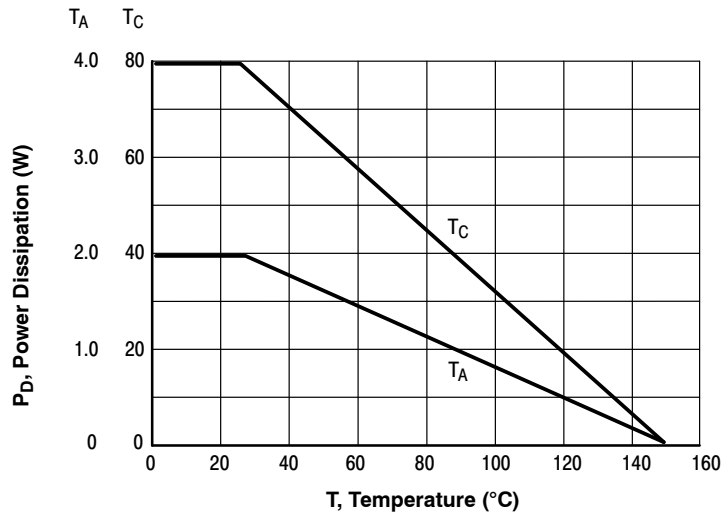


Figure 2. Power Derating

TIP100, TIP101, TIP102 (NPN); TIP105, TIP106, TIP107 (PNP)

R_B & R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS D_1 , MUST BE FAST RECOVERY TYPE, eg: 1N5825 USED ABOVE I_B 9 100 mA
MSD6100 USED BELOW I_B 9 100 mA

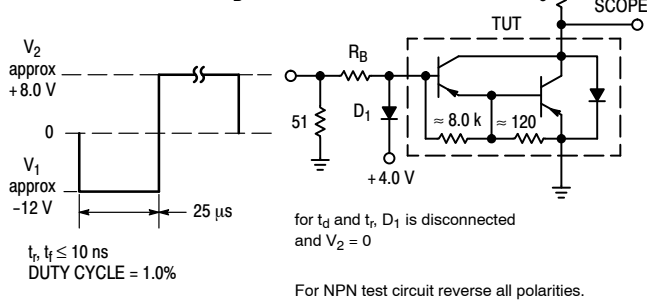


Figure 3. Switching Times Test Circuit

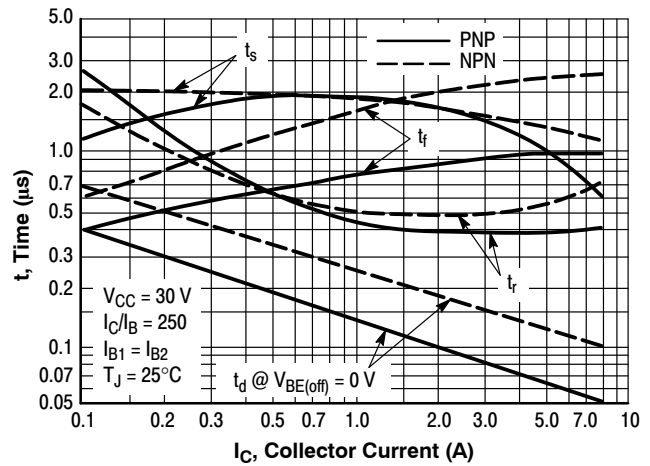


Figure 4. Switching Times

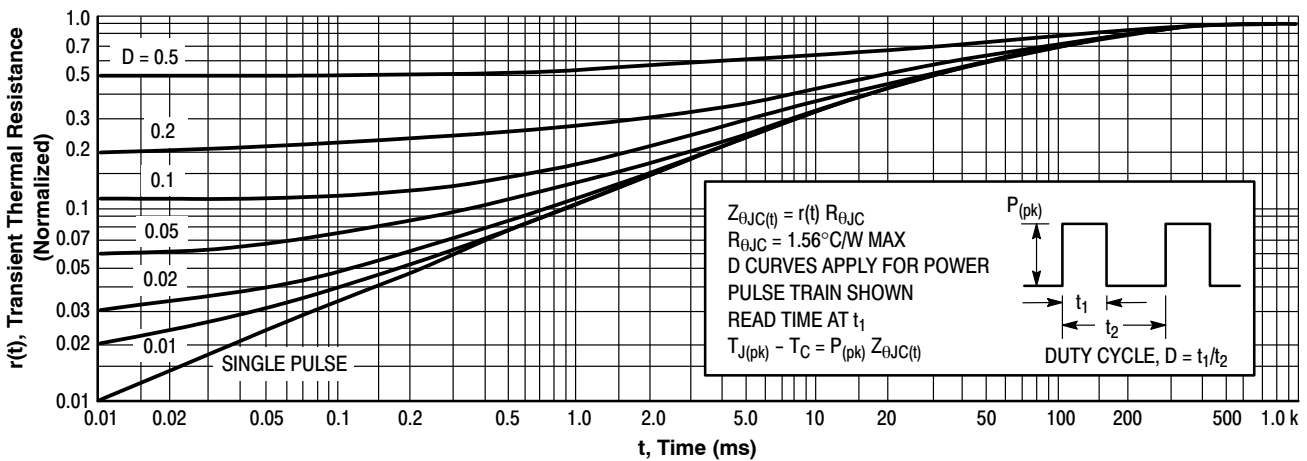


Figure 5. Thermal Response

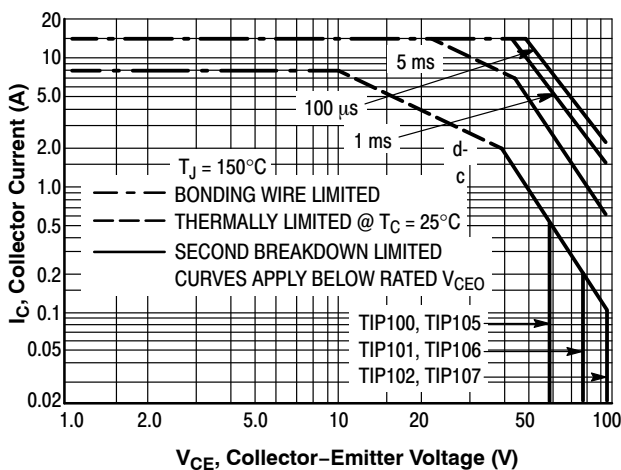


Figure 6. Active-Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown

TIP100, TIP101, TIP102 (NPN); TIP105, TIP106, TIP107 (PNP)

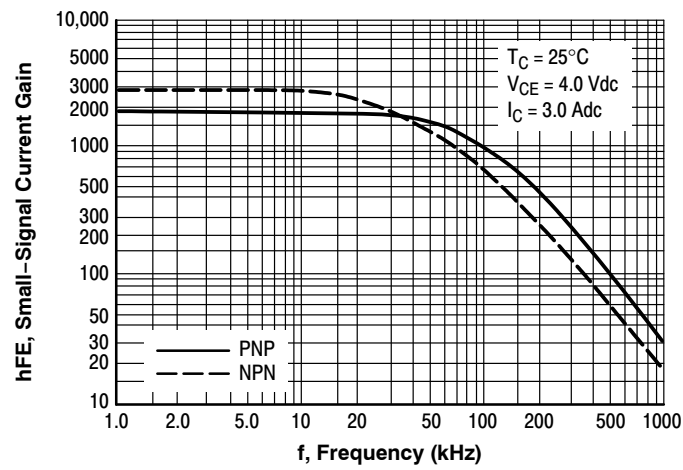


Figure 7. Small-Signal Current Gain

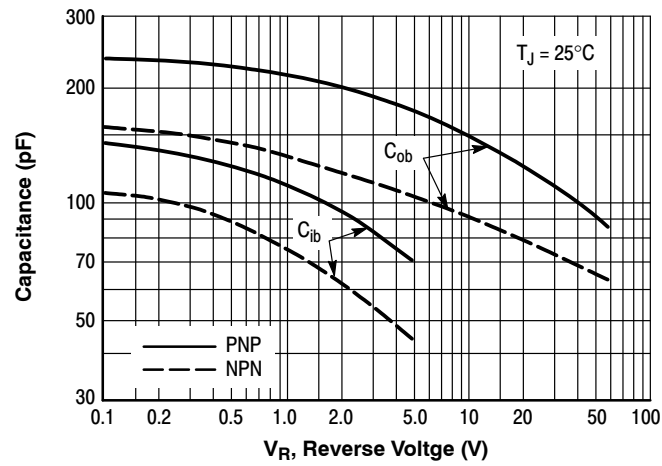


Figure 8. Capacitance

TIP100, TIP101, TIP102 (NPN); TIP105, TIP106, TIP107 (PNP)

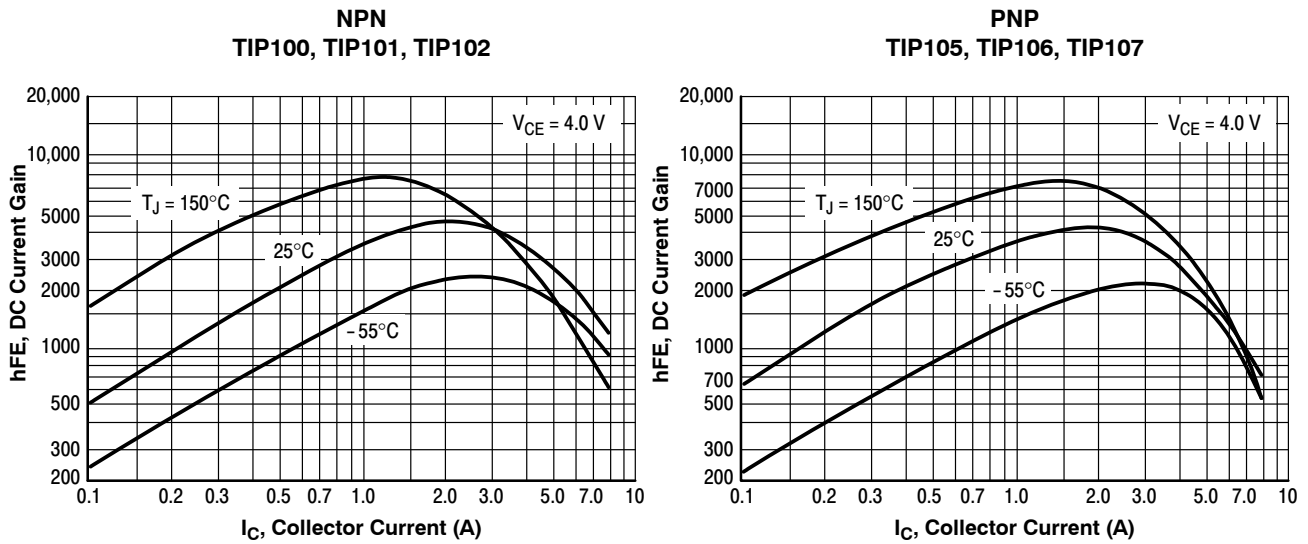


Figure 9. DC Current Gain

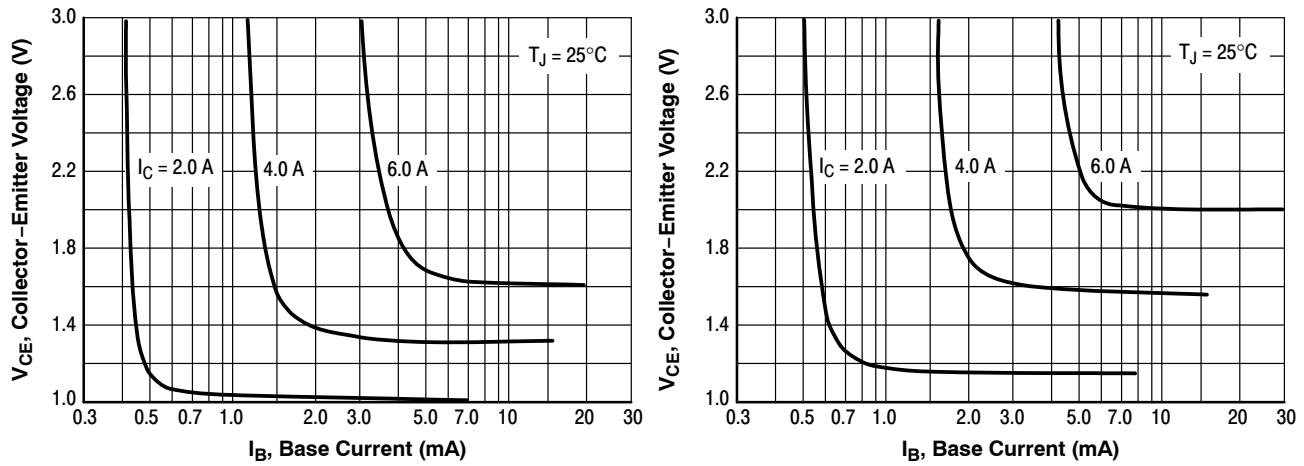


Figure 10. Collector Saturation Region

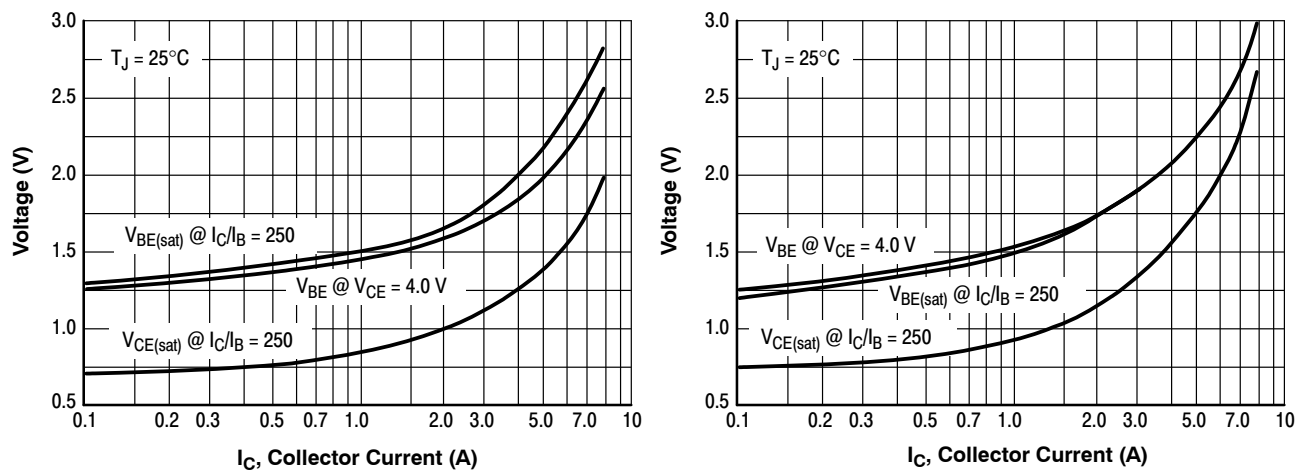


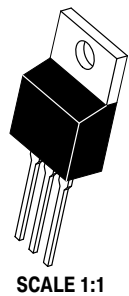
Figure 11. "On" Voltages

TIP100, TIP101, TIP102 (NPN); TIP105, TIP106, TIP107 (PNP)

ORDERING INFORMATION

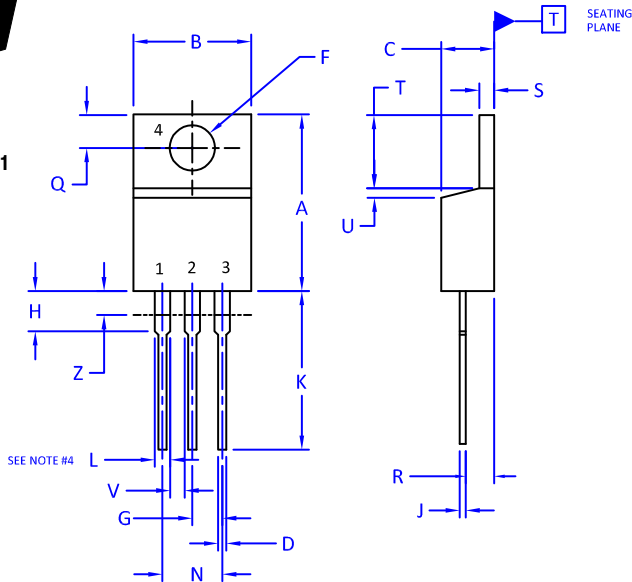
Device	Package	Shipping
TIP100	TO-220	50 Units / Rail
TIP100G	TO-220 (Pb-Free)	50 Units / Rail
TIP101	TO-220	50 Units / Rail
TIP101G	TO-220 (Pb-Free)	50 Units / Rail
TIP102	TO-220	50 Units / Rail
TIP102G	TO-220 (Pb-Free)	50 Units / Rail
TIP105	TO-220	50 Units / Rail
TIP105G	TO-220 (Pb-Free)	50 Units / Rail
TIP106	TO-220	50 Units / Rail
TIP106G	TO-220 (Pb-Free)	50 Units / Rail
TIP107	TO-220	50 Units / Rail
TIP107G	TO-220 (Pb-Free)	50 Units / Rail

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



TO-220 CASE 221A ISSUE AK

DATE 13 JAN 2022



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. MAX WIDTH FOR F102 DEVICE = 1.35MM

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.570	0.620	14.48	15.75
B	0.380	0.415	9.66	10.53
C	0.160	0.190	4.07	4.83
D	0.025	0.038	0.64	0.96
F	0.142	0.161	3.60	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.024	0.36	0.61
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.41
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	----	1.15	---
Z	----	0.080	---	2.04

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

STYLE 3:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 4:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 6:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

STYLE 8:
PIN 1. CATHODE
2. ANODE
3. EXTERNAL TRIP/DELAY
4. ANODE

STYLE 9:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 10:
PIN 1. GATE
2. SOURCE
3. DRAIN
4. SOURCE

STYLE 11:
PIN 1. DRAIN
2. SOURCE
3. GATE
4. SOURCE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. NOT CONNECTED

DOCUMENT NUMBER:	98ASB42148B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	TO-220	PAGE 1 OF 1

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales