CAT853, CAT859, CAT863, CAT869

3-Pin Microprocessor Power Supply Supervisors

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Description

The CAT853, CAT863, CAT859, and CAT869 are supervisory circuits that monitor power supplies in digital systems.

These devices generate a reset signal, which is asserted while the power supply voltage is below a preset threshold level and for at least 140 ms after the power supply level has risen above that level. Industry standard threshold levels are offered to support +3.3 V or 5.0 V systems.

The CAT859 and CAT869 feature a $\overline{\text{RESET}}$ push−pull output (active low) for the two pinout options.

The CAT853 and CAT863 feature an open drain $\overline{\text{RESET}}$ output (active low). Both require a pull−up resistor on the RESET output.

Fast transients on the power supply are ignored and the output is guaranteed to be in the correct state at V_{CC} levels as low as 1.0 V.

Features

- Precision Monitoring of +3.3 V (−5%, −10%), 5 V (−10% Power Supplies)
- Active Low Reset Output
- Reset Valid down to V_{CC} = 1.0 V
- 6 μA Power Supply Current
- Power Supply Transient Immunity
- Industrial Temperature Range: −40°C to +85°C
- SOT−23 Package
- These Devices are Pb−Free and are RoHS Compliant

Applications

- Computers, Servers, Laptops and Cable Modems
- Wireless Communications
- Embedded Control Systems
- White Goods
- Power Meters
- Intelligent Instruments
- PDAs and Handheld Equipment

Table 1. THRESHOLD SUFFIX SELECTOR

Nominal Threshold Voltage	Threshold Suffix Designation
4.63 V	L
4.38 V	M
4.20 V	F
4.00 V	J
3.08 V	T
2.93 V	S
2.63 V	R
2.40 V	C
2.32 V	Z

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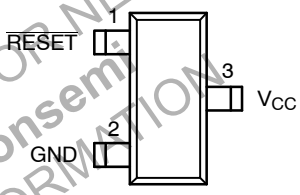
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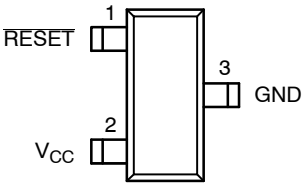
SOT−23
TB SUFFIX
CASE 527AG

PIN CONFIGURATION

CAT853, CAT859

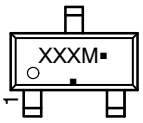


CAT863, CAT869



(Top Views)

MARKING DIAGRAM



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(*Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

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Table 2. PIN DESCRIPTION

Pin Name	Function
$\overline{\text{RESET}}$	Active low reset. $\overline{\text{RESET}}$ is asserted if V_{CC} falls below the reset threshold and remains low for at least 140 ms after V_{CC} rises above the reset threshold
GND	Ground
V_{CC}	Power supply voltage that is monitored

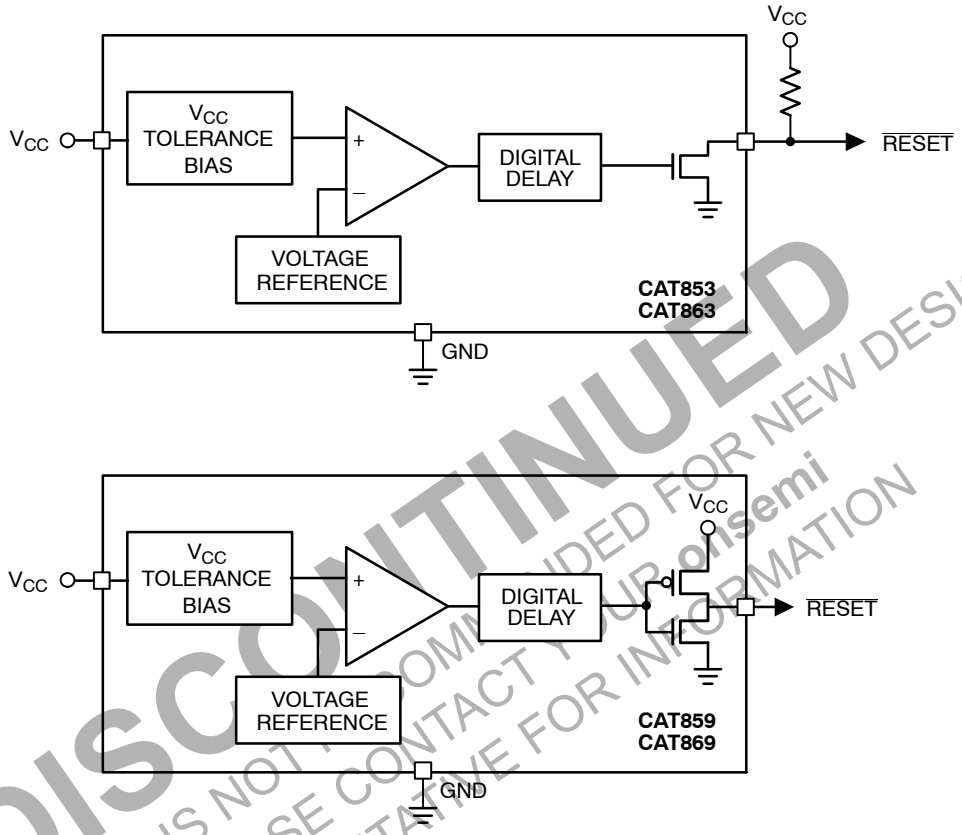


Figure 1. Block Diagrams

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Table 3. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
Any pin with respect to ground	−0.3 to +6.0	V
Input Current, V_{CC}	20	mA
Output Current, $\overline{\text{RESET}}$	20	mA
Rate of Rise, V_{CC}	100	V/μs
Continuous Power Dissipation Derate 4 mW/°C above 70°C (SOT23)	320	mW
Operating Temperature Range	−40 to +85	°C
Storage Temperature Range	−65 to +105	°C
Lead Soldering Temperature (10 sec)	300	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 4. ELECTRICAL CHARACTERISTICS (V_{CC} = Full range, T_A = −40°C to +85°C unless otherwise noted. Typical values at T_A = +25°C and V_{CC} = 3.3 V for the C, S, T versions, V_{CC} = 5 V for the M version.)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
	V_{CC} Range	T_A = 0°C to +70°C		1.0		5.5	V
		T_A = −40°C to +85°C		1.2		5.5	
I_{CC}	Supply Current	T_A = −40°C to +85°C	V_{CC} < 3.6 V, C, S, T		6	15	μA
V_{TH}	Reset Threshold Voltage	L Threshold	T_A = +25°C	4.56	4.63	4.70	V
			T_A = −40°C to +85°C	4.50		4.75	
		M Threshold	T_A = +25°C	4.31	4.38	4.45	
			T_A = −40°C to +85°C	4.25		4.50	
		F Threshold	T_A = +25°C	4.14	4.20	4.26	
			T_A = −40°C to +85°C	4.08		4.31	
		J Threshold	T_A = +25°C	3.93	4.00	4.06	
			T_A = −40°C to +85°C	3.89		4.10	
		T Threshold	T_A = +25°C	3.04	3.08	3.11	
			T_A = −40°C to +85°C	3.00		3.15	
		S Threshold	T_A = +25°C	2.89	2.93	2.96	
			T_A = −40°C to +85°C	2.85		3.00	
		R Threshold	T_A = +25°C	2.59	2.63	2.66	
			T_A = −40°C to +85°C	2.55		2.70	
		C Threshold	T_A = +25°C	2.35	2.40	2.45	
			T_A = −40°C to +85°C	2.30		2.50	
		Z Threshold	T_A = +25°C	2.28	2.32	2.35	
			T_A = −40°C to +85°C	2.25		2.38	
	Reset Threshold Tempco				30		ppm/°C
	V_{CC} to Reset Delay	V_{CC} = V_{TH} to (V_{TH} − 100 mV)			20		μs
	Reset Active Timeout Period	T_A = −40°C to +85°C		140	240	460	ms
V_{OL}	$\overline{\text{RESET}}$ Output Voltage Low	V_{CC} = V_{TH} min, I_{SINK} = 1.2 mA				0.4	V
		V_{CC} > 1.0 V, I_{SINK} = 50 μA				0.3	
V_{OH}	$\overline{\text{RESET}}$ Output Voltage High	V_{CC} = V_{TH} max, I_{SOURCE} = −500 μA (for CAT859/869 only)		0.8 V_{CC}			V

1. Production testing done at T_A = +25°C; limits over temperature guaranteed by design only.

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TYPICAL ELECTRICAL OPERATING CHARACTERISTICS

(V_{CC} = Full range, T_A = −40°C to +85°C unless otherwise noted. Typical values at T_A = +25°C and V_{CC} = 3.3 V for the C, S, T versions, V_{CC} = 5 V for the M version.)

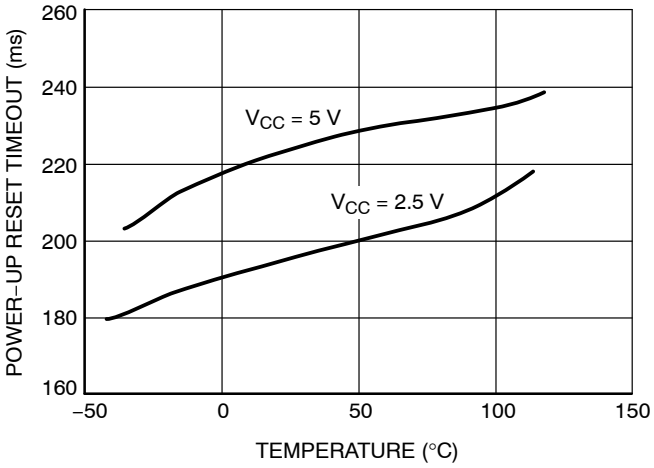


Figure 2. Power−Up Reset Timeout vs. Temperature

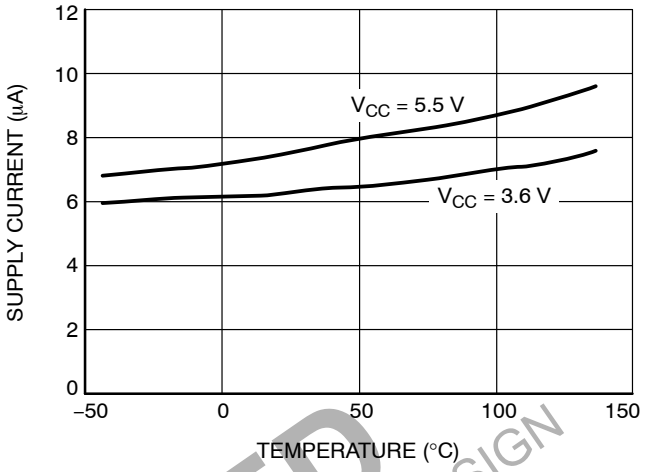


Figure 3. Supply Current vs. Temperature (No Load)

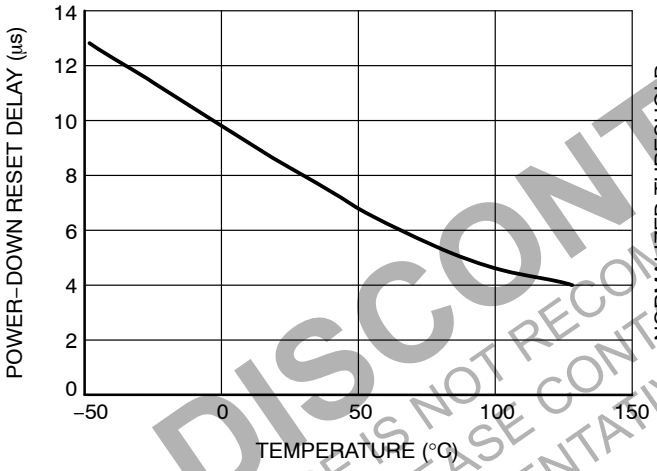


Figure 4. Power−Down Reset Delay vs. Temperature

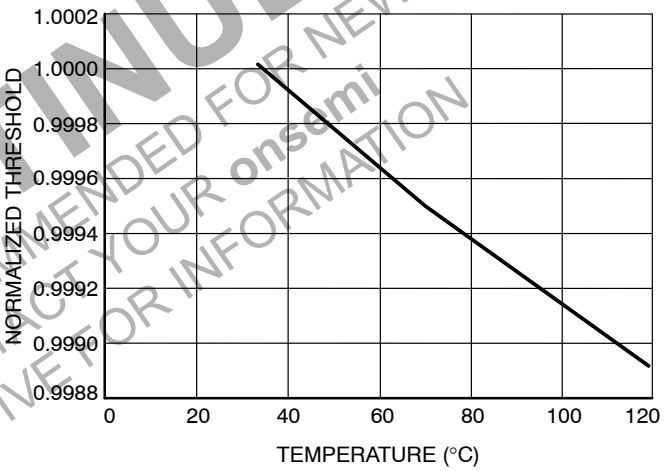


Figure 5. Normalized Reset Threshold vs. Temperature

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DETAILED DESCRIPTION

Reset Timing

The reset signal is asserted low for the CAT853, CAT863, CAT859, and CAT869 when the power supply voltage falls below the threshold trip voltage and remains asserted for at least 140 ms after the power supply voltage has risen above the threshold.

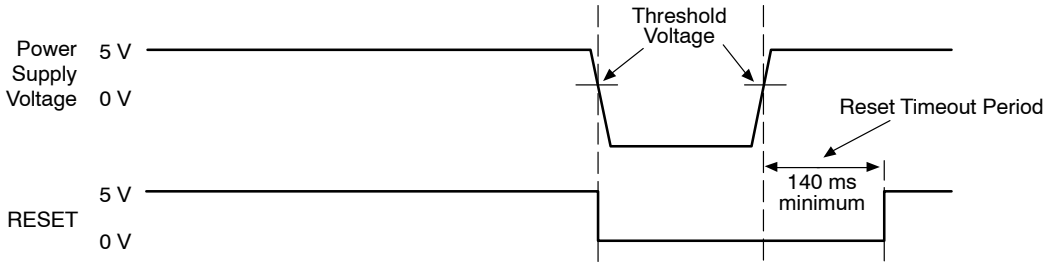


Figure 6. Reset Timing Diagram

V_{CC} Transient Response

The CAT853, CAT863, CAT859, and CAT869 protect μPs against brownout failure. Short duration transients of 4 μs or less and 100 mV amplitude typically do not cause a false RESET.

Figure 7 shows the maximum pulse duration of negative−going V_{CC} transients that do not cause a reset condition. As the amplitude of the transient goes further below the threshold (increasing $V_{TH} - V_{CC}$), the maximum pulse duration decreases. In this test, the V_{CC} starts from an initial voltage of 0.5 V above the threshold and drops below it by the amplitude of the overdrive voltage ($V_{TH} - V_{CC}$).

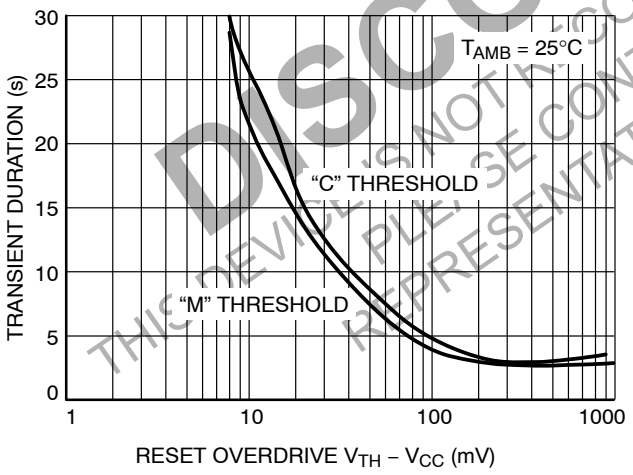


Figure 7. Maximum Transient Duration Without Causing a Reset Pulse vs. Reset Comparator Overdrive

Valid Reset with V_{CC} under 1.0 V

To ensure that the CAT859 and CAT869 $\overline{\text{RESET}}$ pin is in a known state when V_{CC} is under 1.0 V, a > 10 kΩ pull−down resistor between $\overline{\text{RESET}}$ pin and GND is recommended.

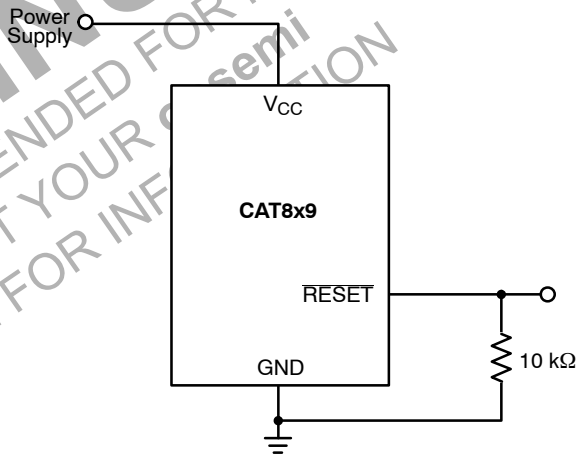


Figure 8. $\overline{\text{RESET}}$ Valid with V_{CC} Under 1.0 V

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Bi−directional Reset Pin Interfacing

The CAT859 and CAT869 can interface with μP/μC bi−directional reset pins by connecting a 4.7 kΩ resistor in series with the CAT859 and CAT869 reset output and the μP/μC bi−directional reset pin.

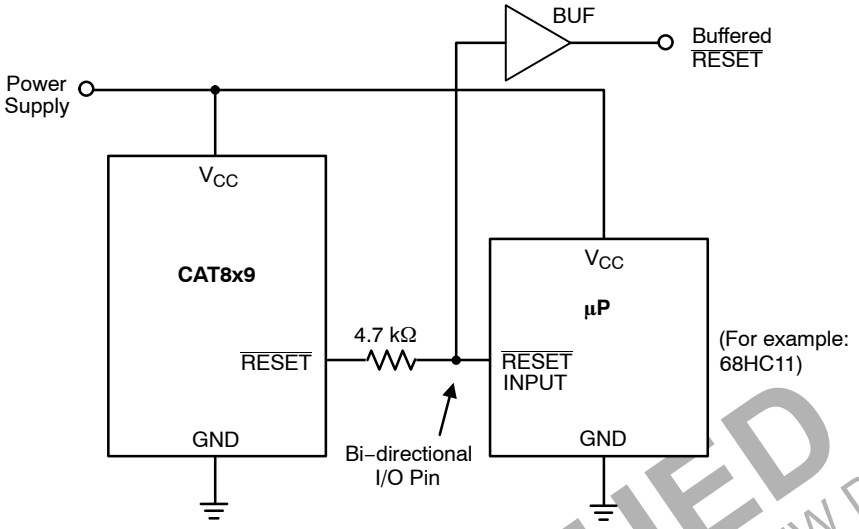


Figure 9. Bi−directional Reset Pin Interfacing

CAT853 and CAT863 Open−Drain RESET Application

The CAT853 and CAT863 features an open−drain RESET output and therefore need a pull−up resistor on the output for proper operation, as shown on Figure 10. An advantage of the open−drain output includes the ability to "wire AND" several outputs together to form an inexpensive logic circuit. It is also possible to have the pull−up resistor connected to a different supply which can be higher than the CAT8x3 V_{CC} pin. The value of the pull−up resistor is not critical in most applications, typical values being between 5 kΩ and 10 kΩ.

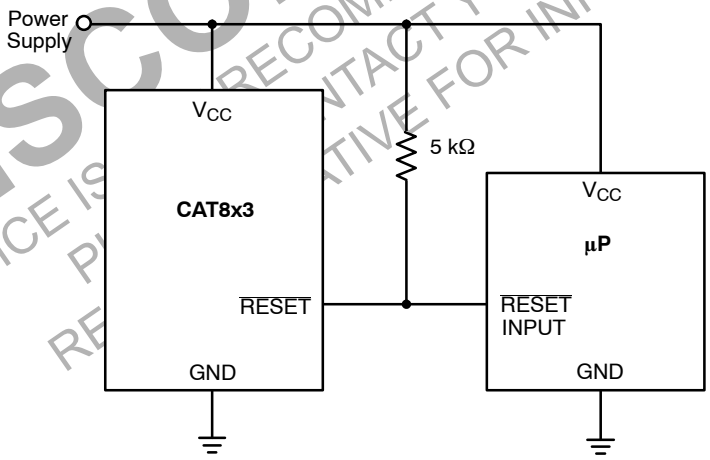


Figure 10. Typical CAT8x3 Open−Drain Circuit Configuration

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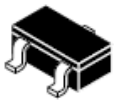
ORDERING INFORMATION

Order Number		Voltage	Top Mark (Note 2)		Reset	Package	Quantity per Reel (Note 3)
NiPdAu	Matte−Tin		NiPdAu	Matte−Tin			
CAT853LTBI−GT3	CAT853LTBI−T3	4.63 V	VPA	VPR	LOW	SOT−23−3	3,000
CAT853MTBI−GT3	CAT853MTBI−T3	4.38 V	VPA	VPR			
CAT853FTBI−GT3	CAT853FTBI−T3	4.20 V	VPA	VPR			
CAT853JTBI−GT3	CAT853JTBI−T3	4.00 V	VPA	VPR			
CAT853TTBI−GT3	CAT853TTBI−T3	3.08 V	VPA	VPR			
CAT853STBI−GT3	CAT853STBI−T3	2.93 V	VPA	VPR			
CAT853RTBI−GT3	CAT853RTBI−T3	2.63 V	VPA	VPR			
CAT853CTBI−GT3	CAT853CTBI−T3	2.40 V	VPA	VPR			
CAT853ZTBI−GT3	CAT853ZTBI−T3	2.32 V	VPA	VPR			
CAT859LTBI−GT3	CAT859LTBI−T3	4.63 V	VNA	VNR	LOW	SOT−23−3	3,000
CAT859MTBI−GT3	CAT859MTBI−T3	4.38 V	VNA	VNR			
CAT859FTBI−GT3	CAT859FTBI−T3	4.20 V	VNA	VNR			
CAT859JTBI−GT3	CAT859JTBI−T3	4.00 V	VNA	VNR			
CAT859TTBI−GT3	CAT859TTBI−T3	3.08 V	VNA	VNR			
CAT859STBI−GT3	CAT859STBI−T3	2.93 V	VNA	VNR			
CAT859RTBI−GT3	CAT859RTBI−T3	2.63 V	VNA	VNR			
CAT859CTBI−GT3	CAT859CTBI−T3	2.40 V	VNA	VNR			
CAT859ZTBI−GT3	CAT859ZTBI−T3	2.32 V	VNA	VNR			
CAT863LTBI−GT3	CAT863LTBI−T3	4.63 V	VNB	VNK	LOW	SOT−23−3	3,000
CAT863MTBI−GT3	CAT863MTBI−T3	4.38 V	VNB	VNK			
CAT863FTBI−GT3	CAT863FTBI−T3	4.20 V	VNB	VNK			
CAT863JTBI−GT3	CAT863JTBI−T3	4.00 V	VNB	VNK			
CAT863TTBI−GT3	CAT863TTBI−T3	3.08 V	VNB	VNK			
CAT863STBI−GT3	CAT863STBI−T3	2.93 V	VNB	VNK			
CAT863RTBI−GT3	CAT863RTBI−T3	2.63 V	VNB	VNK			
CAT863CTBI−GT3	CAT863CTBI−T3	2.40 V	VNB	VNK			
CAT863ZTBI−GT3	CAT863ZTBI−T3	2.32 V	VNB	VNK			
CAT869LTBI−GT3	CAT869LTBI−T3	4.63 V	VNC	VNJ	LOW	SOT−23−3	3,000
CAT869MTBI−GT3	CAT869MTBI−T3	4.38 V	VNC	VNJ			
CAT869FTBI−GT3	CAT869FTBI−T3	4.20 V	VNC	VNJ			
CAT869JTBI−GT3	CAT869JTBI−T3	4.00 V	VNC	VNJ			
CAT869TTBI−GT3	CAT869TTBI−T3	3.08 V	VNC	VNJ			
CAT869STBI−GT3	CAT869STBI−T3	2.93 V	VNC	VNJ			
CAT869RTBI−GT3	CAT869RTBI−T3	2.63 V	VNC	VNJ			
CAT869CTBI−GT3	CAT869CTBI−T3	2.40 V	VNC	VNJ			
CAT869ZTBI−GT3	CAT869ZTBI−T3	2.32 V	VNC	VNJ			

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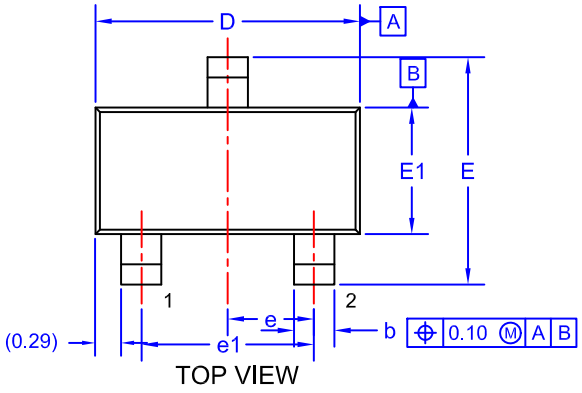
2. Threshold and full part numbers will be provided on box and reel labels as well as all Shipping documents.
3. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
4. For detailed information and a breakdown of device nomenclature and numbering systems, please see the ON Semiconductor Device Nomenclature document, TND310/D, available at www.onsemi.com

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



SOT−23/SUPERSOT™ −23, 3 LEAD, 1.4x2.9
CASE 527AG
ISSUE A

DATE 09 DEC 2019

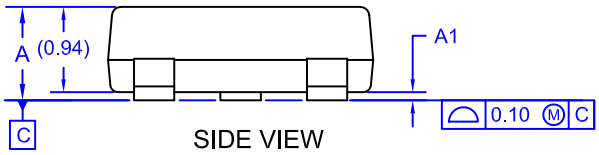


TOP VIEW

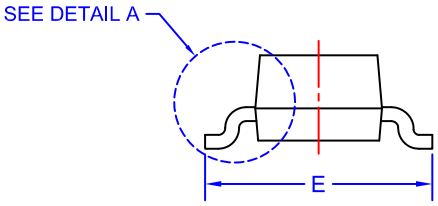
NOTES: UNLESS OTHERWISE SPECIFIED

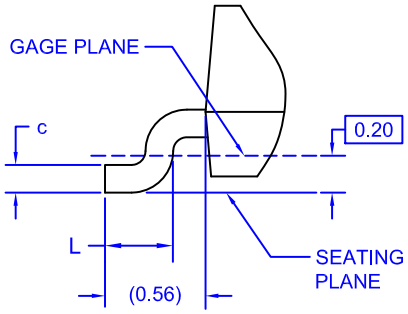
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.

DIM	MIN.	NOM.	MAX.
A	0.85	0.95	1.12
A1	0.00	0.05	0.10
b	0.370	0.435	0.508
c	0.085	0.150	0.180
D	2.80	2.92	3.04
E	2.31	2.51	2.71
E1	1.20	1.40	1.52
e	0.95 BSC		
e1	1.90 BSC		
L	0.33	0.38	0.43

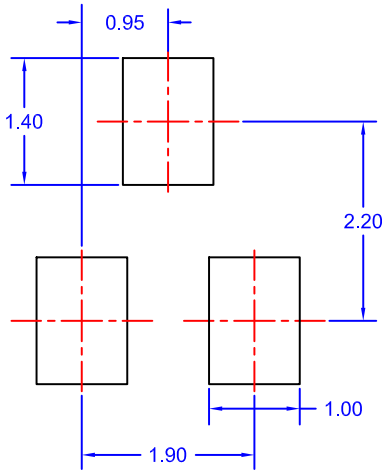


SIDE VIEW





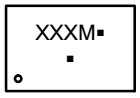
DETAIL A



LAND PATTERN RECOMMENDATION*

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Month Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON34319E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**SOT−23/SUPERSOT−23, 3 LEAD, 1.4X2.9**	**PAGE 1 OF 1**

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