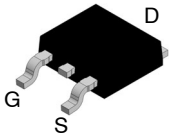
MOSFET – N-Channel, QFET

200 V, 9.0 A, 280 mΩ

FQD12N20L

V_{DSS}	$R_{DS(on)}$ MAX	I_D MAX
200 V	280 mΩ @ 10 V	9.0 A



DPAK3 (TO−252 3 LD)
CASE 369AS

Description

This N−Channel enhancement mode power MOSFET is produced using **onsemi**'s proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on−state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

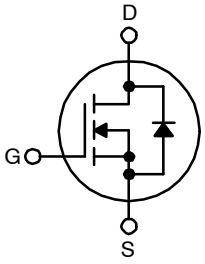
Features

- 9.0 A, 200 V, $R_{DS(on)}$ = 280 mΩ (Max.) @ V_{GS} = 10 V, I_D = 4.5 A
- Low Gate Charge (Typ. 16 nC)
- Low Crss (Typ. 17 pF)
- 100% Avalanche Tested

MARKING DIAGRAM



&Z	= Assembly Plant Code
&3	= 3−Digit Date Code
&K	= 2−Digits Lot Run Traceability Code
FQD12N20L	= Device Code



N−Channel MOSFET

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, unless otherwise noted)

Symbol	Parameter		Rating	Unit
V_{DSS}	Drain−Source Voltage		200	V
I_D	Drain Current	− Continuous (T_C = 25°C)	9.0	A
		− Continuous (T_C = 100°C)	5.7	A
I_{DM}	Drain Current	− Pulsed (Note 1)	36	A
V_{GSS}	Gate−Source Voltage		±20	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		210	mJ
I_{AR}	Avalanche Current (Note 1)		9.0	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		5.5	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		5.5	V/ns
P_D	Power Dissipation (T_A = 25°C) *		2.5	W
	Power Dissipation (T_C = 25°C)		55	W
		− Derate Above 25°C	0.44	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		−55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 seconds		300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Rating	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	2.27	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Minimum Pad of 2−oz Copper), Max.	110	
	Thermal Resistance, Junction to Ambient (*1 in^2 Pad of 2−oz Copper), Max.	50	

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain−Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	200	–	–	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	–	0.14	–	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 200 V, V_{GS} = 0 V	–	–	1	μA
		V_{DS} = 160 V, T_C = 125°C	–	–	10	μA
I_{GSSF}	Gate−Body Leakage Current, Forward	V_{GS} = 20 V, V_{DS} = 0 V	–	–	100	nA
I_{GSSR}	Gate−Body Leakage Current, Reverse	V_{GS} = −20 V, V_{DS} = 0 V	–	–	−100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	1.0	–	2.0	V
$R_{DS(on)}$	Static Drain−Source On−Resistance	V_{GS} = 10 V, I_D = 4.5 A V_{GS} = 5 V, I_D = 4.5 A	– –	0.22 0.25	0.28 0.32	Ω
g_{FS}	Forward Transconductance	V_{DS} = 30 V, I_D = 4.5 A	–	11.6	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	–	830	1080	pF
C_{oss}	Output Capacitance		–	120	155	pF
C_{rss}	Reverse Transfer Capacitance		–	17	22	pF
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 100 V, I_D = 11.6 A, R_G = 25 Ω (Note 4)	–	15	40	ns
t_r	Turn−On Rise Time		–	190	390	ns
$t_{d(off)}$	Turn−Off Delay Time		–	60	130	ns
t_f	Turn−Off Fall Time		–	120	250	ns
Q_g	Total Gate Charge	V_{DS} = 160 V, I_D = 11.6 A, V_{GS} = 5 V (Note 4)	–	16	21	nC
Q_{gs}	Gate−Source Charge		–	2.8	–	nC
Q_{gd}	Gate−Drain Charge		–	7.6	–	nC
DRAIN−SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain−Source Diode Forward Current		–	–	9.0	A
I_{SM}	Maximum Pulsed Drain−Source Diode Forward Current		–	–	36	A
V_{SD}	Drain−Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 9.0 A	–	–	1.5	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 11.6 A, dI_F / dt = 100 A/μs	–	128	–	ns
Q_{rr}	Reverse Recovery Charge		–	0.56	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Repetitive rating: pulse−width limited by maximum junction temperature.
2. L = 3.9 mH, I_{AS} = 9.0 A, V_{DD} = 50 V, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 11.6 A, di/dt ≤ 300 A/μs, V_{DD} ≤ BV_{DSS}, starting T_J = 25°C.
4. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

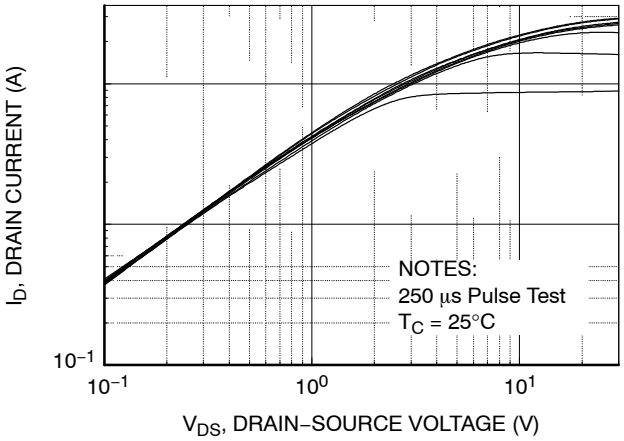


Figure 1. On−Region Characteristics

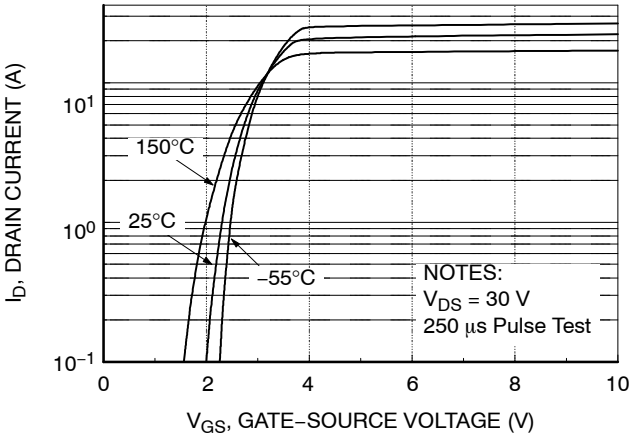


Figure 2. Transfer Characteristics

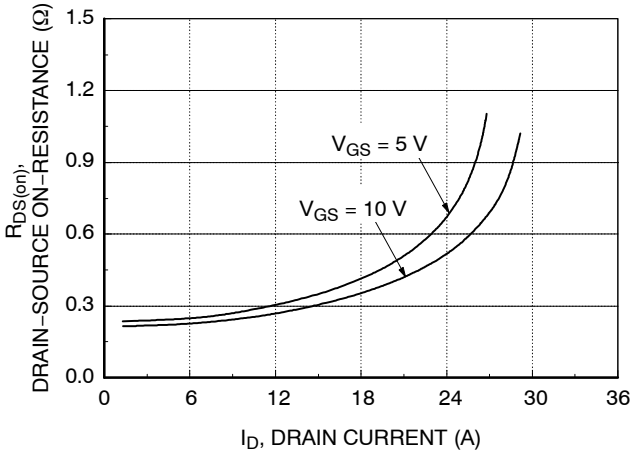


Figure 3. On−Resistance Variation vs. Drain Current and Gate Voltage

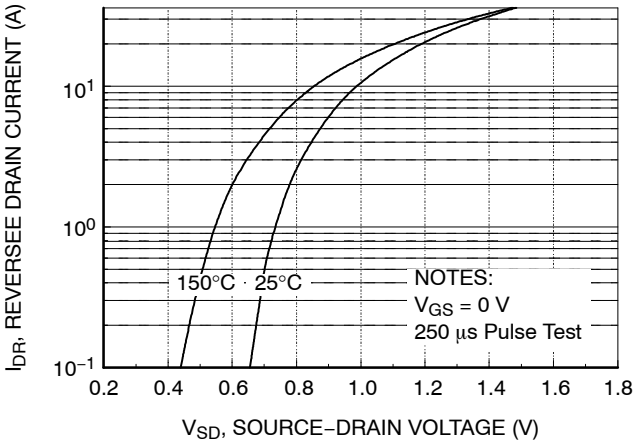


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

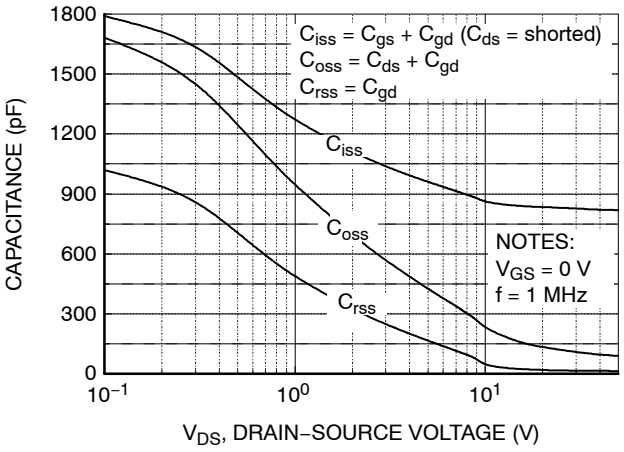


Figure 5. Capacitance Characteristics

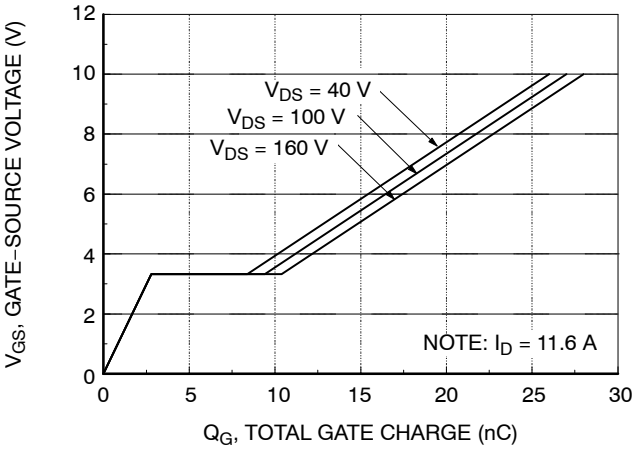


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS (continued)

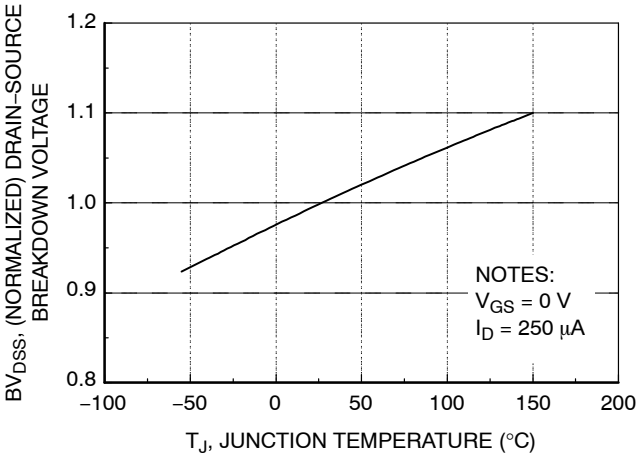


Figure 7. Breakdown Voltage Variation vs. Temperature

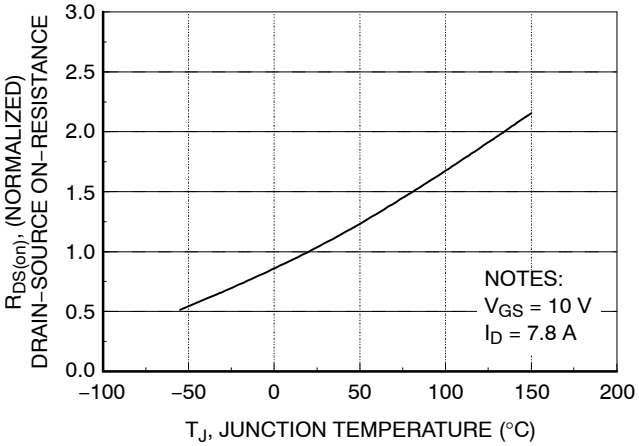


Figure 8. On−Resistance Variation vs. Temperature

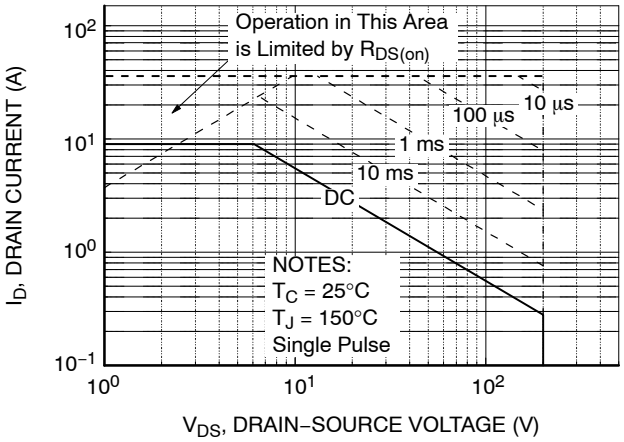


Figure 9. Maximum Safe Operating Area

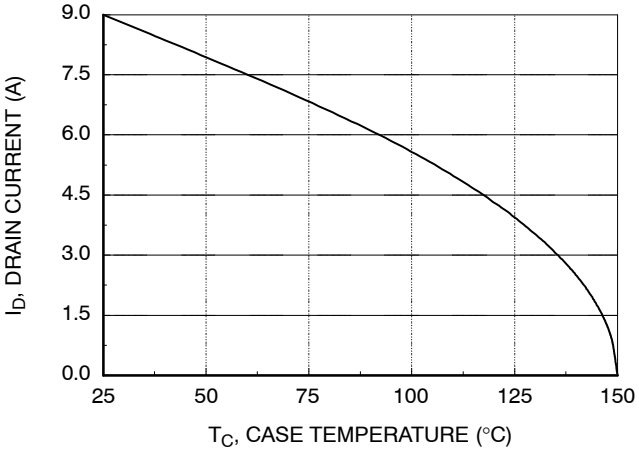


Figure 10. Maximum Drain Current vs. Case Temperature

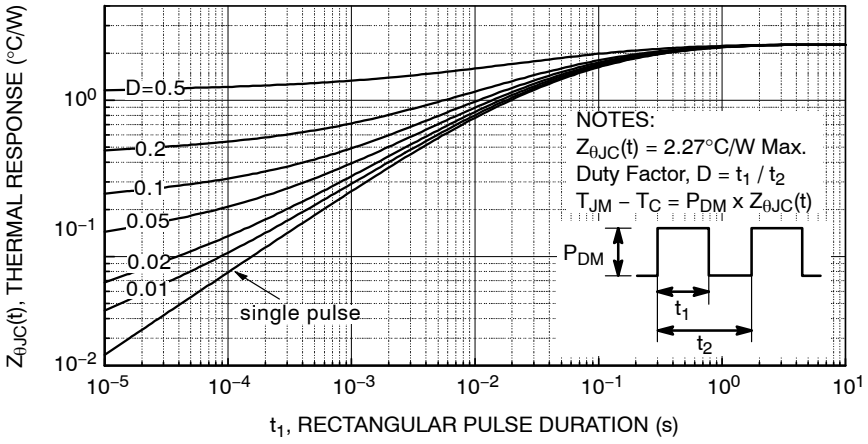


Figure 11. Transient Thermal Response Curve

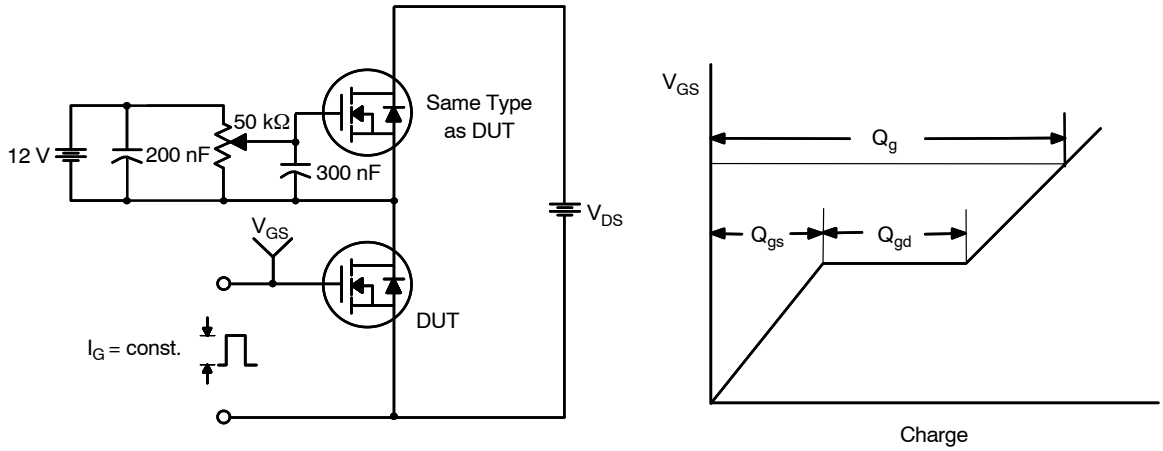


Figure 12. Gate Charge Test Circuit & Waveform

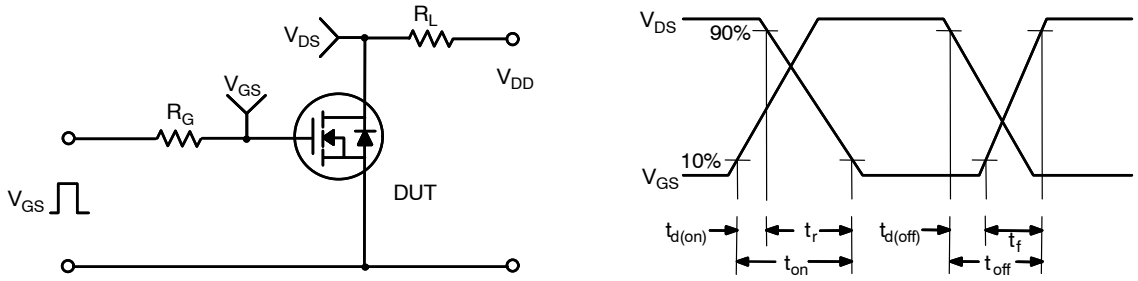


Figure 13. Resistive Switching Test Circuit & Waveforms

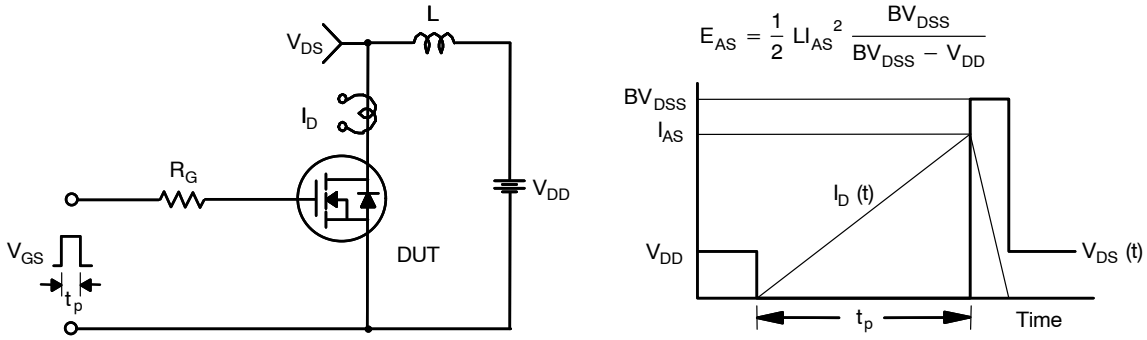


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

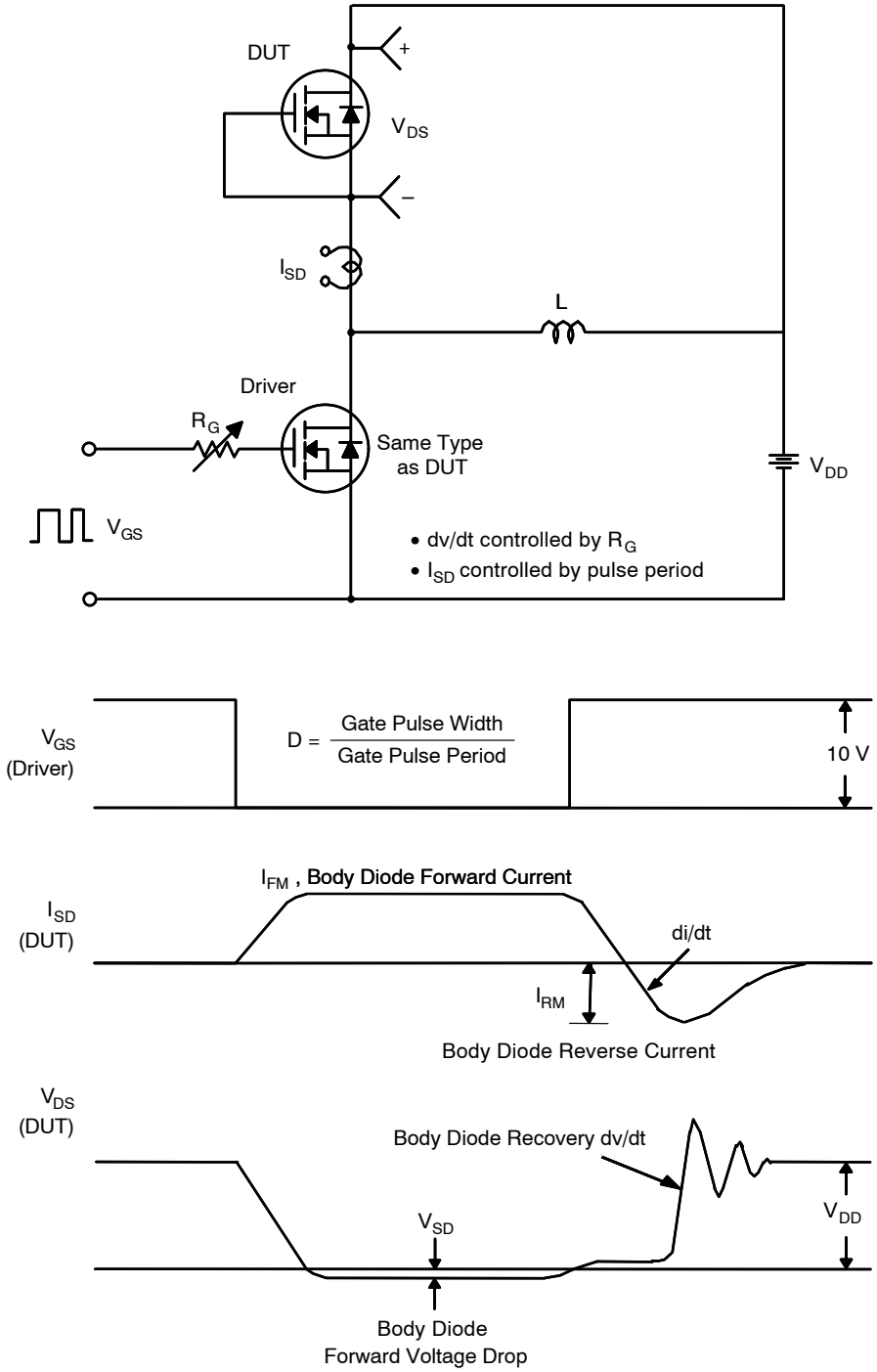


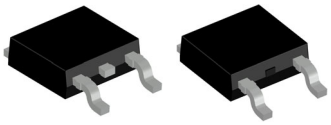
Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Shipping†
FQD12N20LTM	FQD12N20L	DPAK3 (TO−252 3 LD)	2500 / Tape & Reel

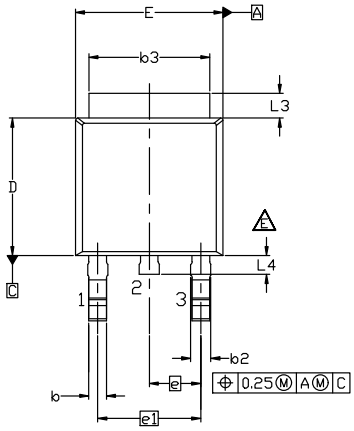
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

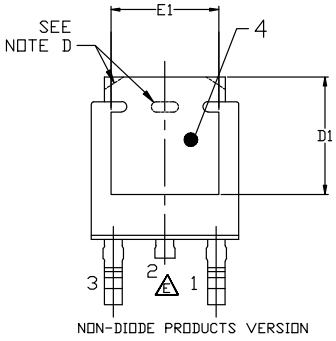


DPAK3 6.10x6.54x2.29, 4.57P
CASE 369AS
ISSUE B

DATE 20 DEC 2023

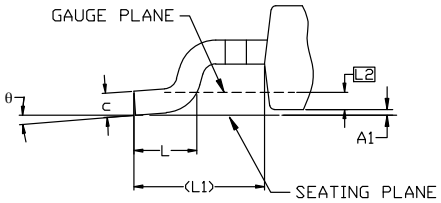


NON-DIODE PRODUCTS VERSION



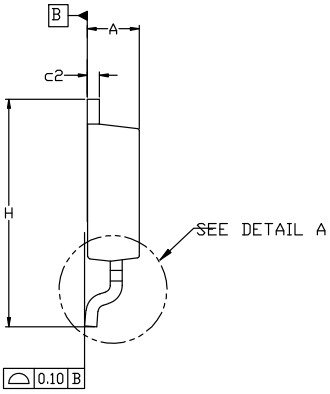
NON-DIODE PRODUCTS VERSION

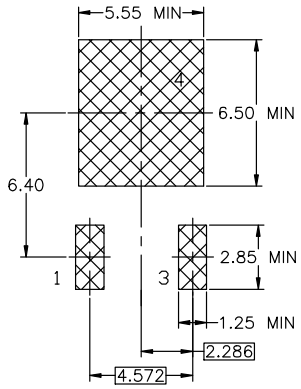
NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE F, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2018.
D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
E) FOR DIODE PRODUCTS, L4 IS 0.25 MM MAX PLASTIC BODY STUB WITHOUT CENTER LEAD.
F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.



DETAIL A
(ROTATED -90°)
SCALE: 12X

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.18	2.29	2.39
A1	0.00	–	0.127
b	0.64	0.77	0.89
b2	0.76	0.95	1.14
b3	5.21	5.34	5.46
c	0.45	0.53	0.61
c2	0.45	0.52	0.58
D	5.97	6.10	6.22
D1	5.21	---	---
E	6.35	6.54	6.73
E1	4.32	---	---
e	2.286 BSC		
e1	4.572 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	1.08	1.27
L4	---	---	1.02
θ	0°	---	10°





LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

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DESCRIPTION:	**DPAK3 6.10x6.54x2.29, 4.57P**	**PAGE 1 OF 1**

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