2.5 V/3.3 V Differential 2 x 2 Crosspoint Switch with CML Outputs Clock/Data Buffer/Translator

Multi−Level Inputs w/ Internal Termination

NB7L72M



QFN16
MN SUFFIX
CASE 485G

MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

Description

The NB7L72M is a high bandwidth, low voltage, fully differential 2 x 2 crosspoint switch with CML outputs. The NB7L72M design is optimized for low skew and minimal jitter as it produces two identical copies of Clock or Data operating up to 7 GHz or 10 Gb/s, respectively. As such, the NB7L72M is ideal for SONET, GigE, Fiber Channel, Backplane and other clock/data distribution applications.

The differential IN/$\overline{\text{IN}}$ inputs incorporate internal 50 Ω termination resistors and will accept LVPECL, CML, or LVDS logic levels (see Figure 11). The 16 mA differential CML outputs provide matching internal 50 Ω terminations and produce 400 mV output swings when externally terminated with a 50 Ω resistor to V_{CC} (see Figure 9).

The NB7L72M is the 2.5 V/3.3 V version of the and NB7V72M and is offered in a low profile 3x3 mm 16−pin QFN package. Application notes, models, and support documentation are available at www.onsemi.com.

The NB7L72M is a member of the GigaComm™ family of high performance clock products.

Features

- Maximum Input Data Rate > 10 Gb/s
- Data Dependent Jitter < 10 ps pk−pk
- Maximum Input Clock Frequency > 7 GHz
- Random Clock Jitter < 0.5 ps RMS, Max
- 150 ps Typical Propagation Delay
- 30 ps Typical Rise and Fall Times
- Differential CML Outputs, 400 mV peak−to−peak, typical
- Operating Range: V_{CC} = 2.375 V to 3.6 V with GND = 0 V
- Internal 50 Ω Input Termination Resistors
- QFN16 Package, 3mm x 3mm
- −40°C to +85°C Ambient Operating Temperature
- These are Pb−Free Devices

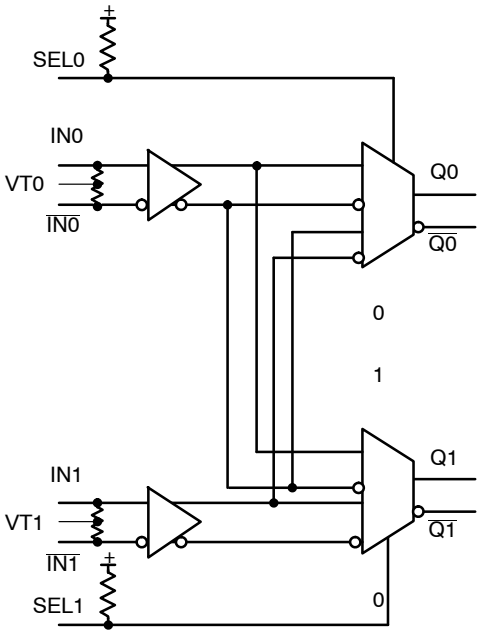


Figure 1. Logic Diagram[1]

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

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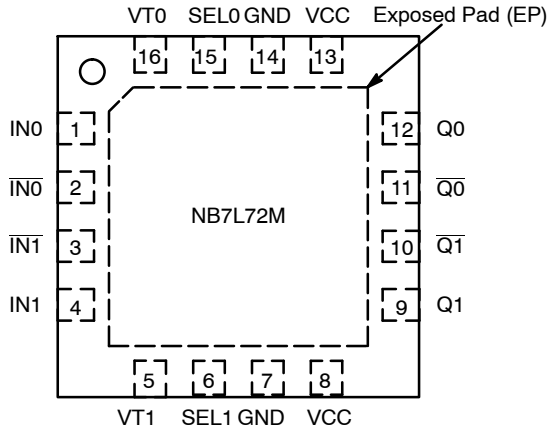


Figure 2. Pin Configuration (Top View)

Table 1. INPUT/OUTPUT SELECT TRUTH TABLE

SEL0*	SEL1*	Q0	Q1
L	L	IN0	IN0
L	H	IN0	IN1
H	L	IN1	IN0
H	H	IN1	IN1

*Defaults HIGH when left open

Table 2. PIN DESCRIPTION

Pin	Name	I/O	Description
1	IN0	LVPECL, CML, LVDS Input	Noninverted Differential Input. (Note 1)
2	$\overline{IN0}$	LVPECL, CML, LVDS Input	Inverted Differential Input. (Note 1)
3	$\overline{IN1}$	LVPECL, CML, LVDS Input	Inverted Differential Input. (Note 1)
4	IN1	LVPECL, CML, LVDS Input	Noninverted Differential Input. (Note 1)
5	VT1	–	Internal 50 Ω Termination Pin for IN1 and $\overline{IN1}$.
6	SEL1	LVCMOS Input	Input Select logic pin for IN0 or IN1 Inputs to Q1 output. See Table 1, Input/Output Select Truth Table; pin defaults HIGH when left open.
7	GND		Negative Supply Voltage
8	VCC	–	Positive Supply Voltage
9	Q1	CML Output	Noninverted Differential Output. (Note 1)
10	$\overline{Q1}$	CML Output	Inverted Differential Output. (Note 1)
11	$\overline{Q0}$	CML Output	Inverted Differential Output. (Note 1)
12	Q0	CML Output	Noninverted Differential Output. (Note 1)
13	VCC	–	Positive Supply Voltage
14	GND	–	Negative Supply Voltage
15	SEL0	LVCMOS Input	Input Select logic pin for IN0 or IN1 Inputs to Q0 output. See Table 1, Input/Output Select Truth Table; pin defaults HIGH when left open.
16	VT0	–	Internal 50 Ω Termination Pin for IN0 and $\overline{IN0}$
–	EP	–	The Exposed Pad (EP) on the QFN16 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat−sinking conduit. The pad is electrically connected to the die, and is recommended to be electrically and thermally connected to GND on the PC board.

1. In the differential configuration when the input termination pins (VT0, VT1) are connected to a common termination voltage or left open, and if no signal is applied on INx/$\overline{INx}$ input, then the device will be susceptible to self−oscillation.
2. All VCC and GND pins must be externally connected to a power supply for proper operation.

Table 3. ATTRIBUTES

Characteristics	Value
ESD Protection Human Body Model Machine Model	 > 4 kV > 200 V
R_{PU} – Input Pullup Resistor	75 kΩ
Moisture Sensitivity (Note 3) QFN16	 Level 1
Flammability Rating Oxygen Index: 28 to 34	 UL 94 V−0 @ 0.125 in
Transistor Count	212
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

3. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Positive Power Supply	GND = 0 V		4.0	V
V_{IN}	Positive Input Voltage	GND = 0 V		−0.5 to V_{CC} +0.5	V
V_{INPP}	Differential Input Voltage |IN − $\overline{IN}$|			1.89	V
I_{IN}	Input Current Through R_T (50 Ω Resistor)			±40	mA
I_{OUT}	Output Current Through R_T (50 Ω Resistor)			±40	mA
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient) (Note 4)	0 lfpm 500 lfpm	QFN16 QFN16	42 35	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case) (Note 4)		QFN16	4	°C/W
T_{sol}	Wave Solder Pb−Free			265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

4. JEDEC standard multilayer board − 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

Table 5. DC CHARACTERISTICS, Multi−Level Inputs V_{CC} = 2.375 V to 3.6 V, GND = 0 V, T_A = −40°C to +85°C (Note 5)

Symbol	Characteristic	Min	Typ	Max	Unit
POWER SUPPLY CURRENT					
V_{CC}	Power Supply Voltage V_{CC} = 2.5 V V_{CC} = 3.3 V	2.375 3.0	2.5 3.3	2.625 3.6	V
I_{CC}	Power Supply Current (Inputs and Outputs Open)	80	135	175	mA
CML OUTPUTS					
V_{OH}	Output HIGH Voltage (Note 6) V_{CC} = 3.3 V V_{CC} = 2.5 V	V_{CC} − 40 3260 2460	V_{CC} − 20 3280 2480	V_{CC} 3300 2500	mV
V_{OL}	Output LOW Voltage (Note 6) V_{CC} = 3.3 V V_{CC} = 2.5 V	V_{CC} − 650 2650 V_{CC} − 600 1900	V_{CC} − 500 2800 V_{CC} − 500 2000	V_{CC} − 400 2900 V_{CC} − 350 2150	mV
DIFFERENTIAL CLOCK INPUTS DRIVEN SINGLE−ENDED (Note 7) (Figures 5 and 7)					
V_{th}	Input Threshold Reference Voltage Range (Note 8)	1050		V_{CC} − 100	mV
V_{IH}	Single−Ended Input HIGH Voltage	V_{th} + 100		V_{CC}	mV
V_{IL}	Single−Ended Input LOW Voltage	GND		V_{th} − 100	mV
V_{ISE}	Single−Ended Input Voltage (V_{IH} − V_{IL})	200		2800	mV
DIFFERENTIAL DATA/CLOCK INPUTS DRIVEN DIFFERENTIALLY (Figures 6 and 8) (Note 9)					
V_{IHD}	Differential Input HIGH Voltage (INn, $\overline{INn}$)	1100		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage (INn, $\overline{INn}$)	GND		V_{CC} − 100	mV
V_{ID}	Differential Input Voltage (INn, $\overline{INn}$) (V_{IHD} − V_{ILD})	100		1200	mV
V_{CMR}	Input Common Mode Range (Differential Configuration, Note 10) (Figure 9)	950		V_{CC} − 50	mV
I_{IH}	Input HIGH Current INn, $\overline{INn}$ (VTIN/$\overline{VTIN}$ Open)	−150		150	μA
I_{IL}	Input LOW Current INn, $\overline{INn}$ (VTIN/$\overline{VTIN}$ Open)	−150		150	μA
CONTROL INPUTS (SEL0, SEL1)					
V_{IH}	Input HIGH Voltage for Control Pins	2.0		V_{CC}	V
V_{IL}	Input LOW Voltage for Control Pins	GND		0.8	V
I_{IH}	Input HIGH Current	−150		150	μA
I_{IL}	Input LOW Current	−150		150	μA
TERMINATION RESISTORS					
R_{TIN}	Internal Input Termination Resistor	40	50	60	Ω
R_{TOUT}	Internal Output Termination Resistor	40	50	60	Ω

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

5. Input and output parameters vary 1:1 with V_{CC}.
6. CML outputs loaded with 50 Ω to V_{CC} for proper operation.
7. V_{th}, V_{IH}, V_{IL}, and V_{ISE} parameters must be complied with simultaneously.
8. V_{th} is applied to the complementary input when operating in single−ended mode.
9. V_{IHD}, V_{ILD}, V_{ID}, and V_{CMR} parameters must be complied with simultaneously.
10. V_{CMR} min varies 1:1 with GND, V_{CMR} max varies 1:1 with V_{CC}. The V_{CMR} range is referenced to the most positive side of the differential input signal.

Table 6. AC CHARACTERISTICS V_{CC} = 2.375 V to 3.6 V, GND = 0 V, T_A = −40°C to 85°C (Note 11)

Symbol	Characteristic		Min	Typ	Max	Unit
f_{MAX}	Maximum Input Clock Frequency	$V_{OUT} \geq 250$ mV $V_{OUT} \geq 200$ mV	7.0 8.5			GHz
$f_{DATAMAX}$	Maximum Operating Data Rate (PRBS23)		10			Gbps
V_{OUTPP}	Output Voltage Amplitude (@ $V_{INPPmin}$) (See Figures 3 and 10, Note 12)	$f_{in} \leq 8.5$ GHz	200	400		mV
t_{PLH}, t_{PHL}	Propagation Delay to Differential Outputs, @ 1GHz, Measured at Differential Cross−point	INn/$\overline{INn}$ to Qn/$\overline{Qn}$ SELn to Qn/$\overline{Qn}$	110	150	180	ps
t_{PLH} TC	Propagation Delay Temperature Coefficient			50		Δfs/°C
t_{SKEW}	Output−to−Output Skew (within device) (Note 13) Device−to−Device Skew ($t_{pdmax} - t_{pdmin}$)				10 20	ps
t_{DC}	Output Clock Duty Cycle (Reference Duty Cycle = 50%)	$f_{in} \leq 8.5$GHz	45	50	55	%
t_{jitter}	RJ − Output Random Jitter (Note 14) DJ − Deterministic Jitter (Note 15)	$f_{in} \leq 8.5$ GHz ≤ 10 Gbps		0.2	0.5 10	ps RMS ps pk−pk
V_{INPP}	Input Voltage Swing (Differential Configuration) (Note 16)		100		1200	mV
$t_{r,}$ t_f	Output Rise/Fall Times @ 1 GHz (20% − 80%),	Q, $\overline{Q}$	25	30	50	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

11. Measured using a 400 mV source, 50% duty cycle clock source. All output loading with external 50 Ω to V_{CC}. Input edge rates ≥ 40 ps (20% − 80%).
12. Output voltage swing is a single−ended measurement operating in differential mode.
13. Skew is measured between outputs under identical transitions and conditions. Duty cycle skew is defined only for differential operation when the delays are measured from cross−point of the inputs to the cross−point of the outputs.
14. Additive RMS jitter with 50% duty cycle clock signal.
15. Additive Peak−to−Peak data dependent jitter with input NRZ data at PRBS23.
16. Input voltage swing is a single−ended measurement operating in differential mode.

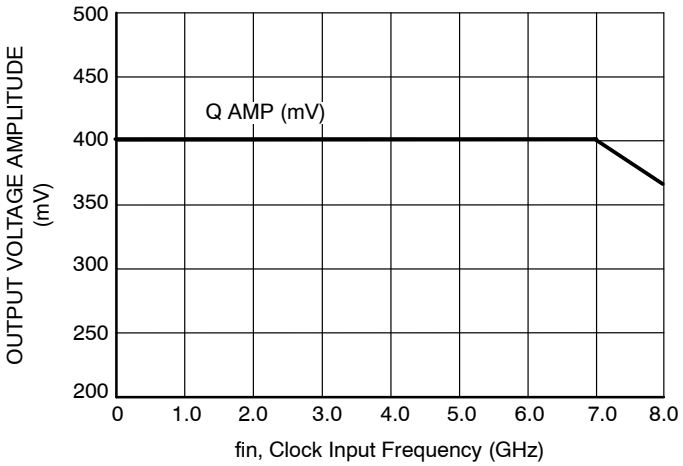


Figure 3. CLOCK Output Voltage Amplitude (V_{OUTPP}) vs. Input Frequency (f_{in}) at Ambient Temperature (Typ)

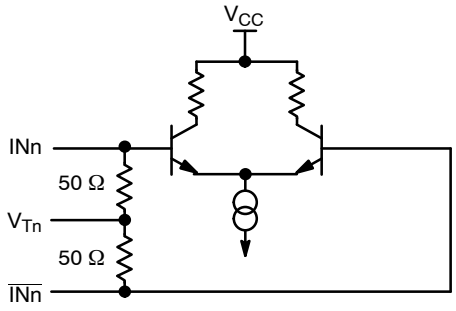


Figure 4. Input Structure

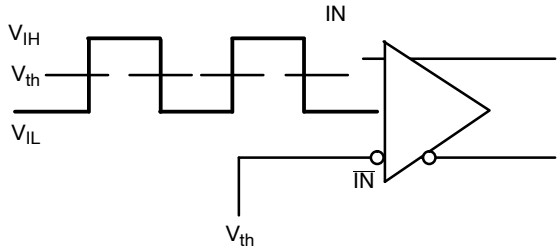


Figure 5. Differential Input Driven Single−Ended

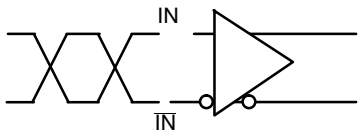


Figure 6. Differential Inputs Driven Differentially

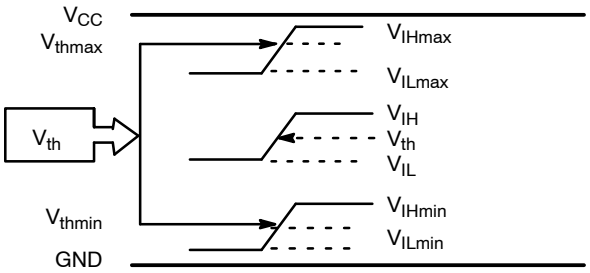


Figure 7. V_{th} Diagram

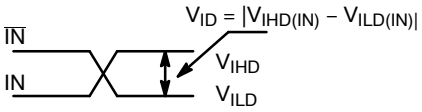


Figure 8. Differential Inputs Driven Differentially

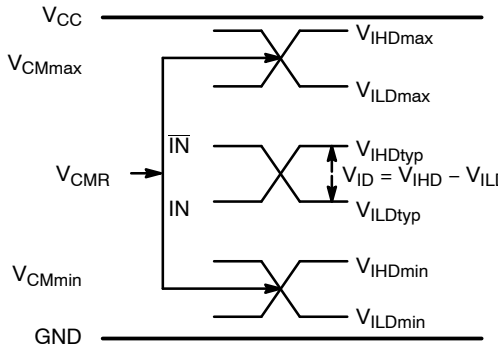


Figure 9. V_{CMR} Diagram

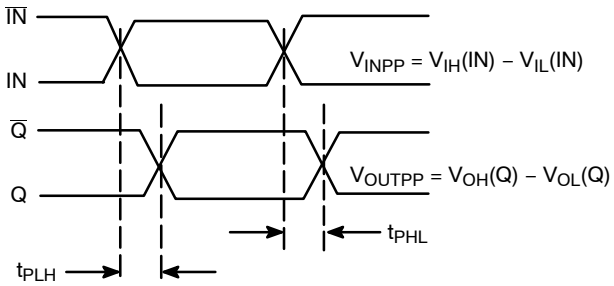


Figure 10. AC Reference Measurement

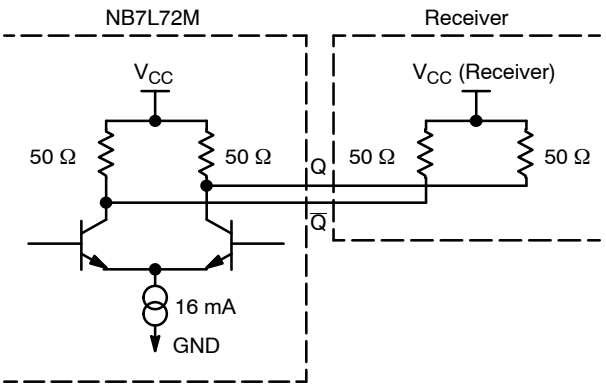


Figure 11. Typical CML Output Structure and Termination

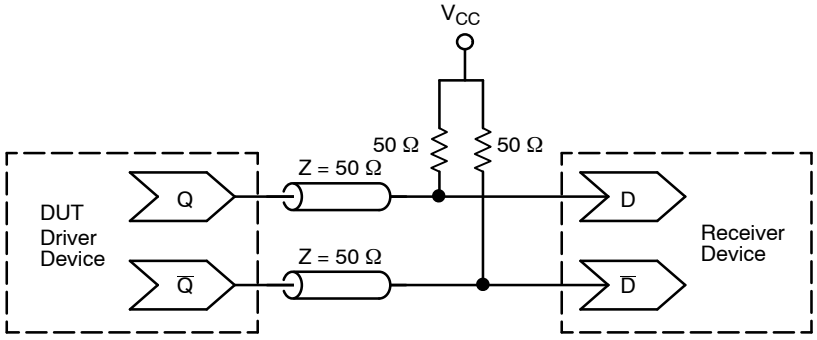


Figure 12. Typical Termination for CML Output Driver and Device Evaluation

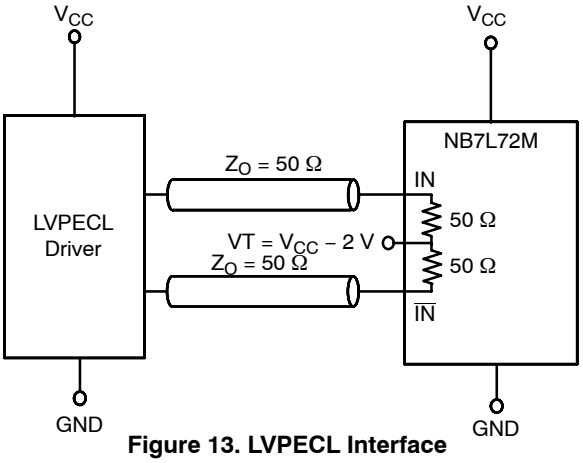


Figure 13. LVPECL Interface

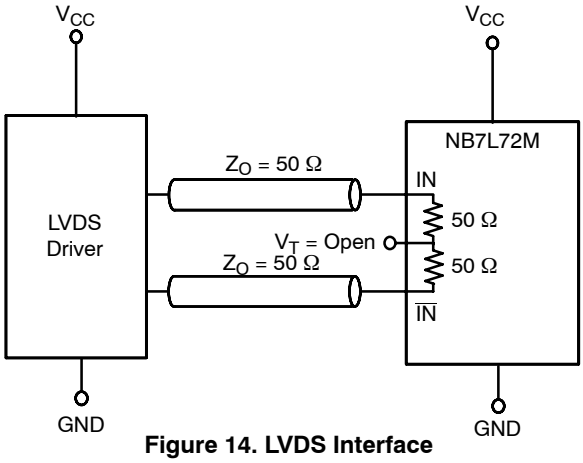


Figure 14. LVDS Interface

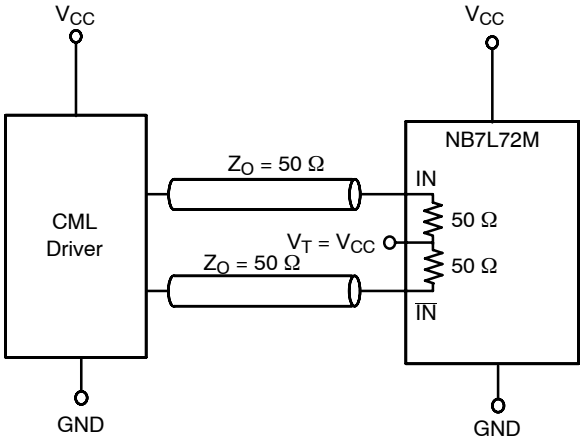


Figure 15. Standard 50 Ω Load CML Interface

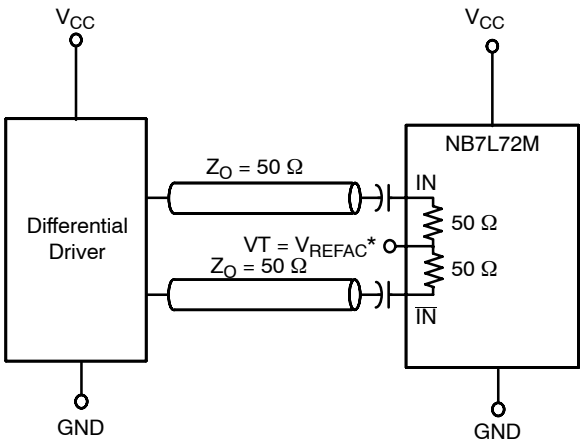


Figure 16. Capacitor−Coupled Differential Interface (VT Connected to External V_{REFAC})

*V_{REFAC} bypassed to ground with a 0.01 μF capacitor

ORDERING INFORMATION

Device	Package	Shipping†
NB7L72MMNG	QFN16 (Pb−free)	123 Units / Tube
NB7L72MMNHTBG	QFN16 (Pb−free)	100 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

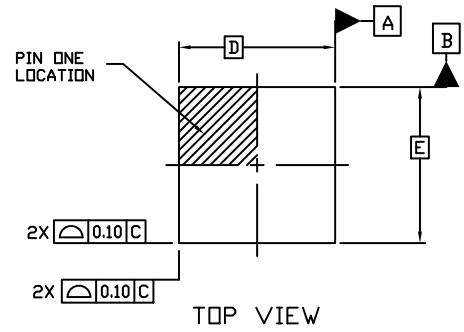
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MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

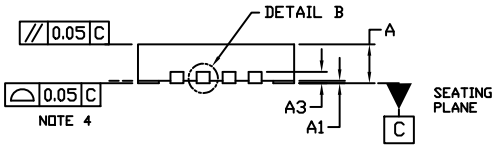
QFN16 3x3, 0.5P
CASE 485G
ISSUE G

DATE 08 OCT 2021

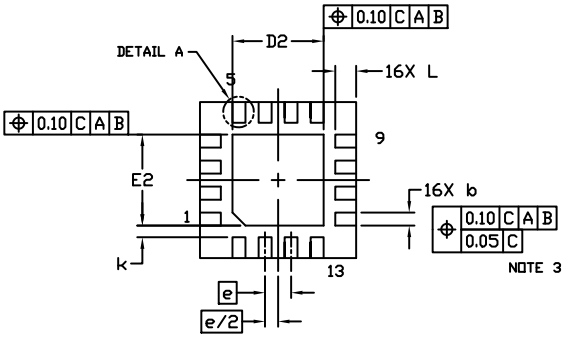
SCALE 2:1



TOP VIEW

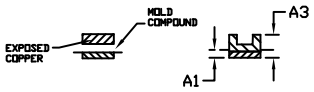


SIDE VIEW

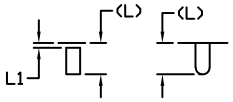


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.



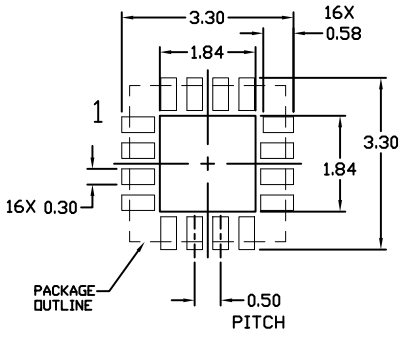
DETAIL B
ALTERNATE CONSTRUCTIONS



DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	0.03	0.05
A3		0.20 REF	
b	0.18	0.24	0.30
D		3.00 BSC	
D2	1.65	1.75	1.85
E		3.00 BSC	
E2	1.65	1.75	1.85
e		0.50 BSC	
k		0.18 TYP	
L	0.30	0.40	0.50
L1	0.00	0.08	0.15

MOUNTING FOOTPRINT



GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**QFN16 3X3, 0.5P**	**PAGE 1 OF 1**

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