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# NOII5SM1300A

# IBIS5 1.3 Megapixel CMOS Image Sensor

ON Semiconductor®

http://onsemi.com

### Features

- 1280 x 1024 Active Pixels
- 6.7 μm x 6.7 μm Square Pixels
- 2/3" Optical Format
- Global and Rolling Shutter
- Master Clock: 40 MHz
- 27 fps (1280 x 1024) and 106 fps (640 x 480)
- On-chip 10-bit ADCs
- Serial Peripheral Interface (SPI)
- Windowing (ROI)
- Sub-sampling: 1:2 Mode
- Supply Voltage
  - Analog: 3.0 V to 4.5 V
  - Digital: 3.3 V
  - I/O: 3.3 V
- Power Consumption: 200 mW
- −30°C to +65°C Operating Temperature Range
- 84-pin LCC Package
- These Devices are Pb−Free and are RoHS Compliant

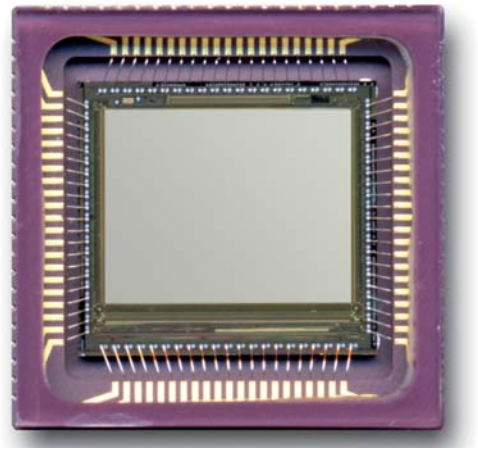


**Figure 1. IBIS5−1300 Photo**

### Applications

- Machine Vision
- Inspection
- Robotics
- Traffic Monitoring

### Description

The IBIS5-1300 is a solid state CMOS image sensor that integrates the functionality of complete analog image acquisition, digitizer, and digital signal processing system on a single chip. This 1.3-mega pixel (1280 x 1024) CMOS active pixel sensor dedicated to industrial vision applications features both rolling and snapshot (or global) shutter. Full frame readout time is 36 ms (max. 27.5 fps), and readout speed are boosted by windowed region of interest (ROI) readout. Another feature includes the double and multiples slope functionality to capture high dynamic range scenes. The sensor is available in a monochrome version or Bayer (RGB) patterned color filter array.

User programmable row and column start/stop positions allow windowing down to a 2x1 pixel window for digital zoom. Sub sampling or viewfinder mode reduces resolution while maintaining the constant field of view and an increased frame rate. An on-chip analog signal pipeline processes the analog video output of the pixel array. Double sampling (DS) eliminates the fixed pattern noise. The programmable gain and offset amplifier maps the signal swing to the ADC input range. A 10-bit ADC converts the analog data to a 10-bit digital word stream. The sensor uses a 3-wire serial peripheral interface (SPI), or a 16-bit parallel interface. It operates with a 3.3 V power supply and requires only one master clock for operation up to 40 MHz. It is housed in an 84-pin ceramic LCC package.

### ORDERING INFORMATION

| Marketing Part Number | Description | Package | Device Status |
|---|---|---|---|
| NOII5SM1300A-QDC | Mono with glass | 84−pin LCC | End−of−Life (EOL)<br>Last Time Buy<br>PCN Close date:<br>**October 29, 2011** |
| NOII5SM1300A-QWC | Mono without glass | | |
| NOII5SC1300A-QDC | Color with glass | | |
| NOII5FM1300A-QDC | Mono on thicker epitaxial layer, with glass | | |

NOTE: See Ordering Code Information on page 33 for more information.

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## SPECIFICATIONS

### Key Specifications

**Table 1. GENERAL SPECIFICATIONS**

| Parameter | Specifications |
|---|---|
| Active pixels | 1280 (H) x 1024 (V) |
| Pixel size | 6.7 μm x 6.7 μm |
| Master Clock | 40 MHz |
| Shutter type | Global and rolling shutter |
| Frame rate | 27 fps at full resolution |
| Windowing (ROI) | Randomly programmable ROI read out. Implemented as scanning of lines or columns from an uploaded position |
| ADC resolution | 10-bit, on-chip |
| Extended dynamic range | Global shutter: Up to 4 slopes<br>Rolling shutter: Double slope |
| Power dissipation | 200 mW |

**Table 2. ELECTRO OPTICAL SPECIFICATIONS**

| Parameter | Specifications |
|---|---|
| Sensitivity | 8.4 V/lux.s at 650 nm |
| Full Well Charge | 62500 $e^-$ |
| Temporal Noise | 2.5 LSB10 |
| Parasitic light sensitivity | 3% |
| Dark noise | 21 $e^-$ |
| Signal to Noise Ratio | 64 dB |
| Fixed pattern noise (FPN) | 4.5 LSB10 |
| Dark signal | 5.5 LSB10/sec at 30°C |

**Table 3. RECOMMENDED OPERATING RATINGS**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_J$ (Note 2) | Operating temperature range | −30 | +65 | °C |

**Table 4. ABSOLUTE MAXIMUM RATINGS** (Note 1)

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| ABS<br>(3.0 V to 3.3 V supply group) | ABS rating for 3.0 V and 3.3 V supply group | −0.5 | 4.3 | V |
| ABS<br>(4.5 V supply group) | ABS rating for 4.5 V supply group | −0.5 | ($V_{DD}$ + 0.5) | V |
| $T_S$ (Note 1) | ABS storage temperature range | −30 | 150 | °C |
| | ABS storage humidity range | 5 | 90 | %RH |
| %RH | Humidity (Relative) | - | 85% at 85°C | |
| Electrostatic discharge (ESD)<br>(Note 3) | Human Body Model (HBM) | (Note 4) | | V |
| | Charged Device Model (CDM) | | | |
| LU (Note 3) | Latch-up | (Note 5) | | mA |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Absolute maximum ratings are limits beyond which damage may occur. Long term exposure toward the maximum storage temperature accelerates color filter degradation.
2. Operating ratings are conditions in which operation of the device is intended to be functional.
3. ON Semiconductor recommends that customers become familiar with, and follow the procedures in JEDEC Standard JESD625−A. Refer to Application Note AN52561.
4. The IBIS5−1300 complies with JESD22−A114 HBM Class 0 and JESD22−C101 Class I. It is recommended that extreme care be taken while handling these devices to avoid damages due to ESD event. Refer to Application Note AN52561.
5. The IBIS5−1300 does not have latch−up protection.

## Electrical Specifications

*Recommended Operating Conditions*

**Table 5. RECOMMENDED OPERATING CONDITIONS**

| Parameter | Description | Typical Currents | Peak Currents | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| VDDH | Voltage on HOLD switches. | 0.047 mA | 100 mA | +3.3 | +4.5 | +4.5 | V |
| VDDR_LEFT | Highest reset voltage. | 0.050 mA | 100 mA | +3.3 | +4.5 | +4.5 | V |
| VDDC | Pixel core voltage. | 0.052 mA | 100 mA | +2.5 | +3.0 | +3.3 | V |
| VDDA | Analog supply voltage of the image core. | 19.265 mA | N/A | +3.0 | +3.3 | +3.6 | V |
| VDDD | Digital supply voltage of the image core. | 5.265 mA | N/A | +3.0 | +3.3 | +3.6 | V |
| IDDA_ADC | Analog supply of ADC | 34.5 mA | N/A | N/A | N/A | N/A | mA |
| IDDD_ADC | Digital supply of ADC | 10.5 mA | N/A | N/A | N/A | N/A | mA |
| $T_A$ | Commercial operating temperature. | N/A | N/A | −30 | 30 | 65 | °C |

All parameters are characterized for DC conditions after thermal equilibrium is established.

Always tie unused inputs to an appropriate logic level, for example, either VDD or GND.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, take normal precautions to avoid application of any voltages higher than the maximum rated voltages to this high impedance circuit.

*DC Electrical Characteristics*

**Table 6. DC ELECTRICAL CHARACTERISTICS**

| Parameter | Characteristic | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{IH}$ | Input high voltage | | 2.1 | – | V |
| $V_{IL}$ | Input low voltage | | – | 0.6 | V |
| $I_{IN}$ | Input leakage current | $V_{IN}$= VDD or GND | –10 | +10 | μA |
| $V_{OH}$ | Output high voltage | VDD = min; $I_{OH}$ = –100 μA | 2.2 | – | V |
| $V_{OL}$ | Output low voltage | VDD = min; $I_{OH}$ = 100 μA | | 0.5 | V |
| $I_{DD}$ | Maximum operating current | System clock ≤ 40 MHz | 40 | 60 | mA |

## ARCHITECTURE AND OPERATION

This section presents detailed information about the most important sensor blocks

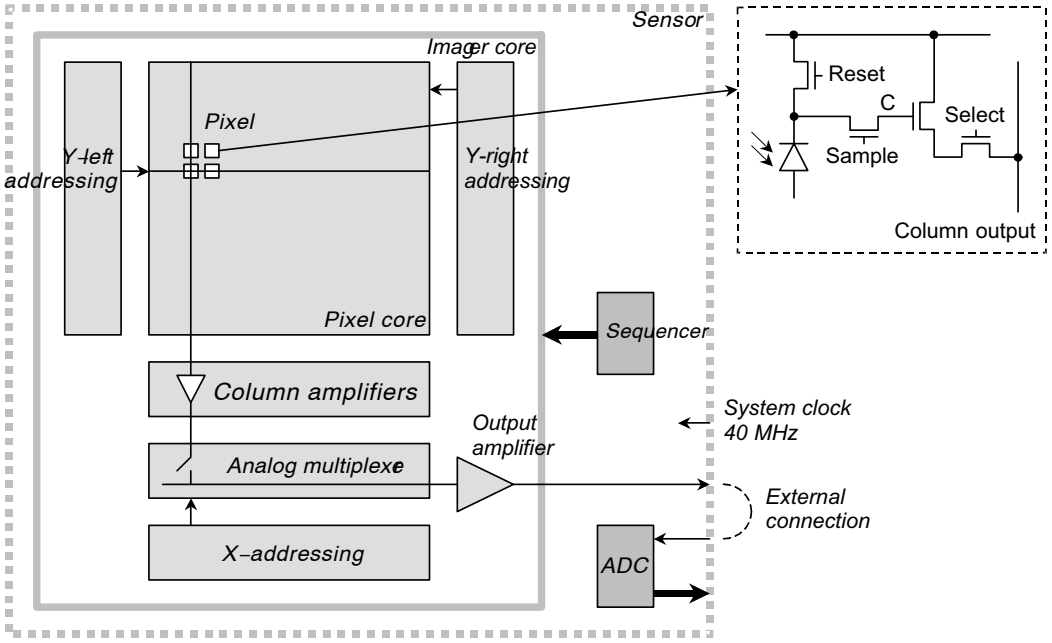



**Figure 2. Block Diagram of IBIS5−1300 Image Sensor**

### Floor Plan

Figure 2 shows the architecture of the IBIS5-1300 image sensor. It consists basically of a pixel array, one X- and two Y-addressing registers for the readout in X- and Y-direction, column amplifiers that correct for the fixed pattern noise, an analog multiplexer, and an analog output amplifier

Use the left Y-addressing register for readout operation. Use the right Y-addressing register for reset of pixel rows. In multiple slope synchronous shutter mode, the right Y-addressing register resets the whole pixel core with a lowered reset voltage. In rolling curtain shutter mode, use the right Y-addressing register for the reset pointer in single and double slope operation to reset one pixel row.

The on-chip sequencer generates most of the signals for the image core. Some basic signals (such as start/stop integration, line and frame sync signals) are generated externally.

A 10-bit ADC is implemented on chip but electrically isolated from the image core. You must route the analog pixel output to the analog ADC input on the outside.

## Pixel

A description of the pixel architecture and the color filter array follows.

*Architecture*

The pixel architecture used in the IBIS5-1300 is a 4-transistor pixel as shown in Figure 3. Implement the pixel using the high fill factor technique. The 4T-pixel features a snapshot shutter but can also emulate the 3T-pixel by continuously closing sampling switch M2. Using M2 as a global sample transistor for all pixels enables the snapshot shutter mode. Due to this pixel architecture, integration during read out is not possible in synchronous shutter mode.

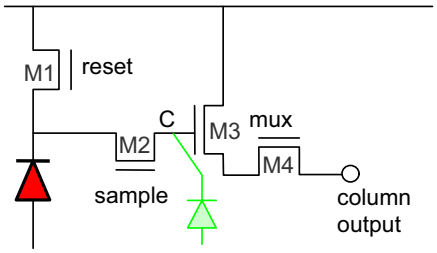



**Figure 3. 4T Pixel Architecture**

*Color Filter Array*

The IBIS5-1300 is also processed with a Bayer RGB color pattern. Pixel (0,0) is a green filter and is situated on a green-blue row. Green1 and Green2 have a slightly different spectral response due to cross talk from neighboring pixels. Green1 pixels are located on a blue-green row, green2 pixels are located on a green-red row. Figure 5 shows the response of the color filter array as function of the wavelength. Note that this response curve includes the optical cross talk of the pixels.

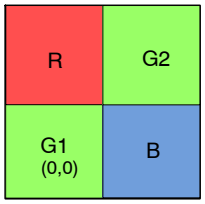



**Figure 4. Color Filter Arrangement of Pixels**

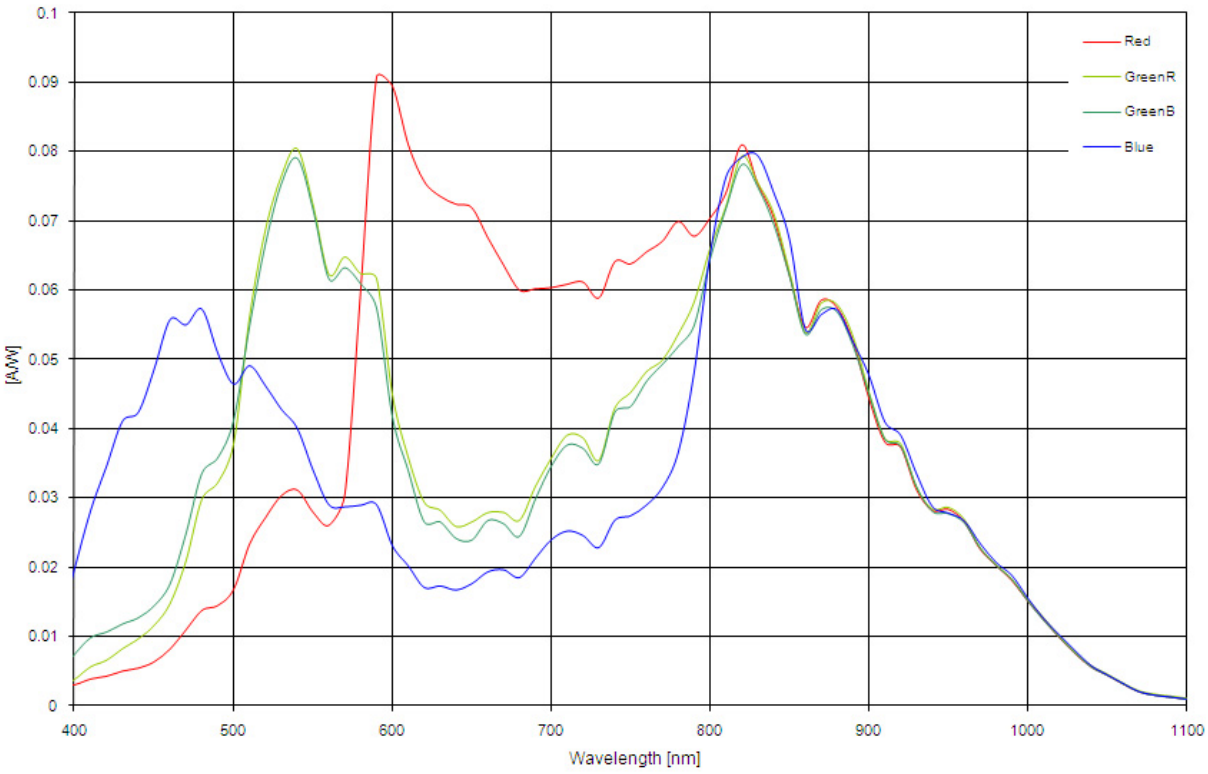



**Figure 5. Spectral Response for IBIS5−1300 Color**

*Spectral Response Curve*

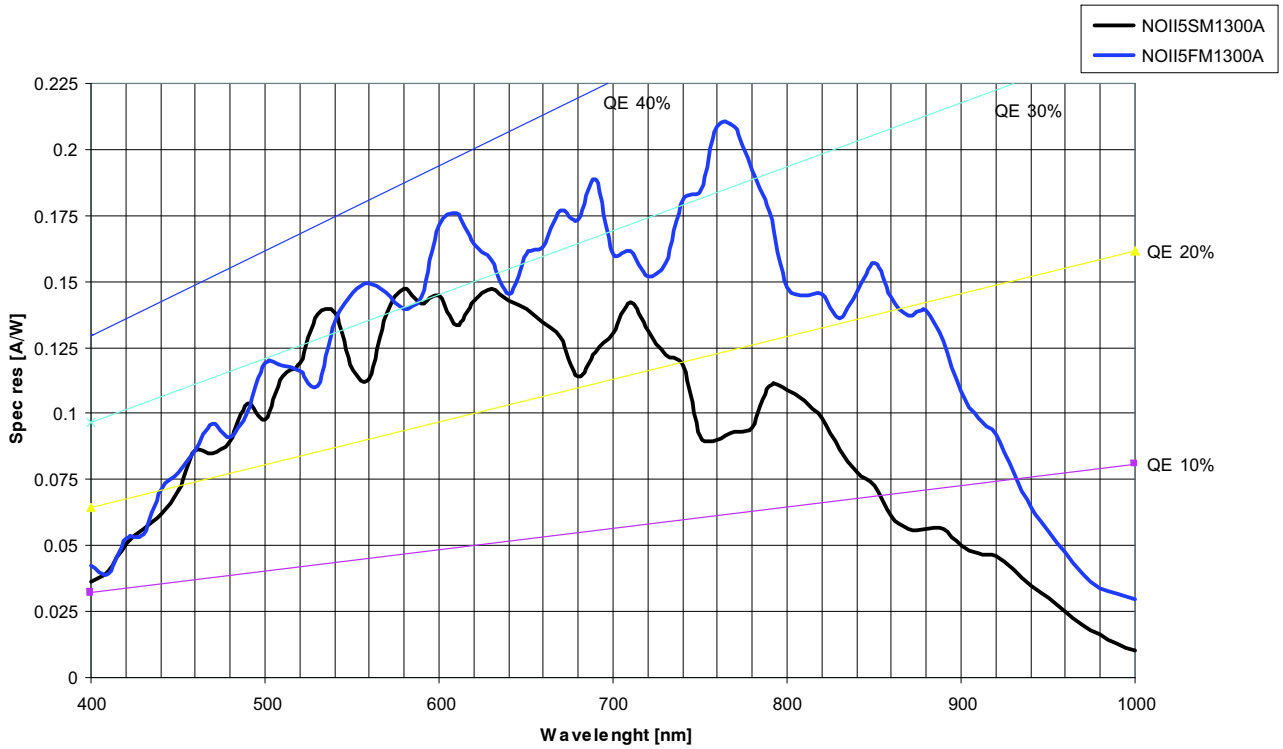



**Figure 6. Spectral Response Curve**

Figure 6 shows the spectral response characteristic for the NOII5SM1300A and the NOII5FM1300A.

The curve is measured directly on the pixels. It includes effects of non-sensitive areas in the pixel, for example, interconnection lines. The sensor is light sensitive between 400 and 1000 nm. The peak QE x FF is 30%, approximately around 650 nm. In view of a fill factor of 40%, the QE is thus close to 75% between 500 and 700 nm. The NOII5FM1300A has superior response in the NIR region (700-900 nm).

*Electro-voltaic Response Curve*

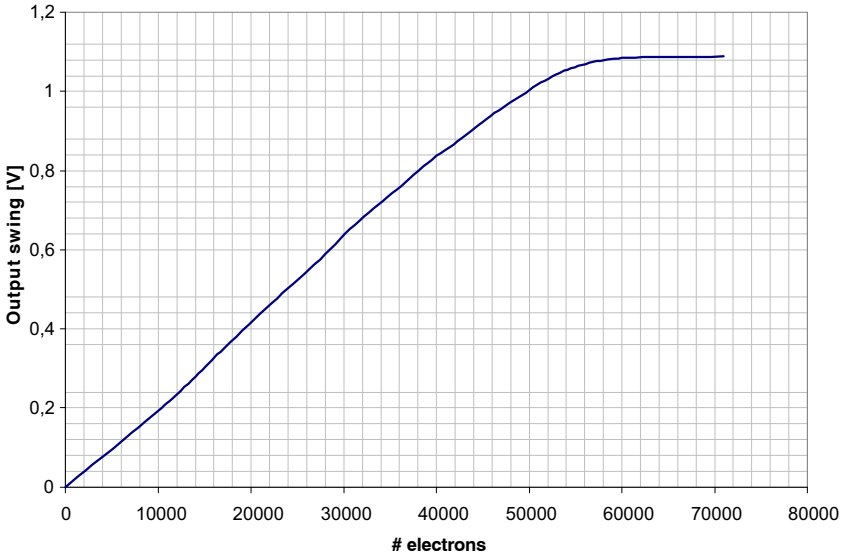



**Figure 7. Electro−Voltaic Response Curve**

Figure 7 shows the pixel response curve in linear response mode. This curve is the relation between the electrons detected in the pixel and the output signal. The resulting voltage-electron curve is independent of any parameters (integration time, and others). The voltage to electrons conversion gain is 17.6 μV/electron.

*NOII5FM1300A:*

The NOII5FM1300A is processed on a thicker epitaxial silicon featuring higher sensitivity in the NIR (Near Infra Red) wavelengths (700–900 nm). The spectral response curves, highlighting the difference between IBIS5-1300 using the standard process and thicker epitaxial layer process are shown in Figure 6 on page 7. Various machine vision applications use light sources in the NIR, hence the NOII5FM1300A sensor has a significant sensitivity advantage in the NIR domain.

A drawback of the thicker epitaxial layer is a slight performance decrease in MTF (Modular Transfer Function or electrical pixel to pixel cross-talk) as indicated in Table 7.

**Table 7. MTF COMPARISON**

| Direction | Wavelength | NOII5SM1300A | NOII5FM1300A |
|---|---|---|---|
| Horizontal | 600 | 0.58 | 0.37 |
| Horizontal | 700 | | 0.18 |
| Horizontal | 800 | | 0.16 |
| Horizontal | 900 | | 0.07 |
| Vertical | 600 | 0.53 | 0.26 |
| Vertical | 700 | | 0.16 |
| Vertical | 800 | | 0.13 |
| Vertical | 900 | | 0.11 |

The resulting image sharpness is hardly affected by this decreased MTF value. Both IBIS5-1300 versions are fully pin compatible and have identical timing and biasing.

### Image Core Operation

*Image Core Operation and Signalling*

Figure 8 is a functional representation of the image core without sub-sampling and column/row swapping circuits. Most of the signals involved are not available from the outside because they are generated by the X-sequencer and SS-sequencer blocks.

The integration of the pixels is controlled by internal signals such as reset, sample, and hold which are generated by the on-chip SS-sequencer that is controlled with the external signals SS_START and SS_STOP. Reading out the pixel array starts by applying a Y_START together with a Y_CLOCK signal; internally this is followed by a calibration sequence to calibrate the output amplifiers (during the row blanking time). Signals necessary to do this calibration are generated by the on-chip X-sequencer. This calibration sequence takes typically 3.5 μs and is necessary to remove 'Fixed Pattern Noise' of the pixels and of the column amplifiers themselves by means of a double sampling technique. After the row blanking time, the pixels are fed to the output amplifier. The pixel rate is equal to the SYS_CLOCK frequency.

*Image Core Supply Considerations*

The image sensor has several supply voltages:

VDDH is the voltage that controls the sample switches. Do not apply a higher voltage than this to the chip.

The VDDR_LEFT voltage is the highest (nominal) reset voltage of the pixel core.

The VDDR_RIGHT voltage is generated from the VDDR_LEFT voltage using a circuit that is programmed with the KNEEPOINT_LSB/MSB bits in the sequencer register (see also Pixel reset knee−point for multiple slope operation (bits 8, 9, and 10) on page 17). You can disconnect the VDDR_RIGHT pin from the circuit and apply an external voltage to supply the multiple slope reset voltage by setting the VDDR_RIGHT_EXT bit in the SEQUENCER register. When no external voltage is applied (recommended), connect the VDDR_RIGHT pin to a capacitor (recommended value = 1 μF). VDDC is the pixel core supply. VDDA is the image core and periphery analog supply. VDDD is the image core and periphery digital supply .

Note that the IBIS5-1300 image sensor has no on-chip power rejection circuitry. As a consequence all variations on the analog supply voltages can contribute to random variations (noise) on the analog pixel signal, which is seen as random noise in the image. During the camera design, take precautions to supply the sensor with very stable supply voltages to avoid this additional noise. The pixel array (VDDR_LEFT, VDDH and VDDC) analog supplies are especially vulnerable to this.

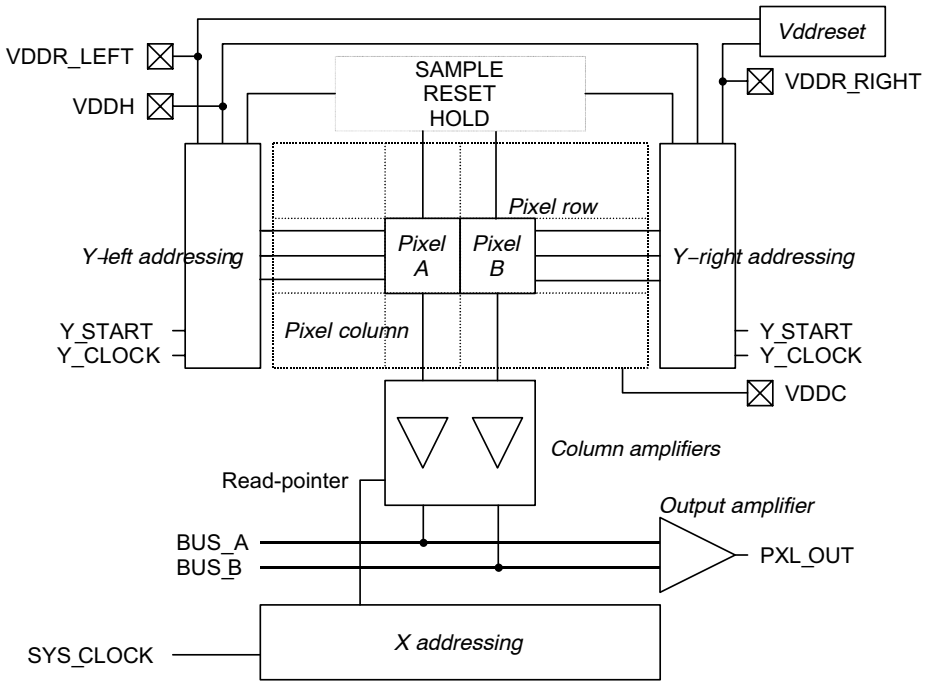



**Figure 8. Image Core**

*Global Shutter Supply Considerations*

The recommended supply voltage settings listed in Table 8 are used when the sensor is in global shutter mode only.

**Table 8. GLOBAL SHUTTER RECOMMENDED SUPPLY SETTINGS**

| Parameter | Description | Typ | Units |
|---|---|---|---|
| VDDH | Voltage on HOLD switches. | +4.5 | V |
| VDDR_LEFT | Highest reset voltage. | +4.5 | V |
| VDDC | Pixel core voltage. | +3.3 | V |
| VDDA | Analog supply voltage of the image core. | +3.3 | V |
| VDDD | Digital supply voltage of the image core. | +3.3 | V |
| GNDA | Analog ground. | 0 | V |
| GNDD | Digital ground. | 0 | V |
| GND_AB | Anti-blooming ground. | 0 | V |

*Dual Shutter Supply Considerations*

If you analyze the supply settings listed in Table 8, you can see some fixed column non-uniformities (FPN) when operating in rolling shutter mode. If a dual shutter mode (both rolling and global shutter) is required during operation, you must apply the supply settings listed in Table 9 to achieve the best possible image quality.

**Table 9. DUAL SHUTTER RECOMMENDED SUPPLY SETTINGS**

| Parameter | Description | Typ | Units |
|---|---|---|---|
| VDDH | Voltage on HOLD switches. | +4.5 | V |
| VDDR_LEFT | Highest reset voltage. | +4.5 | V |
| VDDC | Pixel core voltage. | +3.0 | V |
| VDDA | Analog supply voltage of the image core. | +3.3 | V |
| VDDD | Digital supply voltage of the image core. | +3.3 | V |
| GNDA | Analog ground. | 0 | V |
| GNDD | Digital ground. | 0 | V |
| GND_AB | Anti-blooming ground. | 0 | V |

*Image Core Biasing Signals*

Table 10 summarizes the biasing signals required to drive the IBIS5-1300. For optimization on speed and power dissipation of all internal blocks, several biasing resistors are needed.

Each biasing signal determines the operation of a corresponding module in the sense that it controls the speed and power dissipation. The tolerance on the DC-level of the bias levels can vary ±150 mV due to process variations.

**Table 10. OVERVIEW OF BIAS SIGNALS**

| Signal | Comment | Related module | DC-Level |
|---|---|---|---|
| DEC_CMD | Connect to VDDA with R = 51 kΩ and decouple to GNDA with C = 100 nF. | Decoder stage. | 1.0 V |
| DAC_VHIGH | Connect to VDDA with R = 0 Ω. | High level of DAC. | 3.3 V |
| DAC_VLOW | Connect to GNDA with R = 0 Ω. | Low level of DAC. | 0.0 V |
| AMP_CMD | Connect to VDDA with R = 51 kΩ and decouple to GNDA with C = 100 nF. | Output amplifier stage. | 1.2 V |
| COL_CMD | Connect to VDDA with R = 51 kΩ and decouple to GNDA with C = 100 nF. | Columns amplifiers stage. | 1.0 V |
| PC_CMD | Connect to VDDA with R = 22 kΩ and decouple to GNDA with C = 100 nF. | Pre-charge of column busses. | 1.17 V |
| ADC_CMD | Connect to VDDA with R = 51 kΩ and decouple to GNDA with C = 100 nF. | Analog stage of ADC. | 1.0 V |
| ADC_VHIGH | Connect to VDDA with R = 230 Ω and decouple to GNDA with C = 100 nF. | High level of ADC. | 2.7 V |
| ADC_VLOW | Connect to GNDA with R = 410 Ω and decouple to GNDA with C = 100 nF. | Low level of ADC. | 1.2 V |

### X−Addressing

Because of the high pixel rate, the X-shift register selects two columns at a time for readout, so it runs at half the system clock speed. All even columns are connected to bus A; all odd columns to bus B. In the output amplifier, bus A and bus B are combined into one stream of pixel data at system clock speed.

At the end of the row blanking time, the X_SYNC switch is closed while all other switches are open and the decoder output is fed to the register. The decoder loads a logical one in one of the registers and a logical zero in the rest. This defines the starting point of the window in the X direction. As soon as the X_SYNC signal is released, the register starts shifting from the start position.

When no sub-sampling is required, X_SUB is inactive. The pointer in the shift-register moves one bit at a time.

When sub-sampling is enabled, X_SUB is activated. The shift register moves two bits at a time. Taking into account that every register selects two columns, hence two pixels sub-sampling results in the pattern ‘XXOOXXOO’ when eight pixels are considered. Suppose the columns are numbered from left to right starting with 0 (zero) and sub-sampling is enabled:

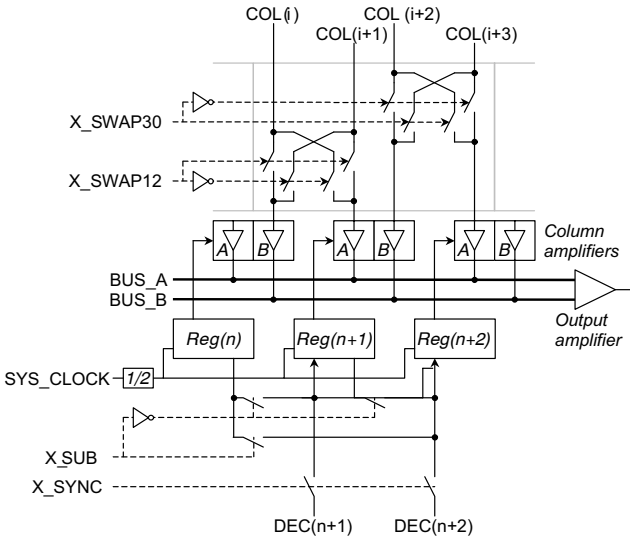



**Figure 9. Column Structure**

If columns 1 and 2, 5 and 6, 9 and 10 … are swapped using the SWAP_12 switches, a normal sub-sampling pattern of ‘XOXOXOXO’ is obtained.

If columns 3 and 4, 7 and 8, 11 and 12 … are swapped using the SWAP_30 switches, the pattern is ‘OXOXOXOX’.

If both the SWAP_12 and SWAP_30 switches are closed, pattern ‘OOXXOOXX’ is obtained.

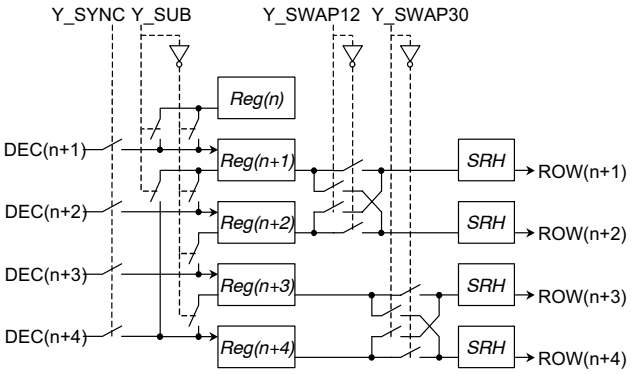



**Figure 10. Row Structure**

Because every register addresses two columns at a time, the addressable pixels range in sub-sample mode is from zero to half the maximum number of pixels in a row (only even values). For instance: 0, 2, 4, 6, 8… 638.

**Table 11. X–SUB-SAMPLING PATTERNS**

| X_SUB | X_SWAP12 | X_SWAP30 | Sub-Sample Pattern |
|---|---|---|---|
| 0 | 0 | 0 | XXXXXXXX |
| 1 | 0 | 0 | XXOOXXOO |
| 1 | 1 | 0 | XOXOXOXO |
| 1 | 0 | 1 | OXOXOXOX |
| 1 | 1 | 1 | OOXXOOXX |

### Y−Addressing

For symmetry reasons, the sub-sampling modes in the Y-direction are the same as in X-direction.

**Table 12. Y–SUB-SAMPLING PATTERNS**

| Y_SUB | Y_SWAP12 | Y_SWAP30 | Sub-Sample Pattern |
|---|---|---|---|
| 0 | 0 | 0 | XXXXXXXX |
| 1 | 0 | 0 | XXOOXXOO |
| 1 | 1 | 0 | XOXOXOXO |
| 1 | 0 | 1 | OXOXOXOX |
| 1 | 1 | 1 | OOXXOOXX |

In normal mode, the pointer for the pixel row is shifted one at a time.

When sub-sampling is enabled, Y_SYNC is activated. The Y-shift register shifts 2 succeeding bits and skips the 2 next bits. This results in pattern ‘XXOOXXOO’.

Activating Y_SWAP12 results in pattern ‘XOXOXOXO’.

Activating Y_SWAP30 results in pattern ‘OXOXOXOX’.

Activating both Y_SWAP12 and Y_SWAP30 results in pattern ‘OOXXOOXX’.

The addressable pixel range when Y-sub sampling is enabled is: 0–1, 4–5, 8–9, 12–13, … 1020–1021

### Output Amplifier

*Architecture and Settings*

The output amplifier stage is user programmable for gain and offset level. Gain is controlled by 4-bit wide word; offset by a 7-bit wide word. Gain settings are on an exponential scale. Offset is controlled by a 7-bit wide DAC, which selects the offset voltage between two reference voltages (DAC_VHIGH and DAC_VLOW) on a linear scale.

The amplifier is designed to match the specifications of the imager array output. This signal has a data rate of 40 MHz. The output impedance of the amplifier is 260 Ohms.

At unity gain and with a mid-range offset value, the amplifier outputs a signal in between 1.59 V (light) and 2.70 V (dark). This analog range must fit to the input range of the ADC, external or internal. The output swing in unity gain is approximately 1.11 V and it is maximum 1.78 V at the highest gain settings. So, the effective signal range is between 1.17 V and 2.95 V, depending on the gain and offset settings of the amplifier.

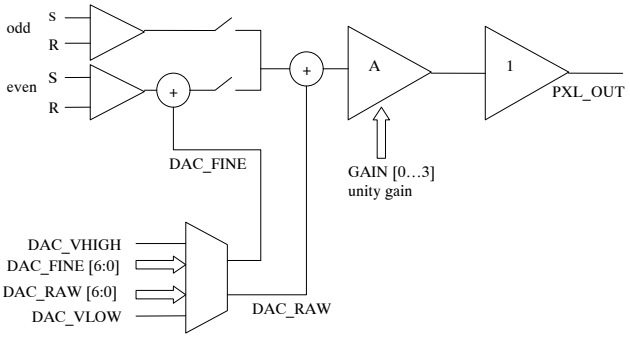



**Figure 11. Output Structure**

Figure 11 shows the architecture of the output amplifier. The odd and even column amplifiers sample both pixel and reset value to perform a double sampling FPN correction. You can adjust two different offsets using the on-chip DAC (7 bit): DAC_FINE and DAC_RAW. DAC_FINE is used to tune the difference between odd and even columns; DAC_RAW is used to add a common (both even and odd columns) to the FPN corrected pixel value. This pixel value is fed to the first amplifier stage which has an adjustable gain, controlled by a 4-bit word ('GAIN [0…3]').

After this, a unity feedback amplifier buffers the signal and the signal leaves the chip. This second amplifier stage determines the maximal readout speed, that is, the bandwidth and the slew rate of the output signal. The whole amplifier chain is designed for a data rate of 40 Mpix/s (at 20 pF).

The analog output of the sensor is not designed to drive very large loads on the PCB. Therefore, it is advised that the PXL_OUT is connected to the ADC_IN right below the sensor in the top layer with a thick track. It is better not to have vias on this trace. If there is a socket being used, then it is advised that we buffer the PXL_OUT close to the sensor output pin and then take the signal to the ADC_IN.

*Output Amplifier Gain Control*

The output amplifier gain is controlled by a 4-bit word set in the AMPLIFIER register (see section Amplifier Register (6:0) on page 19). An overview of the gain settings is given in Table 13.

**Table 13. OVERVIEW GAIN SETTINGS**

| Bits | DC Gain | Bits | DC Gain |
|---|---|---|---|
| 0000 | 1.37 | 1000 | 6.25 |
| 0001 | 1.62 | 1001 | 7.89 |
| 0010 | 1.96 | 1010 | 9.21 |
| 0011 | 2.33 | 1011 | 11.00 |
| 0100 | 2.76 | 1100 | 11.37 |
| 0101 | 3.50 | 1101 | 11.84 |
| 0110 | 4.25 | 1110 | 12.32 |
| 0111 | 5.20 | 1111 | 12.42 |

*Setting of the DAC Reference Voltage*

In the output amplifier, the offset is trimmed by loading registers DACRAW_REG and DACFINE_REG. DAC_RAW is used to adjust the offset of the output amplifier and DAC_FINE is used to tune the offset between the even and odd columns. These registers are inputs for two DACs (see Figure 12) that operate on the same resistor that is connected between pins DAC_VHIGH and DAC_VLOW. The range of the DAC is defined using a resistive division with $R_{VHIGH}$, $R_{DAC}$ and $R_{VLOW}$.

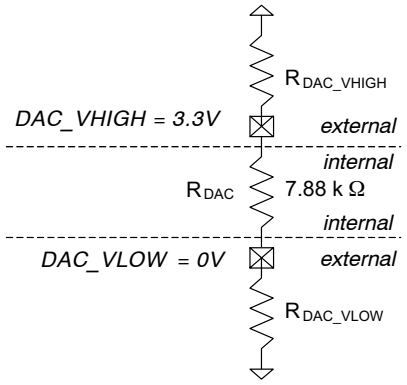



**Figure 12. Internal and External ADC Connections**

The internal resistor $R_{DAC}$ has a value of approximately 7.88 kΩ. The recommend resistor values for both DAC_VLOW and DAC_VHIGH are 0 Ω.

### Analog-to-Digital Converter

The IBIS5-1300 has a 10-bit flash analog digital converter running nominally at 40 Msamples/s. The ADC is electrically separated from the image sensor. Tie the input of the ADC (ADC_IN; pin 69) externally to the output (PXL_OUT1; pin 28) of the output amplifier.

**Table 14. ADC SPECIFICATIONS**

| | |
|---|---|
| Input range | 1–3 V (Note 1) |
| Quantization | 10 bits |
| Nominal data rate | 40 Msamples/s |
| DNL (linear conversion mode) | Typ. < 0.5 LSB |
| INL (linear conversion mode) | Typ. < 3 LSB |
| Input capacitance | < 20 pF |
| Power dissipation at 40 MHz | Typ. 45 mA x 3.3 V = 150 mW |
| Conversion law | Linear / Gamma-corrected |

1. The internal ADC range is typically 100 mV lower than the external applied ADC_VHIGH and ADC_VLOW voltages due to voltage drops over parasitic internal resistors in the ADC.

*ADC Timing*

At the rising edge of SYS_CLOCK, the next pixel is fed to the input of the output amplifier. Due to internal delays of the SYS_CLOCK signal, it takes approximately 20 ns before the output amplifier outputs the analog value of the pixel, as shown in Figure 13.

The ADC converts the pixel data on the rising edge of the ADC_CLOCK, but it takes two clock cycles before this pixel data is at the output of the ADC. Figure 13 shows this pipeline delay

Due to these delays, it is advisable that a variable phase difference is foreseen between the ADC_CLOCK and the SYS_CLOCK to tune the optimal sample moment of the ADC.

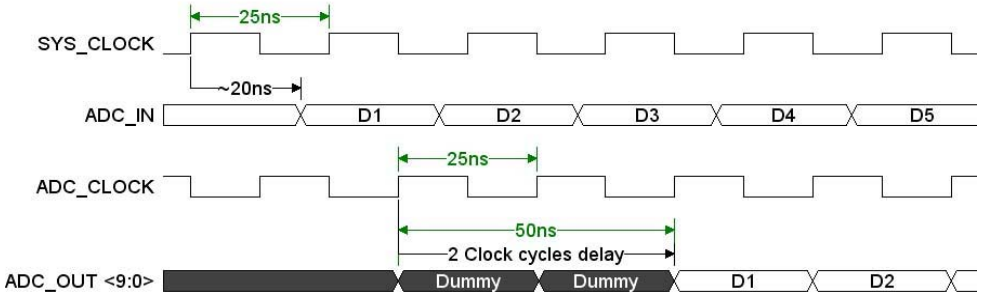



**Figure 13. ADC Timing**

*Setting ADC Reference Voltages*

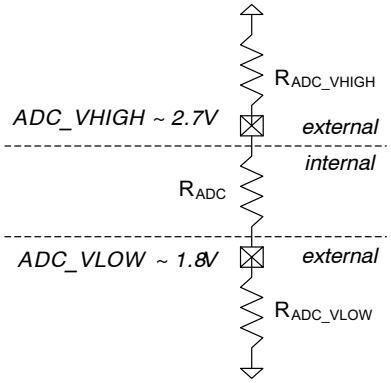



**Figure 14. Internal and External ADC Connections**

The internal resistor $R_{ADC}$ has a value of approximately 585 Ω. This results in the following values for the external resistors:

| Resistor | Value (O) |
|---|---|
| $R_{ADC_VHIGH}$ | 360 |
| $R_{ADC}$ | 585 |
| $R_{ADC_VLOW}$ | 1200 |

Note that the recommended ADC resistor values yield in a conversion of the full analog output swing at unity gain ($V_{DARK_ANALOG}$ < ADC_VHIGH and $V_{LIGHT_ANALOG}$ > ADC_VLOW).

The values of the resistors depend on the value of $R_{ADC}$. To assure proper working of the ADC, make certain the voltage difference between ADC_VLOW and ADC_VHIGH is at least 1.0 V.

*Nonlinear and Linear Conversion Mode—'gamma' Correction*

Figure 15 shows the ADC transfer characteristic. The nonlinear (exponential) ADC conversion is intended for gamma-correction of the images. It increases contrast in dark areas and reduces contrast in bright areas. The non-linear transfer function is given by the following equation:

$$Vin = ADC_VHIGH + (ADC_VHIGH - ADC_VLOW) * \frac{a*x + b*x^2}{a*1023 + b*1023^2}$$

where a = 5; b = 0.027; x = digital output code

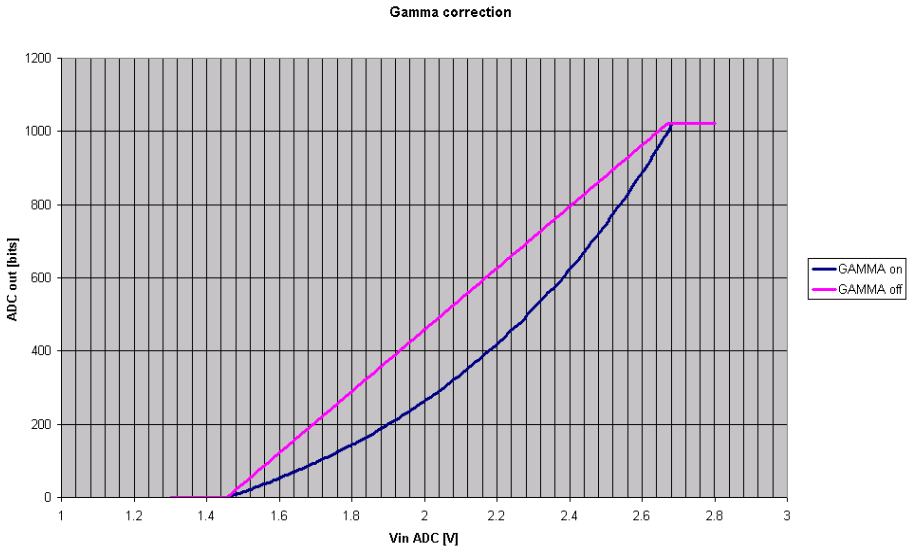



**Figure 15. Linear and Nonlinear ADC Conversion Characteristics**

*Sensor Digital Outputs*

The digital outputs of the sensor are not designed to drive large loads. Hence, the outputs cannot be used to directly drive cables or long traces on the PCB. If it is required to drive traces more than 5 inches long, it is advisable to use a buffer for all the digital signals given out by the sensor.

*Sensor Clock Inputs*

The ADC_CLOCK and the SYS_CLOCK of the sensor are typically 180 phase shifted from each other. However, depending on the board layout, it is possible that there may be a variation (increased phase shift of ADC_CLOCK with respect to SYS_CLOCK) in the phase shift between the clocks.

So, it is recommended that the phase shift between the clocks is maintained programmable.

*Clock Jitter Requirements:*

Min low time: 11.00 ns
Min high time: 11.00 ns
max rise time: 5 ns
max fall time: 5 ns
Max Duty cycle: 47% to 53%
Max period jitter: 150 ps

It is important that the clock is stable, reproducible and has low jitter. SYS_CLOCK and ADC_CLOCK are the most critical clocks, both clock interact in the readout path and influence the sensor performance.

*Black Calibration*

Due to slight variations in the chip fabrication process, the output analog voltage of the PGA is not perfectly matched to the input analog range of the ADC. As a result, a reduced dynamic range is compared when comparing sensors/cameras from different lots. This is especially true in the dark as it is possible that a part of the analog range gets clipped when it reaches the ADC.

For this reason, black calibration step is required. Because this is a fixed setting, and varies very slightly with temperature, the setting can be done at the factory itself.

While grabbing normal images, the settings can be loaded from an on-board memory.

In the IBIS5 image sensor, black calibration step also tries to match the output of the odd and even channels.

The steps for black calibration are -

1. Put the sensor in dark.
2. Change DAC_RAW such that no pixel or least number of pixels (assuming there are defect pixels) have a zero ADC output value.
3. Change DAC_FINE such that the average of the odd columns is almost same as the even columns.
4. Change DAC_RAW again such that all pixels have a non-zero output, but are as close to zero as possible.
5. Repeat for different gains.

### Electronic Shutter Types

The IBIS5-1300 has two shutter types: a rolling (curtain) shutter and a global shutter.

*Rolling (Curtain) Shutter*

The name is due to the fact that the effect is similar to a curtain shutter of a SLR film camera. Although it is an electronic operation, the shutter seems to slide over the image. A rolling shutter is easy and elegant to implement in a CMOS sensor. In the rolling shutter mode, there are two Y-shift registers. One of them points to the row that is currently being read out. The other shift register points to the row that is currently being reset. Both pointers are shifted by the same Y-clock and move over the focal plane. The integration time is set by the delay between both pointers.

Figure 16 graphically displays the relative shift of the integration times for different lines during the rolling shutter operation. Each line is read and reset in a sequential way. The integration time is the same for all lines, but is shifted in time. You can vary the integration time through the INT_TIME register (in number of lines)

This indicates that all pixels are light sensitive at another period of time, and can cause some blurring if a fast moving object is captured.

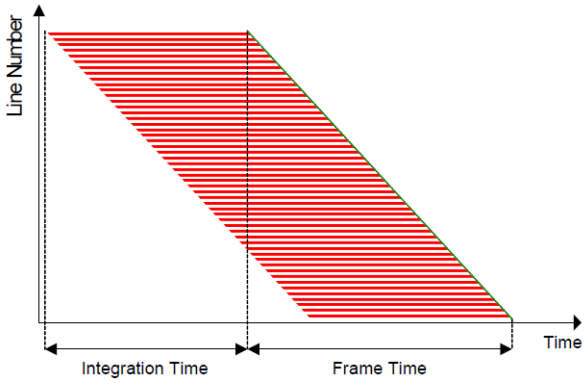



**Figure 16. Rolling Shutter Operation**

When the sensor is set to rolling shutter mode, make certain to hold the input SS_START ans SS_STOP low.

*Global Shutter*

A global (also known as synchronous or snapshot) shutter solves the inconvenience found in the rolling shutter. Light integration takes place on all pixels in parallel, although subsequent readout is sequential.

Figure 17 shows the integration and read out sequence for the synchronous shutter. All pixels are light sensitive at the same period of time. The whole pixel core is reset simultaneously and after the integration time all pixel values are sampled together on the storage node inside each pixel. The pixel core is read out line by line after integration. Note that the integration and read out cycle is carry-out in serial; that causes that no integration is possible during read out

During synchronous shutter mode, the input pins SS_START and SS_STOP are used to start and stop the synchronous shutter.

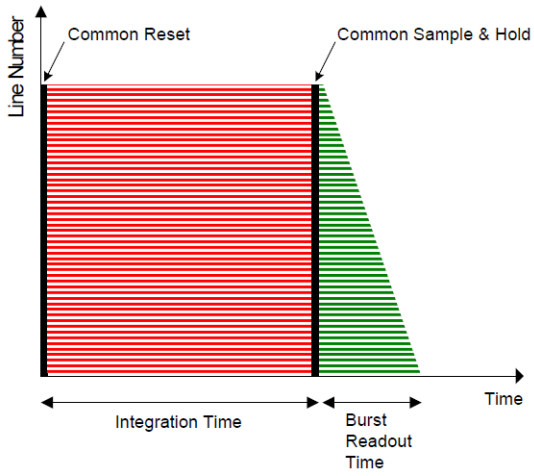



**Figure 17. Global Shutter Operation**

### Sequencer

Figure 8 on page 9 shows a number of control signals that are needed to operate the sensor in a particular sub-sampling mode with a certain integration time, output amplifier gain, and so on. Most of these signals are generated on-chip by the sequencer that uses only a few control signals. Make certain that these control signals are generated by the external system:

- SYS_CLOCK (X-clock) defines the pixel rate
- Y_START pulse indicates the start of a new frame read out
- Y_CLOCK selects a new row and starts the row blanking sequence, including the synchronization and loading of the X-register
- SS_START and SS_STOP control the integration period in snapshot shutter mode.

The relative position of the pulses is determined by a number of data bits that are uploaded in internal registers through the serial or parallel interface.

*Internal Registers*

Table 15 shows a list of the internal registers with a short description. In the next section, the registers are explained in more detail. On power-on, all registers in the sensor are reset to zero. To start operating the sensor, first load all the registers using the parallel or serial-3-wire interface. The value to be loaded in each register on power-on is given in the table.

**Table 15. INTERNAL REGISTERS**

| Register | Bit | Name | Description |
|---|---|---|---|
| 0 (0000) | 11:0 | SEQUENCER register | Default value <11:0>: '000011000100' |
| | 0 | SHUTTER_TYPE | 1 = rolling shutter<br>0 = synchronous shutter |
| | 1 | FRAME_CAL_MODE | 0 = fast<br>1 = slow |
| | 2 | LINE_CAL_MODE | 0 = fast<br>1 = slow |
| | 3 | CONT_CHARGE | 1 = 'Continuous' precharge enabled |
| | 4 | GRAN_X_SEQ_LSB | Granularity of the X sequencer clock |
| | 5 | GRAN_X_SEQ_MSB | |
| | 6 | GRAN_SS_SEQ_LSB | Granularity of the SS sequencer clock |
| | 7 | GRAN_SS_SEQ_MSB | |
| | 8 | KNEEPOINT_LSB | Sets reset voltage for multiple slope operation |
| | 9 | KNEEPOINT_MSB | |
| | 10 | KNEEPOINT_ENABLE | 1 = Enables multiple slope operation in synchronous shutter mode |
| | 11 | VDDR_RIGHT_EXT | 1 = Disables circuit that generates VDDR_RIGHT voltage; this allows the application of an external voltage |
| 1 (0001) | 11:0 | NROF_PIXELS | Number of pixels to count (maximum 1280/2)<br>Default value <11:0>: '001001111111' |
| 2 (0010) | 11:0 | NROF_LINES | Number of lines to count<br>Default value <11:0>: '001111111111' |
| 3 (0011) | 11:0 | INT_TIME | Integration time<br>Default value <11:0>: '111111111111' |
| 4 (0100) | 10:0 | X_REG | X start position (maximum 1280/2)<br>Default value <10:0>: '00000000000' |
| 5 (0101) | 10:0 | YL_REG | Y-left start position<br>Default value <10:0>: '00000000000' |
| 6 (0110) | 10:0 | YR_REG | Y-right start position<br>Default value <10:0>: '00000000000' |
| 7 (0111) | 7:0 | IMAGE CORE register | Default value <7:0>: '00000000' |
| | 0 | TEST_EVEN | Test even columns |
| | 1 | TEST_ODD | Test odd columns |
| | 2 | X_SUBSAMPLE | Enable sub-sampling in X-direction |
| | 3 | X_SWAP12 | Swap columns 1-2, 5-6, … |
| | 4 | X_SWAP30 | Swap columns 3-4, 7-8, … |
| | 5 | Y_SUBSAMPLE | Enable sub-sampling in Y-direction |
| | 6 | Y_SWAP12 | Swap rows 1-2, 5-6, … |
| | 7 | Y_SWAP30 | Swap rows 3-4, 7-8, … |
| 8 (1000) | 6:0 | AMPLIFIER register | Default value <6:0>: '1010000' |
| | 0 | GAIN<0> | Output amplifier gain setting |
| | 1 | GAIN<1> | |
| | 2 | GAIN<2> | |
| | 3 | GAIN<3> | |
| | 4 | UNITY | 1 = Amplifier in unity gain mode |
| | 5 | DUAL_OUT | 1 = Activates second output |

**Table 15. INTERNAL REGISTERS**

| | | | |
|---|---|---|---|
| 8 (1000) | 6 | STANDBY | 0 = Amplifier in standby mode |
| 9 (1001) | 6:0 | DACRAW_REG | Amplifier DAC raw offset<br>Default value <6:0>: ‘1000000’ |
| 10 (1010) | 6:0 | DACFINE_REG | Amplifier DAC fine offset<br>Default value <6:0>: ‘1000000’ |
| 11 (1011) | 2:0 | ADC register | Default value <2:0>: ‘011’ |
| | 0 | TRISTATE_OUT | 0 = Output bus in tri-state |
| | 1 | GAMMA | 0 = Gamma-correction on |
| | 2 | BIT_INV | 1 = Bit inversion on output bus |
| 12 (1100) | | Reserved | |
| 13 (1101) | | Reserved | |
| 14 (1110) | | Reserved | |
| 15 (1111) | | Reserved | |

*Detailed Description of Internal Registers*

**Sequencer register (7:0)**

1. Shutter type (bit 0)

   The IBIS5-1300 image sensor has two shutter types:
   0 = synchronous shutter
   1 = rolling shutter
2. Output amplifier calibration (bits 1 and 2)

   Bits FRAME_CAL_MODE and LINE_CAL_MODE define the calibration mode of the output amplifier.

   During every row-blanking period, a calibration is done of the output amplifier. There are two calibration modes. The FAST mode (0) forces a calibration in one cycle but is not so accurate and suffers from KTC noise. The SLOW mode (1) only makes incremental adjustments and is noise free.

   Approximately 200 or more ¿slow¿ calibrations have the same effect as one ¿fast¿ calibration. Different calibration modes are set at the beginning of the frame (FRAME_CAL_MODE bit) and for every subsequent line that is read (LINE_CAL_MODE bit). The Y_START input defines the beginning of a frame, Y_CLOCK defines the beginning of a new row.
3. Continuous charge (bit 3)

   Some applications may require the use continuous charging of the pixel columns instead of a pre-charge on every line sample operation.

   Setting bit CONT_CHARGE to ‘1’ activates this function. The resistor connected to pin PC_CMD controls the current level on every pixel column.
4. Internal clock granularities (bits 4, 5, 6 and 7)

   The system clock is divided several times on-chip. Half the system clock rate clocks the X-shift-register that controls the column/pixel readout. Odd and even pixel columns are switched to two separate buses. In the output amplifier, the pixel signals on the two buses are combined into one pixel stream at the same frequency as SYS_CLOCK.

   Use the bits GRAN_SS_SEQ_MSB (bit 7) and GRAN_SS_SEQ_LSB (bit 6) to program the clock that drives the ‘snapshot’ or synchronous shutter sequencer. This way the integration time in synchronous shutter mode is a multiple of 32, 64, 128, or 256 times the system clock period. To overcome global reset issues, use the longest SS granularity (bits 6 and 7 set to ‘1’).

**Table 16. SS SEQUENCER CLOCK GRANULARITIES**

| GRAN_SS_SEQ_MSB/ LSB | SS-Sequencer Clock | Integration Time Step[1] |
|---|---|---|
| 00 | 32 x SYS_CLOCK | 800 ns |
| 01 | 64 x SYS_CLOCK | 1.6 μs |
| 10 | 128 x SYS_CLOCK | 3.2 μs |
| 11 | 256 x SYS_CLOCK | 6.4 μs |

1. Using a SYS_CLOCK of 40 MHz (25 ns period).

The clock that drives the X-sequencer is a multiple of 4, 8, 16, or 32 times the system clock. Clocking the X-sequencer at a slower rate (longer row blanking time; pixel read out speed is always equal to the SYSTEM_CLOCK) results in more signal swing for the same light conditions.

**Table 17. X SEQUENCER CLOCK GRANULARITIES**

| GRAN_X_SEQ_MSB/ LSB | X-Sequencer Clock | Integration Time Step[1] |
|---|---|---|
| 00 | 4 x SYS_CLOCK | 100 ns |
| 01 | 8 x SYS_CLOCK | 200 ns |
| 10 | 16 x SYS_CLOCK | 400 ns |
| 11 | 32 x SYS_CLOCK | 800 ns |

1. Using a SYS_CLOCK of 40 MHz (25 ns period).

5. Pixel reset knee-point for multiple slope operation (bits 8, 9, and 10)

   In normal (single slope) mode the pixel reset is controlled from the left side of the image core using the voltage applied on pin VDDR_LEFT as pixel reset voltage. In multiple slope operation, apply one or more variable pixel reset voltages.

   Bits KNEE_POINT_MSB and KNEE_POINT_LSB select the on chip-generated pixel reset voltage.

   Bit KNEE_POINT_ENABLE set to ¿1¿ switches control to the right side of the image core so the pixel reset voltage (VDDR_RIGHT), selected by bits KNEE_POINT_MSB/LSB, is used.

   Use bit KNEE_POINT_ENABLE only for multiple slope operation in synchronous shutter mode. In rolling shutter mode, use only the bits KNEE_POINT_MSB/LSB to select the second knee-point in dual slope operation. The actual knee-point depends on VDDH, VDDR_LEFT and VDDC applied to the sensor.

**Table 18. MULTIPLE SLOPE REGISTER SETTINGS**

| KNEE_POINT | | Pixel Reset Voltage (V)VDDR_RIGHT | Knee-point (V) |
|---|---|---|---|
| MSB/LSB | ENABLE | | |
| 00 | 0 or 1 | VDDR_LEFT | 0 |
| 01 | 1 | VDDR_LEFT – 0.76 | + 0.76 |
| 10 | 1 | VDDR_LEFT – 1.52 | + 1.52 |
| 11 | 1 | VDDR_LEFT – 2.28 | + 2.28 |

6. External Pixel Reset Voltage for Multiple Slope (bit 11)

   Setting bit VDDR_RIGHT_EXT to ‘1’ disables the circuit that generates the variable pixel reset voltage and uses the voltage externally applied to pin VDDR_RIGHT as the double/multiple slope reset voltage.

   Setting bit VDDR_RIGHT_EXT to ‘0’ allows you to monitor the variable pixel reset voltage (used for multiple slope operation) on pin VDDR_RIGHT.

**NROF_PIXELS Register (11:0)**

After the internal x_sync is generated (start of the pixel readout of a particular row), the PIXEL_VALID signal goes high. The PIXEL_VALID signal goes low when the pixel counter reaches the value loaded in the NROF_PIXEL register. Due to the fact that two pixels are read at the same clock cycle, you must divide this number by 2 (NROF_PIXELS = (width of ROI / 2) – 1).

**ROF_LINES Register (11:0)**

After the internal yl_sync is generated (start of the frame readout with Y_START), the line counter increases with each Y_CLOCK pulse until it reaches the value loaded in the NROF_LINES register and generates a LAST_LINE pulse. It must be noted that the value loaded in the register must be (Number of lines required - 1).

**INT_TIME Register (11:0)**

Use the INT_TIME register to set the integration time of the electronic shutter. The interpretation of the INT_TIME depends on the chosen shutter type (rolling or synchronous).

- Global shutter

After the SS_START pulse is applied an internal counter counts the number of SS granulated clock cycles until it reaches the value loaded in the INT_TIME register and generates a TIME_OUT pulse. Use this TIME_OUT pulse to generate the SS_STOP pulse to stop the integration. When the INT_TIME register is used, the maximum integration time is:

TINT_MAX =

[4095 * 256 (max granularity) * (40 MHz) –1] = 26.2 ms.

You can increase this maximum time if you use an external counter to trigger SS_STOP. Ten is the minimal value that you can load into the INT_TIME register (see also Internal clock granularities (bits 4, 5, 6 and 7) on page 17).

- Rolling shutter

When the Y_START pulse is applied (start of the frame readout), the sequencer generates the yl_sync pulse for the left Y-shift register (read out Y-shift register). This loads the left Y-shift register with the pointer loaded in YL_REG register. At each Y_CLOCK pulse, the pointer shifts to the next row and the integration time counter increases until it reaches the value loaded in the INT_TIME register. At that moment, the sequencer generates the yr_sync pulse for the right Y-shift register; it loads the right Y-shift register (reset Y-shift register) with the pointer loaded in YR_REG register (see Figure 18). The integration time counter is reset when the sync for the left Y-shift register, yl_sync is asserted. Both shift registers keep moving until the next sync is asserted, i.e., the yl_sync for the left Y-shift register (generated by Y_START) and the yr_sync for the right Y-shift register (generated when the integration time counter reaches the INT_TIME value).

Treg_int Difference between the left and right pointer = value set in the INT_TIME register (number of lines).

The actual integration time is given by

Tint Integration time [# lines] =

NROF_LINES register – INT_TIME register.

Tint Integration time [# lines] =

NROF_LINES register – INT_TIME register.

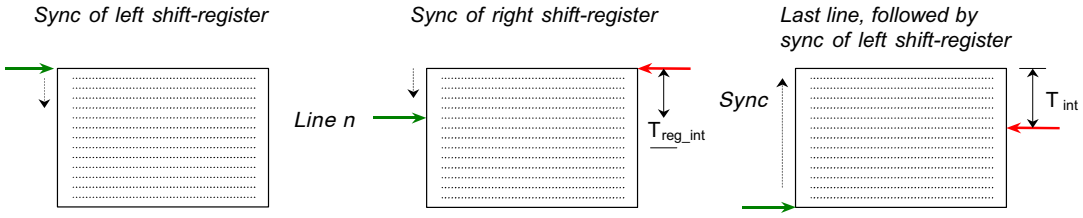



**Figure 18. Synchronization of Shift Registers in Rolling Shutter Mode**

**X_REG Register (10:0)**

The X_REG register determines the start position of the window in the X-direction. In this direction, there are 640 possible starting positions (two pixels are addressed at the same time in one clock cycle). If sub sampling is enabled, only the even pixels are set as starting position (for instance: 0, 2, 4, 6, 8… 638).

**YL_REG (10:0) and YR_REG (10:0)**

The YL_REG and YR_REG registers determine the start position of the window in the Y-direction. In this direction, there are 1024 possible starting positions. In rolling shutter mode the YL_REG register sets the start position of the read (left) pointer and the YR_REG sets the start position of the reset (right) pointer. For both shutter types YL_REG is always equal to YR_REG.

**Image Core Register (7:0)**

Bits 1:0 of the IMAGE_CORE register define the test mode of the image core. Setting 00 is the default and normal operation mode. In case the bit is set to ‘1’, the odd (bit 1) or even (bit 0) columns are tight to the reset level. If the internal ADC is used, bits 0 and 1 are used to create test pattern to test the sample moment of the ADC. If the ADC sample moment is not chosen correctly, the created test pattern is not black-white-black-etc. (IMAGE_CORE register set at 1 or 2) or black-black-white-white-black-black (IMAGE_CORE register set at 9) but grey shadings if the sensor is saturated.

Bits 7:2 of the IMAGE_CORE register define the sub-sampling mode in the X-direction (bits 4:2) and in the Y-direction (bits 7:5). The sub-sampling modes and corresponding bit setting are given in Table 11 and Table 12 on page 11.

**Amplifier Register (6:0)**

1. GAIN (bits 3:0)
   The gain bits determine the gain setting of the output amplifier. They are only effective if UNITY = 0. The gains and corresponding bit setting are given in Table 13 on page 12.
2. UNITY (bit 4)
   In case UNITY = 1, the gain setting of GAIN is bypassed and the gain amplifier is put in unity feedback.
3. DUAL_OUT (bit 5)
   If DUAL_OUT = 1, the two output amplifiers are active. If DUAL_OUT = 0, the signals from the two buses are multiplexed to output PXL_OUT1 which connects to ADC_IN. The gain amplifier and output driver of the second path are put in standby.
4. STANDBY
   If STANDBY = 0, the complete output amplifier is put in standby. For normal use, set STANDBY to ‘1’.

**DAC_RAW Register (6:0) and DAC_FINE (6:0) Register**

These registers determine the black reference level at the output of the output amplifier. Bit setting 1111111 for the DAC_RAW register gives the highest offset voltage. Bit setting 0000000 for the DAC_RAW register gives the lowest offset voltage. Ideally, if the two output paths have no offset mismatch, the DAC_FINE register is set to 1000000. Deviation from this value is used to compensate the internal mismatch (see Output Amplifier on page 12).

**ADC Register (2:0)**

1. TRISTATE_OUT (bit 0)
   In case TRISTATE = 0, the ADC_D<9:0> outputs are in tri-state mode. TRISTATE = 1 for normal operation mode.
2. GAMMA (bit 1)
   If GAMMA is set to ‘1’, the ADC input to output conversion is linear; otherwise the conversion follows a ‘gamma’ law (more contrast in dark parts of the window, lower contrast in the bright parts).
3. BIT_INV (bit 2)
   If BIT_INV = 1, 0000000000 is the conversion of the lowest possible input voltage, otherwise the bits are inverted.

*Data Interfaces*

Two different data interfaces are implemented. They are selected using pins IF_MODE (pin 12) and SER_MODE (pin 6).

**Table 19. SERIAL AND PARALLEL INTERFACE SELECTION**

| IF_MODE | SER_MODE | Selected interface |
|---|---|---|
| 1 | X | Parallel |
| 0 | 1 | Serial 3 Wire |

**Parallel Interface**

The parallel interface uses a 16-bit parallel input (P_DATA (15:0)) to upload new register values. Asserting

P_WRITE loads the parallel data into the internal register of the IBIS5-1300 where it is decoded (see Figure 19). P_DATA (15:12) address bits REG_ADDR (3:0); P_DATA (11:0) data bits REG_DATA (11:0).

*Serial 3-Wire Interface*

The serial 3-wire interface (or serial-to-parallel Interface) uses a serial input to shift the data in the register buffer. When the complete data word is shifted into the register buffer the data word is loaded into the internal register where it is decoded (see Figure 19). S_DATA (15:12) address bits REG_ADDR (3:0); S_DATA (11:0) data bits REG_DATA (11:0). When S_EN is asserted the parallel data is loaded into the internal registers of the sensor. The maximum tested frequency of S_DATA is 2.5 MHz.) The serial 2-wire interface is not operational in the IBIS5-1300 image sensor. Use the 3-wire SPI interface to load the sensor registers.

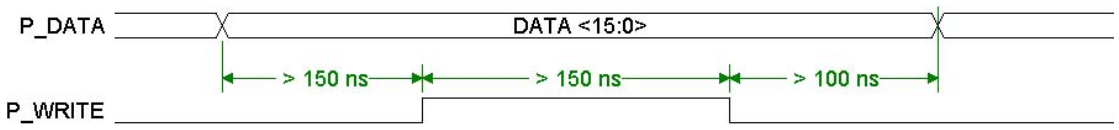



**Figure 19. Parallel Interface Timing**

## TIMING DIAGRAMS

### Frame Rate

The pixel rate for this sensor is high enough to support a frame rate of greater than 100 Hz for a window size of 640 x 480 pixels (VGA format). Considering a row blanking time of 3.5 μs (as baseline, see also Internal clock granularities (bits 4, 5, 6 and 7) on page 17), this requires a minimum pixel rate of nearly 40 MHz. The final bandwidth of the column amplifiers, output stage, and others is determined by external bias resistors. With a nominal pixel rate of 40 MHz, a full frame rate of a little more than 27 frames per second is obtained.

The frame period of the IBIS5-1300 sensor depends on the shutter type.

*Rolling Shutter*

=> Frame period = (Nr. Lines * (RBT + pixel period * Nr. Pixels))

with:

| | |
|---|---|
| Nr. Lines | Number of lines read out each frame (Y) |
| Nr. Pixels | Number of pixels read out each line (X) |
| RBT | Row blanking time = 3.5 μs (typical) |
| Pixel period | 1/40 MHz = 25 ns |

**Example** Read out time of the full resolution at nominal speed (40 MHz pixel rate):

Frame period = (1024 * (3.5 μs + 25 ns * 1280)) = 36.4 ms = 27.5 fps

*Global shutter*

Frame period = Tint + Tread out

= Tint + (Nr. Lines * (RBT + pixel period * Nr. Pixels))

| | |
|---|---|
| with: Tint | Integration (exposure) time |
| Nr. Lines | Number of lines read out each frame (Y) |
| Nr. Pixels | Number of pixels read out each line (X) |
| RBT | Row blanking time = 3.5 μs (typical) |
| Pixel period | 1/40 MHz = 25 ns |

**Example** Read out time of the full resolution at nominal speed (40 MHz pixel rate) with an integration time of 1 ms:

Frame period = 1 ms + (1024 * (3.5 μs + 25 ns * 1280)) = 37.4 ms = 26.8 fps

*Region-of-Interest (ROI) Read Out*

Windowing is easily achieved by uploading the starting point of the X- and Y-shift registers in the sensor registers using the various interfaces. This downloaded starting point initiates the shift register in the X- and Y-direction triggered by the Y_START (initiates the Y-shift register) and the Y_CLK (initiates the X-shift register) pulse. The minimum step size for the x-address is two (only even start addresses are chosen) and one for the Y-address (every line is addressable). The frame rate increases almost linearly when fewer pixels are read out. Table 20 gives an overview of the achievable frame rates (in rolling shutter mode) with various ROI dimensions.

**Table 20. FRAME RATE VS. RESOLUTION**

| Image Resolution (X x Y) | Frame Rate [frames/s] | Frame Readout Time [ms] | Comment |
|---|---|---|---|
| 1280 x 1024 | 27 | 36 | Full resolution. |
| 640 x 480 | 100 | 10 | ROI read out. |
| 100 x 100 | 1657 | 0.6 | ROI read out. |

### Timing Requirements

There are six control signals that operate the image sensor:

- SS_START
- SS_STOP
- Y_CLOCK
- Y_START
- X_LOAD
- SYS_CLOCK

The external system generates these control signals with following time constraints to SYS_CLOCK (rising edge = active edge):

$T_{SETUP}$ >7.5 ns

$T_{HOLD}$ > 7.5 ns

It is important that these signals are free of any glitches.

Figure 20 shows a recommended schematic for generating the basic signals and to avoid any timing problems.

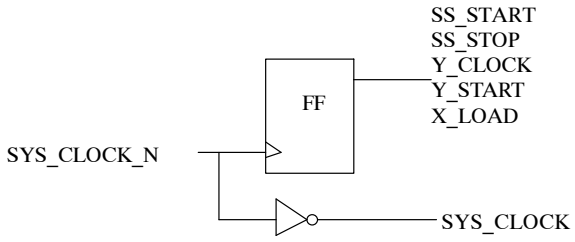



**Figure 20. Recommended Schematic for Basic Signals**

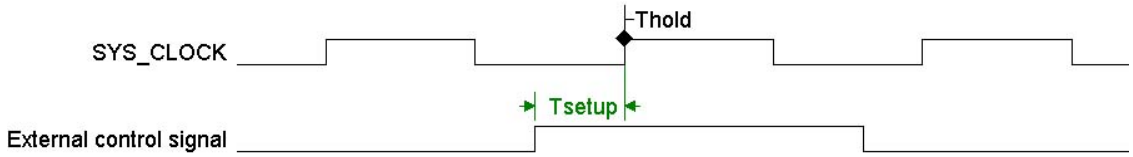



**Figure 21. Relative Timing of 5−Sequencer Control Signal**

### Global Shutter: Single Slope Integration

SS_START and SS_STOP must change on the falling edge of the SYS_CLOCK (Tsetup and Thold > 7.5 ns). Make certain that the pulse width of both signals is a minimum of 1 SYS_CLOCK cycle. As long as SS_START or SS_STOP are asserted, the sequencer stays in a suspended state (see Figure 22).

$T_1$ - Time counted by the integration timer until the value of INT_TIME register is reached. The integration timer is clocked by the granulated SS-sequencer clock.

$T_2$ - TIME_OUT signal stays high for one granulated SS-sequencer clock period.

$T_3$ - There are no constraints for this time. Use the TIME_OUT signal to trigger the SS_STOP pin (or use an external counter to trigger SS_STOP); you cannot tie both signals together.

$T_4$ - During this time, the SS-sequencer applies the control signals to reset the image core and start integration. This takes four granulated SS-sequencer clock periods. The integration time counter starts counting at the first rising edge after the falling edge of SS_START.

$T_5$ - The SS-sequencer puts the image core in a readable state. It takes two granulated SS-sequencer clock periods.

$T_{int}$ - The ‘real’ integration or exposure time.

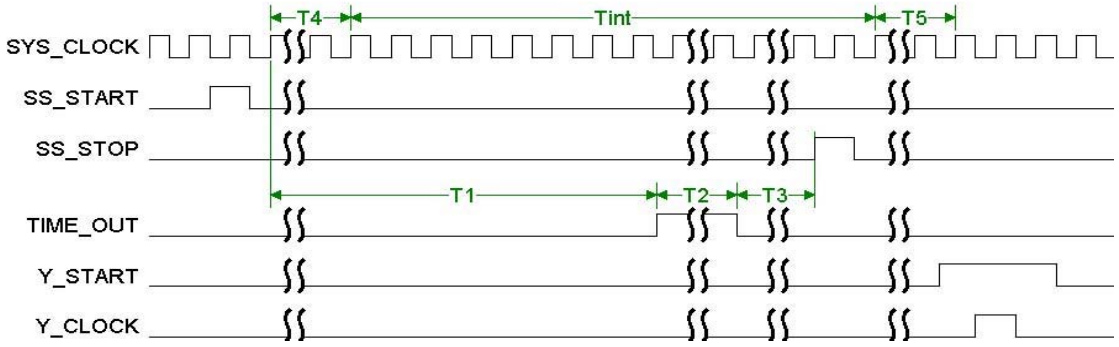



**Figure 22. Global Shutter: Single Slope Integration**

### Global Shutter: Pixel Readout

*Basic Operation*

Y_START and Y_CLOCK must change on the falling edge of the SYS_CLOCK (Tsetup and Thold > 7.5 ns). Make certain that the pulse width is a minimum of one clock cycle for Y_CLOCK and three clock cycles for Y_START. As long as Y_CLOCK is applied, the sequencer stays in a suspended state. (See Figure 23)

$T_1$- Row blanking time: During this period, the X-sequencer generates the control signals to sample the pixel signal and pixel reset levels (double sampling fpn-correction), and starts the readout of one line. The row blanking time depends on the granularity of the X-sequencer clock (see Table 21 on page 22).

$T_2$ - Pixels counted by pixel counter until the value of NROF_PIXELS register is reached. PIXEL_VALID goes high when the internal X_SYNC signal is generated, in other words when the readout of the pixels is started. PIXEL_VALID goes low when the pixel counter reaches the value loaded in the NROF_PIXELS register (after a complete row read out).

$T_3$ - LAST_LINE goes high when the line counter reaches the value loaded in the NROF_LINES register and stays high for one line period (until the next falling edge of Y-CLOCK).

On Y_START the left Y-shift-register of the image core is loaded with the YL-pointer that is loaded in to register YL_REG.

*Advanced Operation:*

It was observed during characterization of the IBIS5-1300 image sensor that there are column non-uniformities in the image in synchronous shutter mode, when the Y-readout pointer is still selecting a line during the global reset for the next frame. To avoid this problem, an advanced timing has been generated for the synchronous shutter mode. See question 12 in AN6004, Frequently Asked Questions about the IBIS5 Device for more information. The application note discusses the cause and corrective action for this problem.

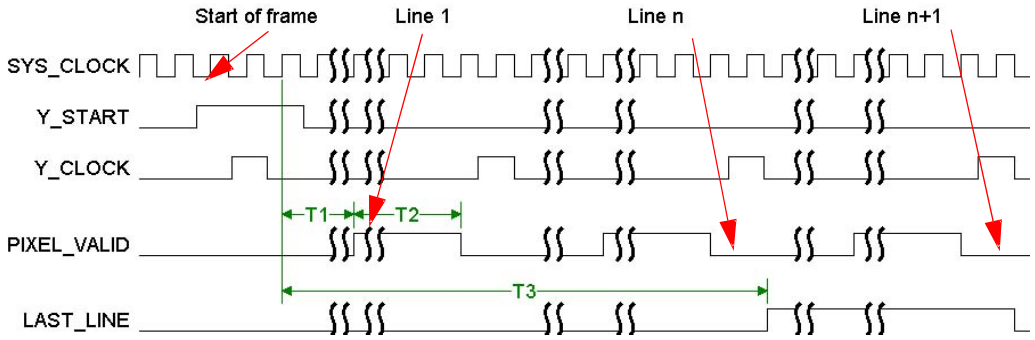



**Figure 23. Global Shutter: Pixel Read Out**

*Pixel Output*

The pixel signal at the PXL_OUT1 output becomes valid after five SYS_CLOCK cycles when the internal X_SYNC (start of PIXEL_VALID output or external X_LOAD pulse) pulse is asserted (see Figure 24).

$T_1$ - Row blanking time (see Table 21).

$T_2$ - 5 SYS_CLOCK cycles.

$T_3$ - Time for new X-pointer position upload in X_REG register (see Windowing in X−Direction on page 24 for more details).

**Table 21. ROW BLANKING TIME AS FUNCTION OF X−SEQUENCER GRANULARITY**

| Granularity $N_{GRAN}$ | $T_1(\mu s)$ $= 35 \times N_{GRAN} \times T_{SYS_CLOCK}$ | GRAN_X_SEQ MSB/LSB |
|---|---|---|
| x 4 | 140 x $T_{SYS_CLOCK}$ = 3.5 | 00 |
| x 8 | 280 x $T_{SYS_CLOCK}$ = 7.0 | 01 |
| x 16 | 560 x $T_{SYS_CLOCK}$ = 14.0 | 10 |
| x 32 | 1120 x $T_{SYS_CLOCK}$ = 28.0 | 11 |

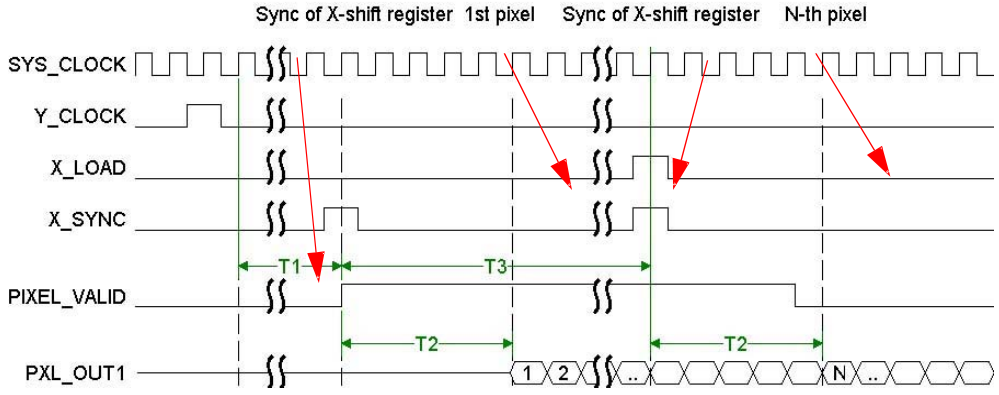



**Figure 24. Pixel Output**

### Global Shutter: Multiple Slope Integration

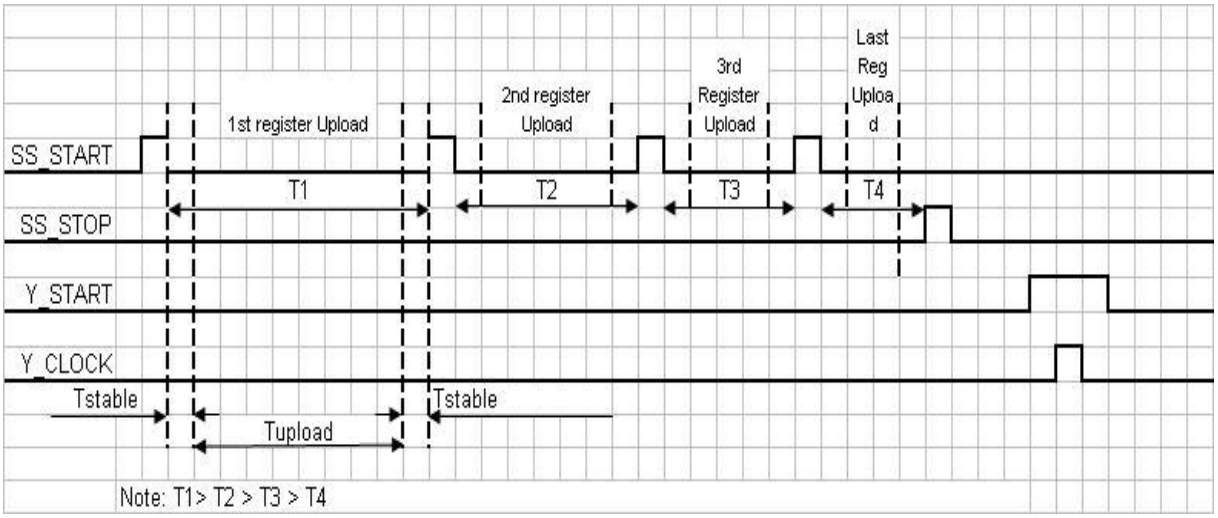



**Figure 25. Multiple Slope Integration**

Use up to four different pixel reset voltages during multiple slope operation in synchronous shutter mode. This is done by uploading new values to register bits KNEEPOINT_MSB/LSB/ENABLE before a new SS_START pulse is applied.

Set bit KNEEPOINT_ENABLE high to do a pixel reset with a lower voltage.

Set bits KNEEPOINT_MSB/LSB/ENABLE back to '0' before the SS_STOP pulse is applied. Every time an SS_START pulse is applied, the integration time counter is reset.

The TIME_OUT signal cannot be used in multi-slope operation to determine the location of the next SS_START or SS_STOP pulse. External counters must be used for generating these signals.

**Table 22. MULTIPLE SLOPE REGISTER SETTINGS**

| | Kneepoint | |
|---|---|---|
| | MSB/LSB | Enable |
| Initial Setup | 00 | 0 |
| 1st Register Upload | 01 | 1 |
| 2nd Register Upload | 10 | 1 |
| 3th Register Upload | 11 | 1 |
| 4th Register Upload | 00 | 0 |

Upload the register after time $T_{stable}$, otherwise, the change affects the SS-sequencer resulting in a bad pixel reset. $T_{stable}$ depends on the granularity of the SS-sequencer clock (see Table 23).

**Table 23. $T_{stable}$ FOR DIFFERENT GRANULARITY SETTINGS**

| Granularity $N_{GRAN}$ | $T_{stable}$ (μs) = 5 x $N_{GRAN}$ x $T_{SYS_CLOCK}$ | GRAN_SS_SEQ MSB/LSB |
|---|---|---|
| x 32 | 160 x $T_{SYS_CLOCK}$ = 4 | 00 |
| x 64 | 320 x $T_{SYS_CLOCK}$ = 8 | 01 |
| x 128 | 640 x $T_{SYS_CLOCK}$ = 16 | 10 |
| x 256 | 1280 x $T_{SYS_CLOCK}$ = 32 | 11 |

$T_{upload}$ depends on the interface mode used to upload the registers.

**Table 24. $T_{upload}$ FOR DIFFERENT INTERFACE MODES**

| Interface Mode | $T_{upload}$ (μs) |
|---|---|
| Parallel | 1 |
| Serial 3-wire | 8 |

### Rolling Shutter Operation

The integration of the light in the image sensor is done during readout of the other lines.

The only difference with synchronous shutter is that the TIME_OUT pin is used to indicate when the Y_SYNC pulse for the right Y-shift-register (reset Y-shift register) is generated. This loads the right Y-shift-register with the pointer loaded in register YR_REG. The Y_SYNC pulse for the left Y-shift register (read Y-shift register) is generated with Y_START.

The INT_TIME register defines how many lines to count before the Y_SYNC of the right Y-shift-register is generated, hence defining the integration time. See also INT_TIME Register (11:0) on page 18 for a detailed description of the rolling shutter operation.

$T_{int}$ Integration time [# lines] = register(NROF_LINES) – register(INT_TIME)

NOTE: For normal operation the values of the YL_REG and YR_REG registers are equal.

### Windowing in X-Direction

An X_LOAD pulse overrides the internal X_SYNC signal, loading a new X-pointer (stored in the X_REG register) into the X-shift-register.

The X_LOAD pulse must appear on the falling edge of SYS_CLOCK and remain high for two SYS_CLOCK cycles overlapping two rising edges of SYS_CLOCK. The new X-pointer is loaded on one of the two rising edges of SYS_CLOCK.

The available time to upload the register is $T_{load}$; it is defined from the previous register load to the rising edge of X_LOAD. It depends on the settling time of the register and the X-decoder.

**Table 25. $T_{load}$ FOR DIFFERENT INTERFACES**

| Interface Mode | $T_{load}$ (µs) |
|---|---|
| Parallel interface | 1 (about 40 SYS_CLOCK cycles) |
| Serial 3 Wire | 16 (at 2.5 MHz data rate) |

The actual time to load the register itself depends on the interface mode that is used. The parallel interface is the fastest.

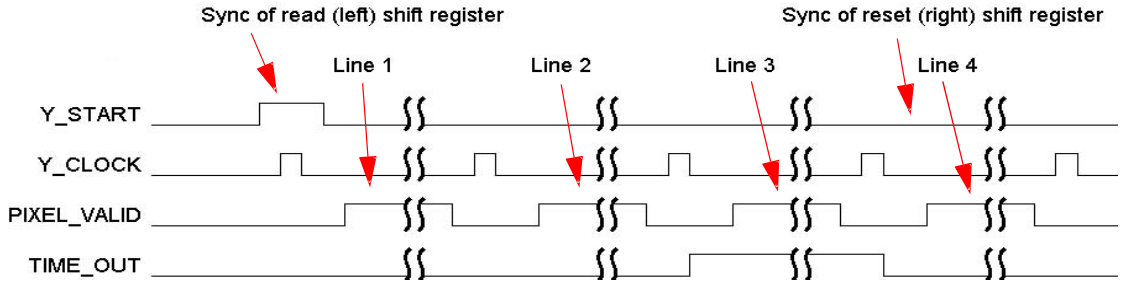



**Figure 26. Rolling Shutter Operation**

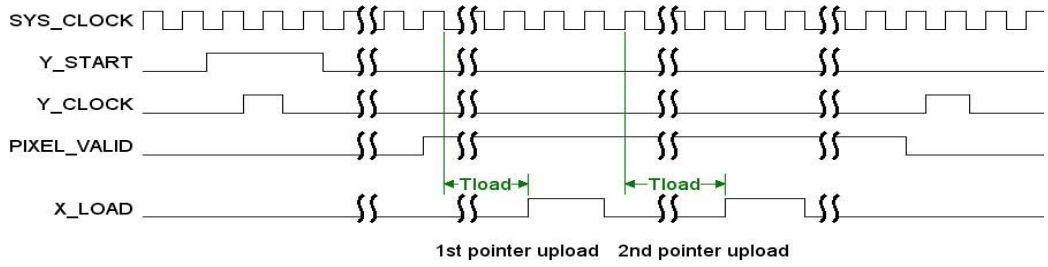



**Figure 27. Windowing in X−Direction**

### Windowing in Y-Direction

Reapply the Y_START pulse after loading a new Y-pointer value into the YL_REG and YR_REG registers to load a new Y-pointer into the Y-shift-register.

Every time a Y_START pulse appears, a frame calibration of the output amplifier occurs.

### Initialization (Startup Behavior)

To avoid any high current consumption at startup, apply the SYS_CLOCK signal as soon as possible after or even before power on of the image sensor. After power on, apply SYS_RESET for a minimum of five SYS_CLOCK periods to ensure a proper reset of the on-chip sequencer and timing circuitry. All internal registers are set to ‘0’ after SYS_RESET is applied.

Because all the IBIS5-1300 control signals are active high, apply a low level (before SYS_RESET occurs) to these pins at start up to avoid latch up.

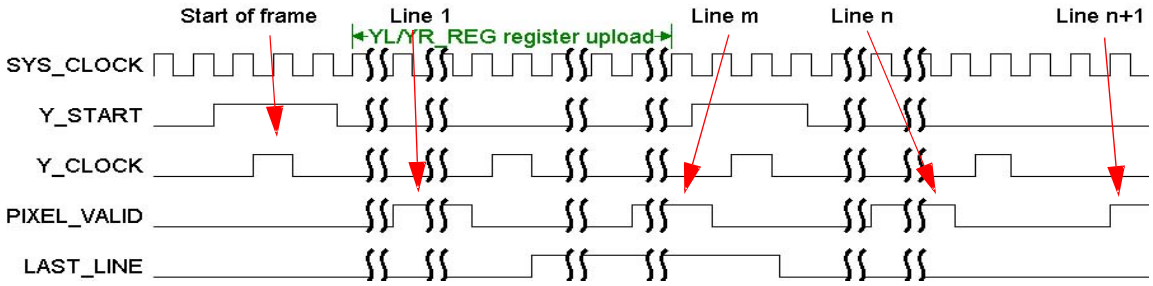



**Figure 28. Windowing in Y−Direction**

## PACKAGE INFORMATION

### Pin List

The IBIS5-1300 image sensor has 84 pins and is packaged in a leadless ceramic carrier (LCC) package. Table 26 lists the pins and their functions.

**Table 26. PIN LIST** (Notes 1, 2 and 3)

| Pin | Pin Name | Pin Type | Pin Description |
|---|---|---|---|
| 1 | P_DATA<8> | Input | Digital input. Data parallel interface. |
| 2 | P_WR | Input | Digital input (active high). Parallel write. |
| 3 | S_CLK | Input | Digital input. Clock signal of serial interface. |
| 4 | S_DATA | Input | Digital input/output. Data of serial interface. |
| 5 | S_EN | Input | Digital input (active low). Enable of serial 3-wire interface. |
| 6 | SER_MODE | Input | Digital input. Serial mode enable (1 = Enable serial 3-wire). |
| 7 | VDDC | Supply | Analog supply voltage. Supply voltage of the pixel core [3.3 V]. |
| 8 | VDDA | Supply | Analog supply voltage. Analog supply voltage of the image sensor [3.3 V]. |
| 9 | GNDA | Ground | Analog ground. Analog ground of the image sensor. |
| 10 | GNDD | Ground | Digital ground. Digital ground of the image sensor. |
| 11 | VDDD | Supply | Digital supply voltage. Digital supply voltage of the image sensor [3.3 V]. |
| 12 | IF_MODE | Input | Digital input. Interface mode (1 = parallel; 0 = serial). |
| 13 | DEC_CMD | Input | Analog input. Biasing of decoder stage. Connect to VDDA with R = 50 kΩ and decouple with C = 100 nF to GNDA. |
| 14 | Y_START | Input | Digital input (active high). Start frame read out. |
| 15 | Y_CLOCK | Input | Digital input (active high). Line clock. |
| 16 | LAST_LINE | Output | Digital output. Generates a high level when the last line is read out. |
| 17 | X_LOAD | Input | Digital input (active high). Loads new X-position during read out. |
| 18 | SYS_CLOCK | Input | Digital input. System (pixel) clock (40 MHz). |
| 19 | PXL_VALID | Output | Digital output. Generates high level during pixel read out. |
| 20 | SS_START | Input | Digital input (active high). Start synchronous shutter operation. |
| 21 | SS_STOP | Input | Digital input (active high). Stop synchronous shutter operation. |
| 22 | TIME_OUT | Output | Digital output.<br>Global shutter: pulse when timeout reached. It is used to trigger SS_STOP; do not tie both signals together.<br>Rolling shutter: pulse when second Y-sync appears. |
| 23 | SYS_RESET | Input | Digital input (active high). Global system reset. |
| 24 | EL_BLACK | Input | Digital input (active high). Enables electrical black in output amplifier. |
| 25 | EOSX | Output | Digital output. Diagnostic end-of-scan of X-register. |
| 26 | DAC_VHIGH | Input | Analog reference input. Biasing of DAC for output dark level. Use this to set the output range of DAC.<br>Default: Connect to VDDA with R = 0 Ω. |
| 27 | DAC_VLOW | Input | Analog reference input. Biasing of DAC for output dark level. Use this to set the output range of DAC.<br>Default: Connect to GND A with R = 0 Ω. |
| 28 | PXL_OUT1 | Output | Analog output. Analog pixel output 1. |
| 29 | PXL_OUT2 | Output | Analog output. Analog pixel output 2. Leave not connected if not used. |
| 30 | AMP_CMD | Input | Analog input. Biasing of the output amplifier. Connect to VDDA with R = 50 kΩ and decouple with C = 100 nF to GNDA. |

1. All pins with the same name can be connected together.
2. All digital input are active high (unless mentioned otherwise).
3. Tie all digital inputs that are not used to GND (inactive level).

**Table 26. PIN LIST** (Notes 1, 2 and 3)

| Pin | Pin Name | Pin Type | Pin Description |
|---|---|---|---|
| 31 | COL_CMD | Input | Analog input. Biasing of the column amplifiers. Connect to VDDA with R = 50 kΩ and decouple with C = 100 nF to GNDA. |
| 32 | PC_CMD | Input | Analog input. Pre-charge bias. Connect to VDDA with R = 25 kΩ and decouple with C = 100 nF to GNDA. |
| 33 | VDDD | Supply | Digital supply. Digital supply voltage of the image sensor [3.3 V]. |
| 34 | GNDD | Ground | Digital ground. Digital ground of the image sensor. |
| 35 | GNDA | Ground | Analog ground. Analog ground of the image sensor. |
| 36 | VDDA | Supply | Analog supply voltage. Analog supply voltage of the image sensor [3.3 V]. |
| 37 | VDDC | Supply | Analog supply voltage. Supply voltage of the pixel core [3.3 V]. |
| 38 | P_DATA<0> | Input | Digital input. Data parallel interface (LSB). |
| 39 | P_DATA<1> | Input | Digital input. Data parallel interface. |
| 40 | P_DATA<2> | Input | Digital input. Data parallel interface. |
| 41 | P_DATA<3> | Input | Digital input. Data parallel interface. |
| 42 | P_DATA<4> | Input | Digital input. Data parallel interface. |
| 43 | P_DATA<5> | Input | Digital input. Data parallel interface. |
| 44 | P_DATA<6> | Input | Digital input. Data parallel interface. |
| 45 | P_DATA<7> | Input | Digital input. Data parallel interface. |
| 46 | SI2_ADDR<0> | Input | Digital Input. Connect to GNDD. |
| 47 | SI2_ADDR<1> | Input | Digital Input. Connect to GNDD. |
| 48 | SI2_ADDR<2> | Input | Digital Input. Connect to GNDD. |
| 49 | SI2_ADDR<3> | Input | Digital Input. Connect to GNDD. |
| 50 | SI2_ADDR<4> | Input | Digital Input. Connect to GNDD. |
| 51 | GNDAB | Supply | Analog supply voltage. Anti-blooming ground. |
| 52 | VDDR_RIGHT | Supply | Analog supply voltage. Variable reset voltage (multiple slope operation). Decouple with 1 μF to GNDA. |
| 53 | ADC_VLOW | Input | Analog reference input. ADC low reference voltage. Default: Connect to GNDA with R = 1200 Ω and decouple with C = 100 nF to GNDA. |
| 54 | ADC_GNDA | Ground | Analog ground. ADC analog ground. |
| 55 | ADC_VDDA | Supply | Analog supply voltage. ADC analog supply voltage [3.3 V]. |
| 56 | ADC_GNDD | Ground | Digital ground. ADC digital ground. |
| 57 | ADC_VDDD | Supply | Digital supply voltage. ADC digital supply voltage [3.3 V]. |
| 58 | ADC_CLOCK | Input | Digital input. ADC clock (40 MHz). |
| 59 | ADC_OUT<9> | Output | Digital output. ADC data output (MSB). |
| 60 | ADC_OUT<8> | Output | Digital output. ADC data output. |
| 61 | ADC_OUT<7> | Output | Digital output. ADC data output. |
| 62 | ADC_OUT<6> | Output | Digital output. ADC data output. |
| 63 | ADC_OUT<5> | Output | Digital output. ADC data output. |
| 64 | ADC_OUT<4> | Output | Digital output. ADC data output. |
| 65 | ADC_OUT<3> | Output | Digital output. ADC data output. |
| 66 | ADC_OUT<2> | Output | Digital output. ADC data output. |
| 67 | ADC_OUT<1> | Output | Digital output. ADC data output. |

1. All pins with the same name can be connected together.
2. All digital input are active high (unless mentioned otherwise).
3. Tie all digital inputs that are not used to GND (inactive level).

**Table 26. PIN LIST** (Notes 1, 2 and 3)

| Pin | Pin Name | Pin Type | Pin Description |
|---|---|---|---|
| 68 | ADC_OUT<0> | Output | Digital output. ADC data output (LSB). |
| 69 | ADC_IN | Input | Analog input. ADC analog input. |
| 70 | ADC_CMD | Input | Analog input. Biasing of the input stage of the ADC. Connect to ADC_VDDA with R = 50 kΩ and decouple with C = 100 nF to ADC_GNDA. |
| 71 | ADC_VDDD | Supply | Digital supply voltage. ADC digital supply voltage [3.3 V]. |
| 72 | ADC_GNDA | Ground | Analog ground. ADC analog ground. |
| 73 | ADC_GNDD | Ground | Digital ground. ADC digital ground. |
| 74 | ADC_VDDA | Supply | Analog supply voltage. ADC analog supply voltage [3.3 V]. |
| 75 | ADC_VHIGH | Input | Analog reference input. ADC high reference volt age.Default: Connect to VDDA with R = 360 Ω and decouple with C = 100 nF to GNDA. |
| 76 | VDDR_LEFT | Supply | Analog supply voltage. High reset level [4.5 V]. |
| 77 | VDDH | Supply | Analog supply voltage. High supply voltage for HOLD switches in the image core [4.5 V] |
| 78 | P_DATA<15> | Input | Digital input. Data parallel interface (MSB). |
| 79 | P_DATA<14> | Input | Digital input. Data parallel interface. |
| 80 | P_DATA<13> | Input | Digital input. Data parallel interface. |
| 81 | P_DATA<12> | Input | Digital input. Data parallel interface. |
| 82 | P_DATA<11> | Input | Digital input. Data parallel interface. |
| 83 | P_DATA<10> | Input | Digital input. Data parallel interface. |
| 84 | P_DATA<9> | Input | Digital input. Data parallel interface. |

1. All pins with the same name can be connected together.
2. All digital input are active high (unless mentioned otherwise).
3. Tie all digital inputs that are not used to GND (inactive level).

### Pad Position and Packaging

*Bare Die*

The IBIS5-1300 image sensor has 84 pins, 21 pins on every edge. The die size from pad-edge to pad-edge (without scribe-line) is: 10156.5 μm (x) by 9297.25 μm (y). Scribe lines take about 100 to 150 μm extra on each side. Pin 1 is located in the middle of the left side, indicated by a ‘1’ on the layout. A logo and some identification tags are on the top right of the die.

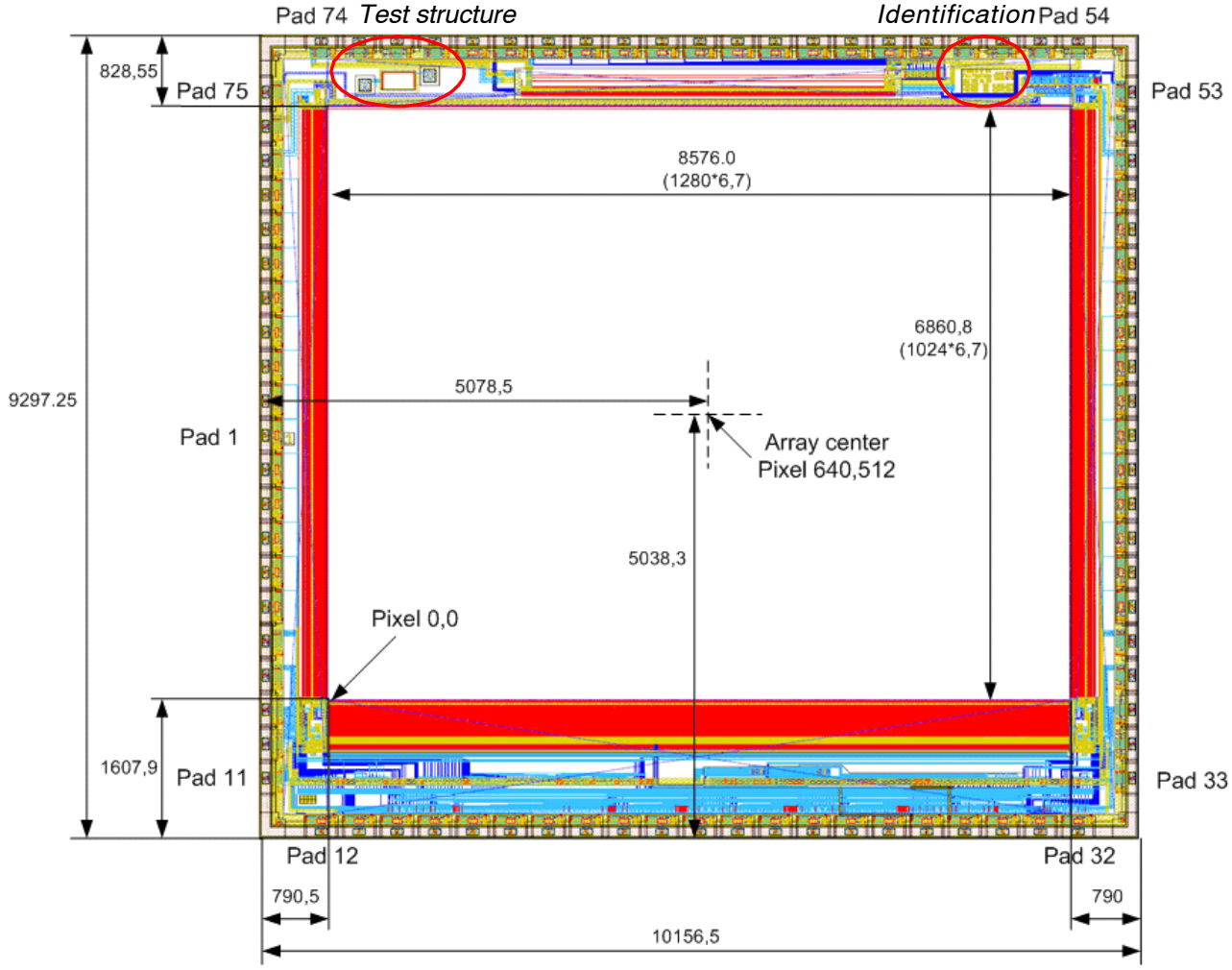
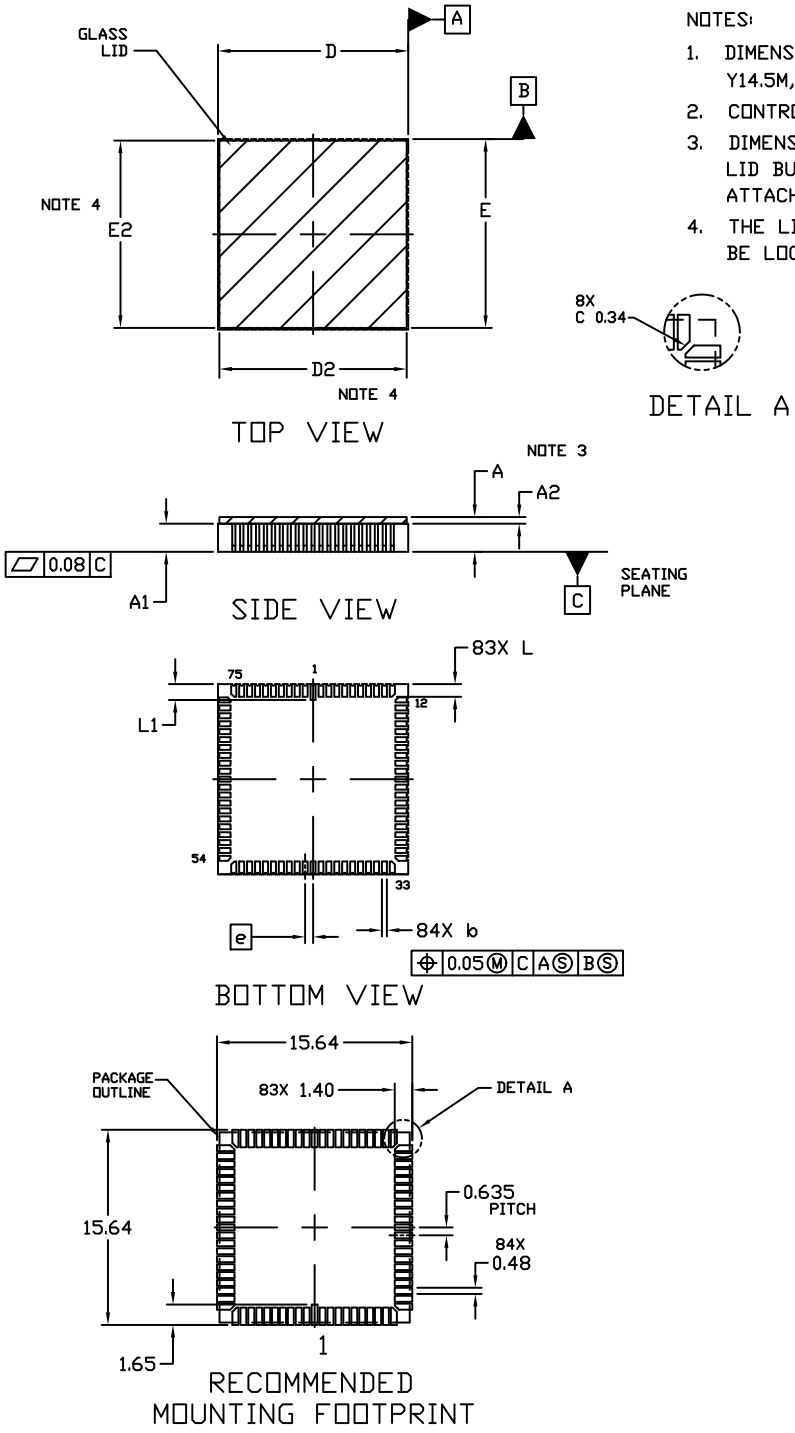



**Figure 29. IBIS5−1300 Bare Die Dimensions (All dimensions in μm)**

**Package Drawing with Glass**

**LCC84, 15.24x15.24**
CASE 115AS−01
ISSUE O

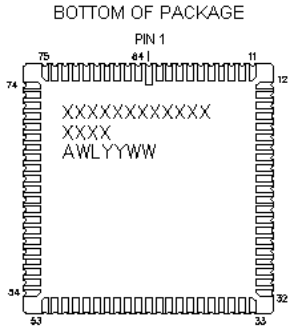



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION A INCLUDES THE PACKAGE BODY AND LID BUT DOES NOT INCLUDE HEATSINKS OR OTHER ATTACHED FEATURES.
4. THE LID DEFINED BY DIMENSIONS D2 AND E2 MUST BE LOCATED WITHIN DIMENSIONS D AND E.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN. | MAX. |
| A | 2.40 | 3.20 |
| A1 | 2.25 REF | |
| A2 | 0.55 REF | |
| b | 0.32 | 0.48 |
| D | 15.06 | 15.42 |
| D2 | 15.00 REF | |
| E | 15.06 | 15.42 |
| E2 | 15.00 REF | |
| e | 0.635 BSC | |
| L | 0.89 | 1.15 |
| L1 | 1.14 | 1.40 |

**GENERIC MARKING DIAGRAM**




XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

**Table 27. MECHANICAL SPECIFICATIONS** (see Package Drawing with Glass on page 30)

| Parameters | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Die (with Pin 1 to the left center, Top View)<br>Pixel (0,0) is bottom left | Die thickness | NA | 0.740 | NA | mm |
| | Die center, X offset to the center of package | –50 | 0 | 50 | μm |
| | Die center, Y offset to the center of the package | –50 | 0 | 50 | μm |
| | Die position, X tilt to the Die Attach Plane | N/A | 1 | N/A | deg |
| | Die position, Y tilt to the Die Attach Plane | N/A | 1 | N/A | deg |
| | Die placement accuracy (referenced to die scribe and lead fingers on package on all four sides) | –50 | 0 | 50 | μm |
| | Die rotation accuracy | –1 | – | 1 | deg |
| | Distance from PCB plane to top of the die surface | – | 1.26 | – | mm |
| | Distance from top of the die surface to top of the glass lid | – | 1.69 | – | mm |
| Glass lid specifications | XY size | – | 15 x 15 | – | mm |
| | Thickness | 0.5 | 0.55 | 0.6 | mm |
| | Spectral range for optical coating of window | 400 | – | 1000 | nm |
| | Reflection coefficient for window (refer to Figure 31) | – | <0.8 | | % |
| Mechanical shock | JESD22-B104C; Condition G | – | – | 2000 | G |
| Vibration | JESD22-B103B; Condition 1 | 20 | – | 2000 | Hz |
| Mounting profile | Reflow profile according to J-STD-020D.1 | – | – | 260 | °C |

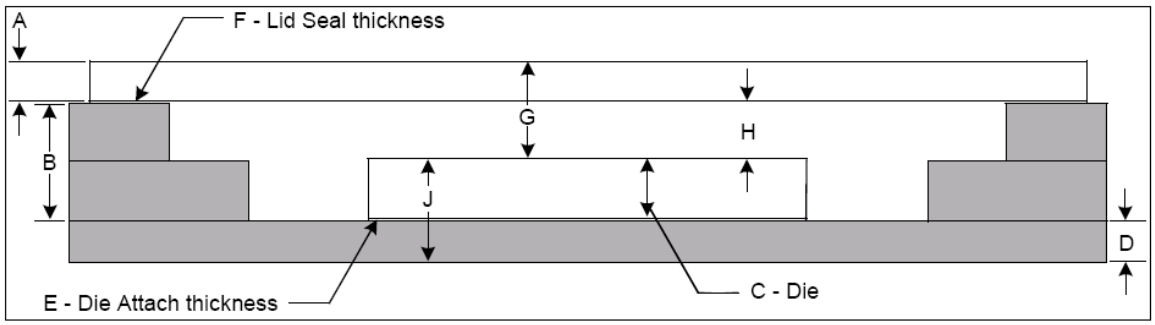



**Figure 30. Side View Dimensions**

### Glass Lid

The IBIS5-1300 image sensor uses a glass lid without any coatings. Figure 31 shows the transmission characteristics of the glass lid. As seen in Figure 31, the sensor does not use infrared attenuating color filter glass. Provide a filter in the optical path when using color devices.

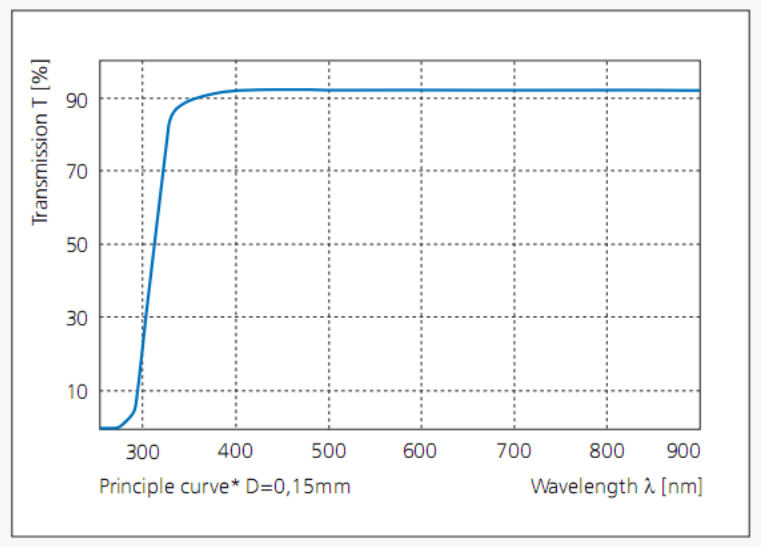



**Figure 31. Transmission Characteristics of Glass Lid**

## HANDLING PRECAUTIONS

For proper handling and storage conditions, refer to the ON Semiconductor application note AN52561.

*Information on Pb-Free Soldering*

IBIS5-1300 product was tested successfully for Pb-free soldering processes, using a reflow temperature profile with maximum 260°C, minimum 40 s at 255°C and minimum 90 s at 217°C.

## LIMITED WARRANTY

ON Semiconductor Image Sensor Business Unit warrants that the image sensor products to be delivered hereunder, if properly used and serviced, will conform to Seller's published specifications and will be free from defects in material and workmanship for two (2) years following the date of shipment. If a defect were to manifest itself within two (2) year period from the sale date, ON Semiconductor will either replace the product or give credit for the product.

### Return Material Authorization (RMA)

ON Semiconductor packages all of its image sensor products in a clean room environment under strict handling procedures and ships all image sensor products in ESD-safe, clean-room-approved shipping containers. Products returned to ON Semiconductor for failure analysis should be handled under these same conditions and packed in its original packing materials, or the customer may be liable for the product.

### RoHS (Pb-free) Compliance

This paragraph reports the use of hazardous chemical substances as required by the RoHS Directive (excluding packing material).

Lead, Cadmium, Mercury Hexavalent Chromium, PBB (Polybrominated biphenyls), PBDE (Polybrominated diphenyl ethers), noted as 'intentional content': is not available in the IBIS5-1300.

NOTE: 'Intentional content' is defined as any material demanding special attention that is allowed into the product as follows:

- A chemical composition is added into the inquired product intentionally to produce and maintain the required performance and function of the product.
- A chemical composition which is used intentionally in the manufacturing process, that is allowed into the product.

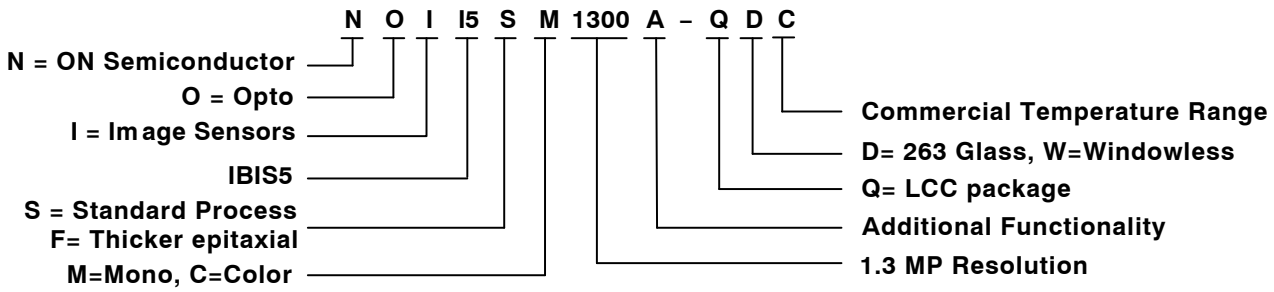
The following case is ***not*** treated as 'intentional content':

- The above material is contained as an impurity into raw materials or parts of the intended product. The impurity is defined as a substance that cannot be removed industrially, or it is produced using a process such as chemical composing or reaction, and it cannot be removed technically.

## ACCEPTANCE CRITERIA SPECIFICATION

The Product Acceptance Criteria is available on request. This document contains the criteria to which the IBIS5-1300 is tested before being shipped.

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