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NCV7517

FLEXMOS™ Hex Low-Side MOSFET Pre-Driver

The NCV7517 programmable six channel low−side MOSFET pre−driver is one of a family of FLEXMOS™ automotive grade products for driving logic−level MOSFETs. The product is controllable by a combination of serial SPI and parallel inputs. It features programmable fault management modes and allows power−limiting PWM operation with programmable refresh time. The device offers 3.3 V/5.0 V compatible inputs and the serial output driver can be powered from either 3.3 V or 5.0 V. Power−on reset provides controlled powerup and two enable inputs allow all outputs to be simultaneously disabled.

Each channel independently monitors its external MOSFET's drain voltage for fault conditions. Shorted load fault detection thresholds are fully programmable using an externally programmed reference voltage and a combination of four discrete internal ratio values. The ratio values are SPI selectable and allow different detection thresholds for each group of three output channels.

Fault information for each channel is 2−bit encoded by fault type and is available through SPI communication. Fault recovery operation for each channel is programmable and may be selected for latch−off or automatic retry.

The FLEXMOS family of products offers application scalability through choice of external MOSFETs.

Features

- 16−Bit SPI with Frame Error Detection
- 3.3 V/5.0 V Compatible Parallel and Serial Control Inputs
- 3.3 V/5.0 V Compatible Serial Output Driver
- Two Enable Inputs
- Open−Drain Fault and Status Flags
- Programmable
  - Shorted Load Fault Detection Thresholds
  - Fault Recovery Mode
  - Fault Retry Timer
  - Flag Masking
- Load Diagnostics with Latched Unique Fault Type Data
  - Shorted Load
  - Open Load
  - Short to GND
- NCV Prefix for Automotive and Other Applications Requiring Site and Change Controls
- These are Pb−Free Devices*

Benefits

- Scalable to Load by Choice of External MOSFET

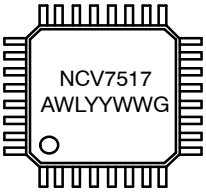
ON Semiconductor®

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MARKING DIAGRAM



32 LEAD LQFP
FT SUFFIX
CASE 873A



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NCV7517FTG	LQFP (Pb−Free)	250 Units/Tray
NCV7517FTR2G	LQFP (Pb−Free)	2000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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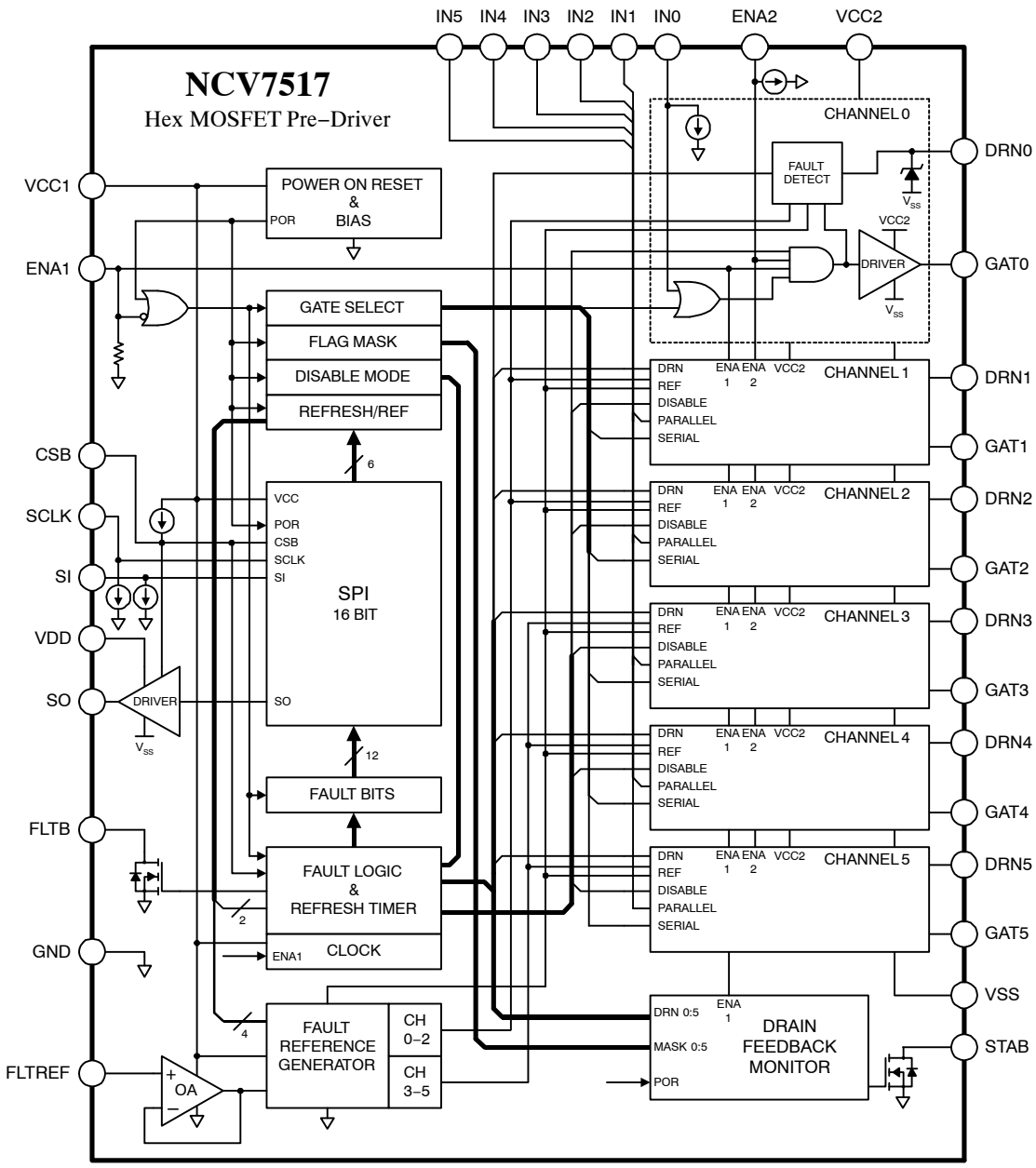


Figure 1. Block Diagram

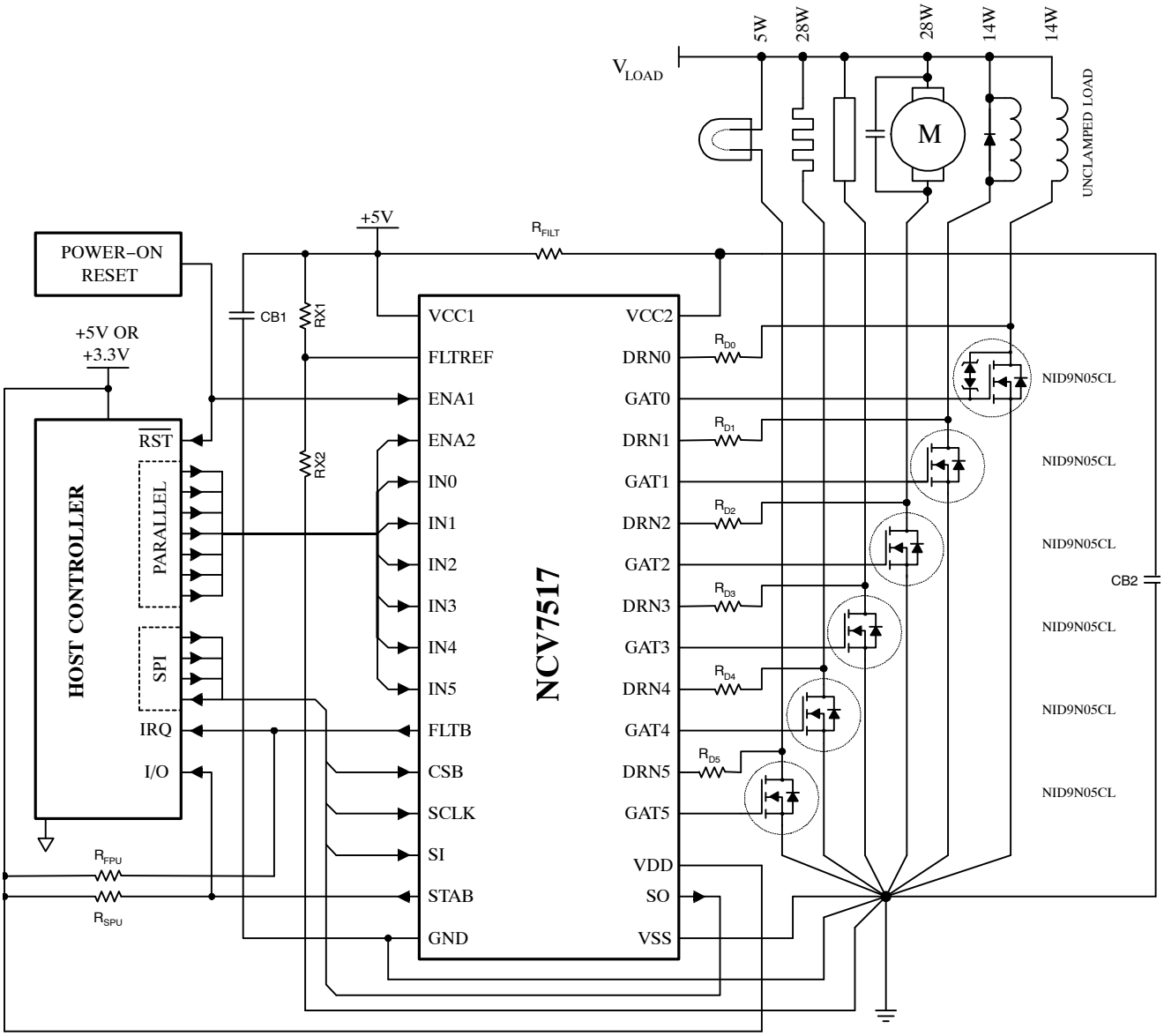


Figure 2. Application Diagram

PIN FUNCTION DESCRIPTION

Symbol	Description
FLTREF	Analog Fault Detect Threshold: 5.0 V Compliant
DRN0 – DRN5	Analog Drain Feedback: Internally Clamped
GAT0 – GAT5	Analog Gate Drive: 5.0 V Compliant
ENA1, ENA2	Digital Master Enable Inputs: 3.3 V/5.0 V (TTL) Compatible
IN0 – IN5	Digital Parallel Input: 3.3 V/5.0 V (TTL) Compatible
CSB	Digital Chip Select Input: 3.3 V/5.0 V (TTL) Compatible
SCLK	Digital Shift Clock Input: 3.3 V/5.0 V (TTL) Compatible
SI	Digital Serial Data Input: 3.3 V/5.0 V (TTL) Compatible
SO	Digital Serial Data Output: 3.3 V/5.0 V Compliant
STAB	Digital Open−Drain Output: 3.3 V/5.0 V Compliant
FLTB	Digital Open−Drain Output: 3.3 V/5.0 V Compliant
VCC1	Power Supply – Low Power Path
GND	Power Return – Low Power Path – Device Substrate
VCC2	Power Supply – Gate Drivers
VDD	Power Supply – Serial Output Driver
VSS	Power Return – VCC2, VDD, Drain Clamps

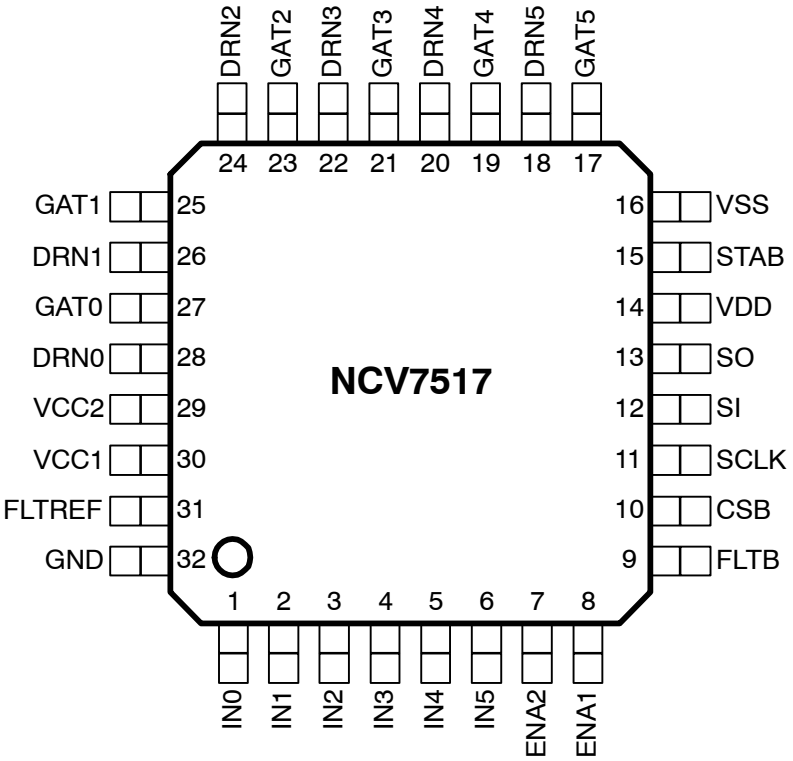


Figure 3. 32 Pin LQFP Pinout (Top View)

MAXIMUM RATINGS (Voltages are with respect to device substrate.)

Rating	Value	Unit
DC Supply (V_{CC1}, V_{CC2}, V_{DD})	−0.3 to 6.5	V
Difference Between V_{CC1} and V_{CC2}	±0.3	V
Difference Between GND (Substrate) and V_{SS}	±0.3	V
Output Voltage (Any Output)	−0.3 to 6.5	V
Drain Feedback Clamp Voltage (Note 1)	−0.3 to 40	V
Drain Feedback Clamp Current (Note 1)	10	mA
Input Voltage (Any Input)	−0.3 to 6.5	V
Junction Temperature, T_J	−40 to 150	°C
Storage Temperature, T_{STG}	−65 to 150	°C
Peak Reflow Soldering Temperature: Lead−Free 60 to 150 seconds at 217°C (Note 2)	260 peak	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

ATTRIBUTES

Characteristic	Value
ESD Capability Human Body Model Machine Model	 ≥ ± 2.0 kV ≥ ± 200 V
Moisture Sensitivity (Note 2)	MSL3
Package Thermal Resistance (Note 3) Junction−to−Ambient, $R_{\theta JA}$ Junction−to−Pin, $R_{\Psi JL}$	 86.0 °C/W 58.5 °C/W

1. An external series resistor must be connected between the MOSFET drain and the feedback input in the application. Total clamp power dissipation is limited by the maximum junction temperature, the application environment temperature, and the package thermal resistances.
2. For additional information, see or download ON Semiconductor's Soldering and Mounting Techniques Reference Manual, SOLDERRM/D, and Application Note AND8003/D.
3. Values represent still air steady−state thermal performance on a 4 layer (42 x 42 x 1.5 mm) PCB with 1 oz. copper on an FR4 substrate, using a minimum width signal trace pattern (384 mm^2 trace area).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC1}	Main Power Supply Voltage	4.75	5.25	V
V_{CC2}	Gate Drivers Power Supply Voltage	V_{CC1} − 0.3	V_{CC1} + 0.3	V
V_{DD}	Serial Output Driver Power Supply Voltage	3.0	V_{CC1}	V
V_{IN} High	Logic High Input Voltage	2.0	V_{CC1}	V
V_{IN} Low	Logic Low Input Voltage	0	0.8	V
T_A	Ambient Still−Air Operating Temperature	−40	125	°C

ELECTRICAL CHARACTERISTICS ($4.75\ V \le V_{CCX} \le 5.25\ V$, $V_{DD} = V_{CCX}$, $-40°C \le T_J \le 125°C$, unless otherwise specified.) (Note 4)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
V_{CC1} Supply						
Operating Current – V_{CC1} = 5.25 V, V_{FLTREF} = 1.0 V		ENA_X = 0 $ENA_1 = ENA_2 = V_{CC1}$, V_{DRNX} = 0 V, GAT_X drivers off $ENA_1 = ENA_2 = V_{CC1}$, GAT_X drivers on	– – –	2.80 3.10 2.80	5.0 5.0 5.0	mA
Power–On Reset Threshold		V_{CC1} Rising	3.65	4.20	4.60	V
Power–On Reset Hysteresis		–	0.150	0.385	–	V
Digital I/O						
V_{IN} High		ENA_X, IN_X, SI, SCLK, CSB	2.0	–	–	V
V_{IN} Low		ENA_X, IN_X, SI, SCLK, CSB	–	–	0.8	V
V_{IN} Hysteresis		ENA_X, IN_X, SI, SCLK, CSB	100	330	500	mV
Input Pullup Current		CSB V_{IN} = 0 V	–25	–10	–	μA
Input Pulldown Current		ENA2, IN_X, SI, SCLK, $V_{IN} = V_{CC1}$	–	10	25	μA
Input Pulldown Resistance		ENA1	100	150	200	kΩ
SO Low Voltage		V_{DD} = 3.3 V, I_{SINK} = 5.0 mA	–	0.11	0.25	V
SO High Voltage		V_{DD} = 3.3 V, I_{SOURCE} = 5.0 mA	V_{DD} – 0.25	V_{DD} – 0.11	–	V
SO Output Resistance		Output High or Low	–	22	–	Ω
SO Tri–State Leakage Current		CSB = 3.3 V	–10	–	10	μA
STAB Low Voltage		STAB Active, I_{STAB} = 1.25 mA	–	0.1	0.25	V
STAB Leakage Current		$V_{STAB} = V_{CC1}$	–	–	10	μA
FLTB Low Voltage		FLTB Active, I_{FLTB} = 1.25 mA	–	0.1	0.25	V
FLTB Leakage Current		$V_{FLTB} = V_{CC1}$	–	–	10	μA
Fault Detection – GAT_X ON						
FLTREF Input Current		V_{FLTREF} = 0 V	–1.0	–	–	μA
FLTREF Input Linear Range		(Note 5)	0	–	V_{CC1} – 2.0	V
FLTREF Op–amp V_{CC1} PSRR		(Note 5)	30	–	–	dB
DRN_X Clamp Voltage	V_{CL}	I_{DRNX} = 10 μA $I_{DRNX} = I_{CL(MAX)}$ = 10 mA	27 –	32 33.6	– 37	V
DRN_X Shorted Load Threshold GAT_X Output High V_{FLTREF} = 1.0 V		Register 2: R_1 = 0, R_0 = 0 or R_4 = 0, R_3 = 0	20	25	30	% V_{FLTREF}
		Register 2: R_1 = 0, R_0 = 1 or R_4 = 0, R_3 = 1	45	50	55	% V_{FLTREF}
		Register 2: R_1 = 1, R_0 = 0 or R_4 = 1, R_3 = 0	70	75	80	% V_{FLTREF}
		Register 2: R_1 = 1, R_0 = 1 or R_4 = 1, R_3 = 1	95	100	105	% V_{FLTREF}
DRN_X Input Leakage Current		$V_{CC1} = V_{CC2} = V_{DD}$ = 5.0 V, $ENA_X = IN_X$ = 0 V, $V_{DRNX} = V_{CL(MIN)}$ $V_{CC1} = V_{CC2} = V_{DD}$ = 0 V, $ENA_X = IN_X$ = 0 V, $V_{DRNX} = V_{CL(MIN)}$	–1.0	–	1.0	μA

4. Designed to meet these characteristics over the stated voltage and temperature recommended operating ranges, though may not be 100% parametrically tested in production.
5. Guaranteed by design.

ELECTRICAL CHARACTERISTICS (continued) (4.75 V ≤ V_{CCX} ≤ 5.25 V, V_{DD} = V_{CCX}, −40°C ≤ T_J ≤ 125°C, unless otherwise specified.) (Note 6)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
Fault Detection – GAT_X OFF						
DRN_X Diagnostic Current	I_{SG}	Short to GND Detection, V_{DRNX} = 0.30 V_{CC1}	−27	−20	−10	μA
	I_{OL}	Open Load Detection, V_{DRNX} = 0.75 V_{CC1}	30	60	80	μA
DRN_X Fault Threshold Voltage	V_{SG}	Short to GND Detection	27	30	33	%V_{CC1}
	V_{OL}	Open Load Detection	72	75	78	%V_{CC1}
DRN_X Off State Bias Voltage	V_{CTR}	–	–	50	–	%V_{CC1}
Gate Driver Outputs						
GAT_X Output Resistance		Output High or Low	200	350	500	Ω
GAT_X High Output Current		V_{GATX} = 0 V	−26.25	–	−9.5	mA
GAT_X Low Output Current		V_{GATX} = V_{CC2}	9.5	–	26.25	mA
Turn−On Propagation Delay	$t_{P(ON)}$	IN_X to GAT_X (Figure 4)	–	–	1.0	μs
		CSB to GAT_X (Figure 5)				
Turn−Off Propagation Delay	$t_{P(OFF)}$	IN_X to GAT_X (Figure 4)	–	–	1.0	μs
		CSB to GAT_X (Figure 5)				
Output Rise Time	t_R	20% to 80% of V_{CC2}, C_{LOAD} = 400 pF (Figure 4, Note 5)	–	–	277	ns
Output Fall Time	t_F	80% to 20% of V_{CC2}, C_{LOAD} = 400 pF (Figure 4, Note 5)	–	–	277	ns
Fault Timers						
Channel Fault Blanking Timer	$t_{BL(ON)}$	V_{DRNX} = 5.0 V; IN_X rising to FLTB falling (Figure 6)	11	21	31	μs
	$t_{BL(OFF)}$	V_{DRNX} = 0 V; IN_X falling to FLTB falling (Figure 6)	90	120	150	μs
Channel Fault Filter Timer	t_{FF}	Figure 7	7.0	12	17	μs
Global Fault Refresh Timer (Auto−retry Mode)	t_{FR}	Register 2: Bit R_2 = 0 or R_5 = 0	7.5	10	12.5	ms
		Register 2: Bit R_2 = 1 or R_5 = 1	30	40	50	ms
Timer Clock		ENA1 = 1	–	500	–	kHz
Serial Peripheral Interface (Figure 9) V_{ccx} = 5.0 V, V_{DD} = 3.3 V, F_{SCLK} = 4.0 MHz, C_{LOAD} = 200 pF						
SO Supply Voltage	V_{DD}	3.3 V Interface	3.0	3.3	3.6	V
		5.0 V Interface	4.5	5.0	5.5	V
SCLK Clock Period		–	–	250	–	ns
Maximum Input Capacitance		SI, SCLK (Note 7)	–	–	12	pF
SCLK High Time		SCLK = 2.0 V to 2.0 V	125	–	–	ns
SCLK Low Time		SCLK = 0.8 V to 0.8 V	125	–	–	ns
SI Setup Time		SI = 0.8 V/2.0 V to SCLK = 2.0 V (Note 7)	25	–	–	ns
SI Hold Time		SCLK = 2.0 V to SI = 0.8 V/2.0 V (Note 7)	25	–	–	ns

6. Designed to meet these characteristics over the stated voltage and temperature recommended operating ranges, though may not be 100% parametrically tested in production.
7. Guaranteed by design.

ELECTRICAL CHARACTERISTICS (continued) (4.75 V ≤ V_{CCX} ≤ 5.25 V, V_{DD} = V_{CCX}, −40°C ≤ T_J ≤ 125°C, unless otherwise specified.) (Note 8)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
Serial Peripheral Interface (continued) (Figure 9) V_{ccx} = 5.0 V, V_{DD} = 3.3 V, F_{SCLK} = 4.0 MHz, C_{LOAD} = 200 pF						
SO Rise Time		(20% V_{SO} to 80% V_{DD}) C_{LOAD} = 200 pF (Note 9)	–	25	50	ns
SO Fall Time		(80% V_{SO} to 20% V_{DD}) C_{LOAD} = 200 pF (Note 9)	–	–	50	ns
CSB Setup Time		CSB = 0.8 V to SCLK = 2.0 V (Note 9)	60	–	–	ns
CSB Hold Time		SCLK = 0.8 V to CSB = 2.0 V (Note 9)	75	–	–	ns
CSB to SO Time		CSB = 0.8 V to SO Data Valid (Note 9)	–	65	125	ns
SO Delay Time		SCLK = 0.8 V to SO Data Valid (Note 9)	–	65	125	ns
Transfer Delay Time		CSB Rising Edge to Next Falling Edge (Note 9)	1.0	–	–	μs

8. Designed to meet these characteristics over the stated voltage and temperature recommended operating ranges, though may not be 100% parametrically tested in production.
9. Guaranteed by design.

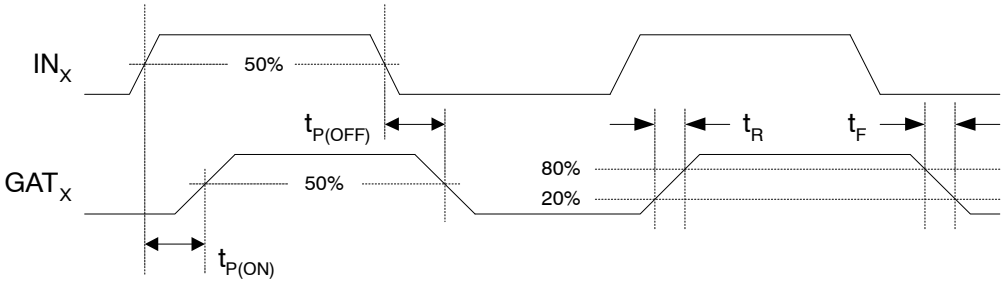


Figure 4. Gate Driver Timing Diagram – Parallel Input

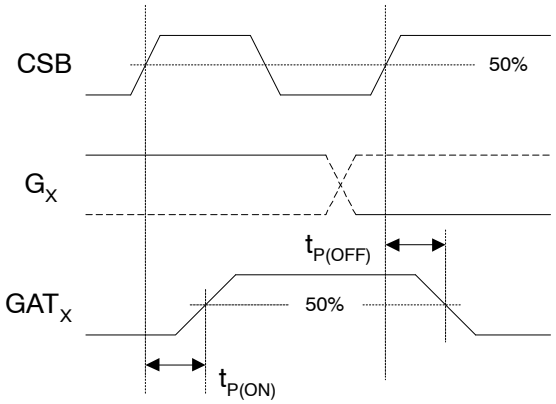


Figure 5. Gate Driver Timing Diagram – Serial Input

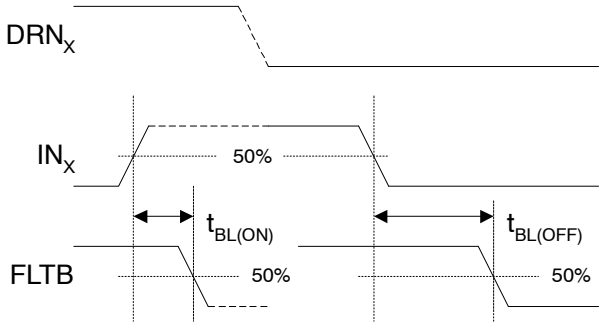


Figure 6. Blanking Timing Diagram

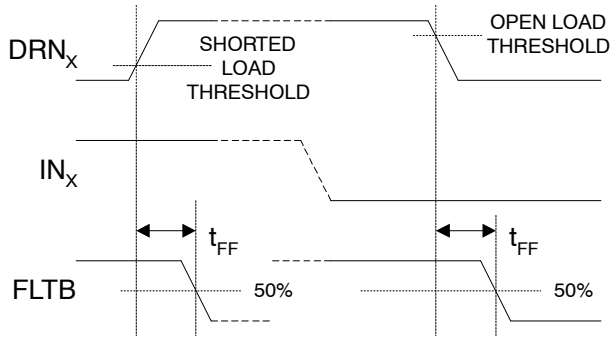


Figure 7. Filter Timing Diagram

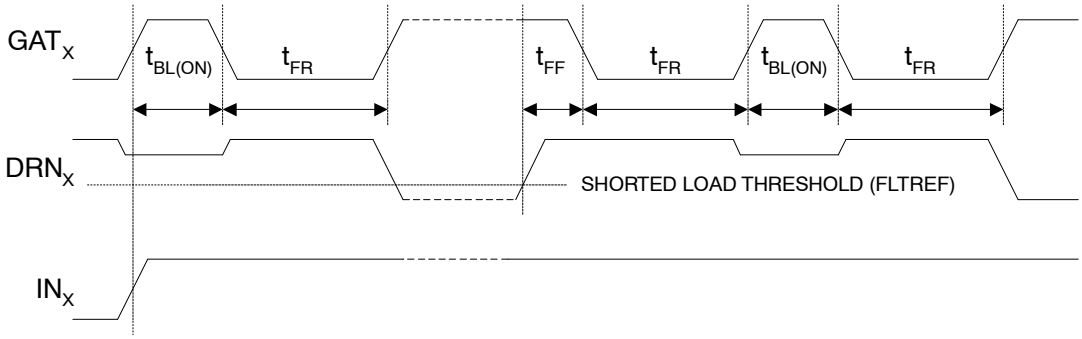
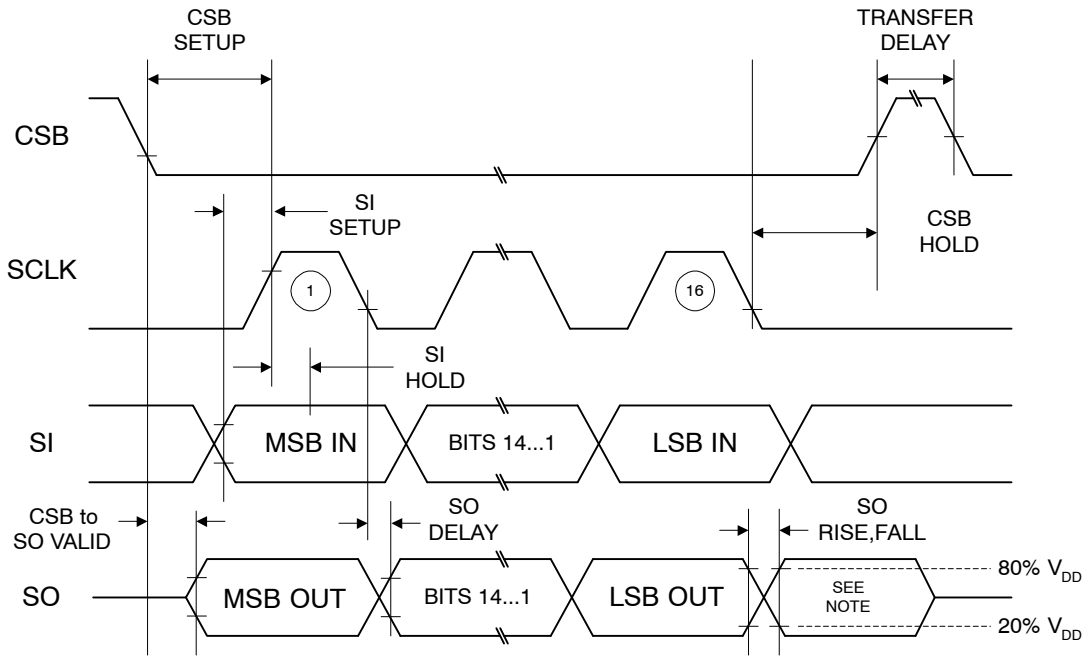


Figure 8. Fault Refresh Timing Diagram



Note: Not defined but usually MSB of data just received.

Figure 9. SPI Timing Diagram

DETAILED OPERATING DESCRIPTION

General

The NCV7517 is a six channel general purpose low−side pre−driver for controlling and protecting N−type logic level MOSFETs. While specifically designed for driving MOSFETs with resistive, inductive or lamp loads in automotive applications, the device is also suitable for industrial and commercial applications. Programmable fault detection and protection modes allow the NCV7517 to accommodate a wide range of external MOSFETs and loads, providing the user with flexible application solutions. Separate power supply pins are provided for low and high current paths to improve analog accuracy and digital signal integrity. ON Semiconductor's SMARTDISCRETES™ clamp MOSFETs, such as the NID9N05CL, are recommended when driving unclamped inductive loads.

Power Up/Down Control

The NCV7517's powerup/down control prevents spurious output operation by monitoring the V_{CC1} power supply. An internal Power−On Reset (POR) circuit causes all GAT_X outputs to be held low until sufficient voltage is available to allow proper control of the device. All internal registers are initialized to their default states, fault data is cleared, and the open−drain fault (FLTB) and status (STAB) flags are disabled.

When V_{CC1} exceeds the POR threshold, outputs and flags are enabled and the device is ready to accept input data. When V_{CC1} falls below the POR threshold during power down, flags are reset and disabled and all GAT_X outputs are driven and held low until V_{CC1} falls below about 0.7 V.

SPI Communication

The NCV7517 is a 16−bit SPI slave device. SPI communication between the host and the NCV7517 may either be parallel via individual CSB addressing or daisy−chained through other devices using a compatible SPI protocol.

The active−low CSB chip select input has a pullup current source. The SI and SCLK inputs have pulldown current sources. The recommended idle state for SCLK is low. The tri−state SO line driver can be supplied with either 3.3 or 5.0 V and is powered via the device's V_{DD} and V_{SS} pins.

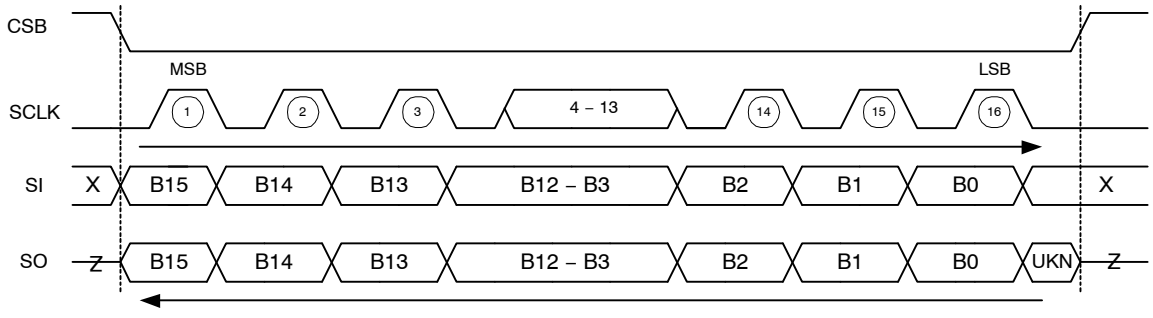
The NCV7517 employs frame error detection that requires integer multiples of 16 SCLK cycles during each CSB high−low−high cycle (valid communication frame.) A frame error does not affect the flags. The CSB input controls SPI data transfer and initializes the selected device's frame error and fault reporting logic.

The host initiates communication when a selected device's CSB pin goes low. Output (fault) data is simultaneously sent MSB first from the SO pin while input (command) data is received MSB first at the SI pin under synchronous control of the master's SCLK signal while CSB is held low (Figure 10). Fault data changes on the falling edge of SCLK and is guaranteed valid before the next rising edge of SCLK. Command data received must be valid before the rising edge of SCLK.

When CSB goes low, frame error detection is initialized, latched fault data is transferred to the SPI, and the FLTB flag is disabled and reset if previously set. Data for faults detected while CSB is low are ignored but will be captured if still present after CSB goes high.

If a valid frame has been received when CSB goes high, the last multiple of 16 bits received is decoded into command data, and FLTB is re−enabled. Latched (previous) fault data is cleared and current fault data is captured. The FLTB flag will be set if a fault is detected.

If a frame error is detected when CSB goes high, new command data is ignored, and previous fault data remains latched and available for retrieval during the next valid frame. The FLTB flag will be set if a fault (not a frame error) is detected.



Note: X=Don't Care, Z=Tri−State, UKN=Unknown Data

Figure 10. SPI Communication Frame Format

Serial Data and Register Structure

The 16−bit data sent by the NCV7517 is always the encoded 12−bit fault information, with the upper 4 bits forced to zero. The 16−bit data received is decoded into a 4−bit address and a 6−bit data word (see Figure 11). The upper four bits, beginning with the received MSB, are fully decoded to address one of four programmable registers and the lower six bits are decoded into data for the addressed register. Bit B15 must always be set to zero. The valid register addresses are shown in Table 1. Each register is next described in detail.

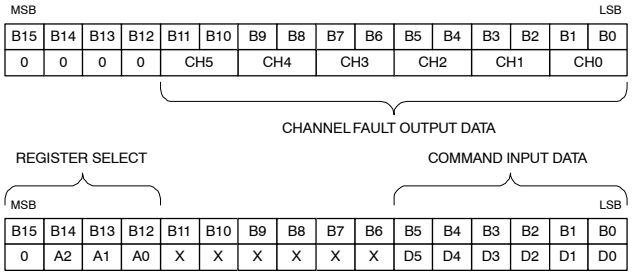


Figure 11. SPI Data Format

Table 1. Register Address Definitions

4−BIT ADDRESS				6−BIT INPUT DATA					
B_{15}	A_2	A_1	A_0	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	Gate Select					
0	0	0	1	Disable Mode					
0	0	1	0	Refresh & Reference					
0	0	1	1	Flag Mask					
0	1	X	X	Null					
16−BIT OUTPUT DATA									
B_{15}	B_{14}	B_{13}	B_{12}	B_{11}					B_0
0	0	0	0	D_{11}	12−bit Fault Data				D_0

Gate Select – Register 0

Each GAT_X output is turned on/off by programming its respective G_X bit (see Table 2). Setting a bit to 1 causes the selected GAT_X output to drive its external MOSFET's gate to V_{CC2} (ON). Setting a bit to 0 causes the selected GAT_X output to drive its external MOSFET's gate to V_{SS} (OFF). Note that the actual state of the output depends on POR, ENA_X and shorted load fault states as later defined by Equation 1. At powerup, each bit is set to 0 (all outputs OFF).

Table 2. Gate Select Register

A_2	A_1	A_0	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	G_5	G_4	G_3	G_2	G_1	G_0
			0 = GAT_X OFF 1 = GAT_X ON					

Disable Mode – Register 1

The disable mode for shorted load faults is controlled by each channel's respective M_X bit (see Table 3). Setting a bit to 1 causes the selected GAT_X output to latch−off when a fault is detected. Setting a bit to 0 causes the selected GAT_X output to auto−retry when a fault is detected. At powerup, each bit is set to 0 (all outputs in auto−retry mode).

Table 3. Disable Mode Register

A_2	A_1	A_0	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	M_5	M_4	M_3	M_2	M_1	M_0
			0 = AUTO−RETRY 1 = LATCH OFF					

Refresh and Reference – Register 2

Refresh time (auto−retry mode) and shorted load fault detection references are programmable in two groups of three channels. Refresh time and the fault reference for channels 5−3 is programmed by R_X bits 5−3. Refresh time and the fault reference for channels 2−0 is programmed by R_X bits 2−0 (see Table 4). At powerup, each bit is set to 0 (V_{FLT} = 25% V_{FLTREF}, t_{FR} = 10 ms).

Table 4. Refresh and Reference Register

A_2	A_1	A_0	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	R_5	R_4	R_3	R_2	R_1	R_0
			CHANNELS 5–3			CHANNELS 2–0		
25% V_{FLTREF}			X	0	0	X	0	0
50% V_{FLTREF}			X	0	1	X	0	1
75% V_{FLTREF}			X	1	0	X	1	0
V_{FLTREF}			X	1	1	X	1	1
t_{FR} = 10 ms			X	X	X	0	X	X
t_{FR} = 40 ms			X	X	X	1	X	X
t_{FR} = 10 ms			0	X	X	X	X	X
t_{FR} = 40 ms			1	X	X	X	X	X

Flag Mask – Register 3

The drain feedback from each channel's DRN_X input is combined with the channel's K_X mask bit (Table 5). When K_X = 1, a channel's mask is cleared and its feedback to the FLTB and STAB flags is enabled. At powerup, each bit is set to 0 (all masks set).

Table 5. Flag Mask Register

A_2	A_1	A_0	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	K_5	K_4	K_3	K_2	K_1	K_0
			0 = MASK SET 1 = MASK CLEAR					

The STAB flag is influenced when a mask bit changes CLR→SET after one valid SPI frame. FLTB is influenced after two valid SPI frames. This is correct behavior for FLTB since, while a fault persists, the FLTB will be set *when* CSB goes LO→HI at the end of an SPI frame. The mask instruction is decoded *after* CSB goes LO→HI so FLTB will only reflect the mask bit change after the next SPI frame. Both FLTB and STAB require only one valid SPI frame when a mask bit changes SET→CLR.

Null Register – Register 4

Fault information is always returned when any register is addressed. The null register (Table 6) provides a way to read back fault information without regard to the content of D_X.

Table 6. Null Register

A_2	A_1	A_0	D_5	D_4	D_3	D_2	D_1	D_0
1	X	X	X	X	X	X	X	X

Gate Driver Control and Enable

Each GAT_X output may be turned on by either its respective parallel IN_X input or the internal G_X (Gate Select) register bit via SPI communication. The device's common ENA_X enable inputs can be used to implement global control functions, such as system reset, overvoltage or input override by a watchdog controller. Each parallel input and the ENA2 input have individual internal pulldown current sources. The ENA1 input has an internal pulldown resistor. Unused parallel inputs should be connected to GND and unused enable inputs should be connected to V_{CC1}. Parallel input is recommended when low frequency ($\leq$ 2.0 kHz) PWM operation of the outputs is desired.

ENA2 disables all GAT_X outputs when brought low. When ENA1 is brought low, all GAT_X outputs, the timer clock, and the flags are disabled. The fault and gate registers are cleared and the flags are reset. New serial G_X data is ignored while ENA1 is low but other registers can be programmed.

When both the ENA1 and ENA2 inputs are high, the outputs will reflect the current parallel or serial input states. This allows ENA1 to be used to perform a soft reset and ENA2 to be used to disable the GAT_X outputs during initialization of the NCV7517.

The IN_X input state and the G_X register bit data are logically combined with the internal (active low) power−on reset signal (POR), the ENA_X input states, and the shorted load state ($SHRT_X$) to control the corresponding GAT_X output such that:

$$GAT_X = POR \cdot ENA1 \cdot ENA2 \cdot \overline{SHRT_X} \cdot (IN_X + G_X) \quad \text{(eq. 1)}$$

The GAT_X state truth table is given in Table 7.

Table 7. Gate Driver Truth Table

POR	ENA1	ENA2	$SHRT_X$	IN_X	G_X	GAT_X
0	X	X	X	X	X	L
1	0	0	X	X	X	L
1	0	1	X	X	X	L
1	1	0	X	X	X	L
1	1	1	1	0	0	L
1	1	1	1	1	X	H
1	1	1	1	X	1	H
1	1	1	0	X	X	L
1	1→0	1	X	X	→0	→L
1	1	1→0	X	X	G_X	→L
1	1	0→1	X	0	G_X	→G_X

Gate Drivers

The non−inverting GAT_X drivers are symmetrical resistive switches (350 Ω typ.) to the V_{CC2} and V_{SS} voltages. While the outputs are designed to provide symmetrical gate drive to an external MOSFET, load current switching symmetry is dependent on the characteristics of the external MOSFET and its load. Figure 12 shows the gate driver block diagram.

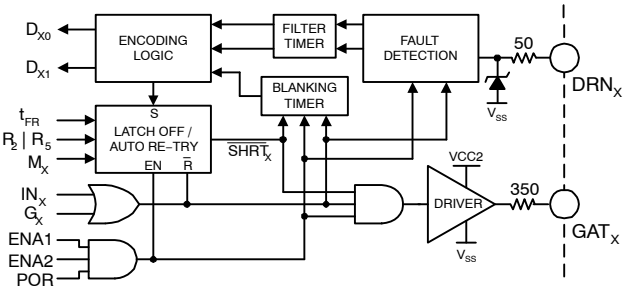


Figure 12. Gate Driver Channel

Fault Diagnostics and Behavior

Each channel has independent fault diagnostics and employs blanking and filter timers to suppress false faults. An external MOSFET is monitored for fault conditions by connecting its drain to a channel's DRN_X feedback input through an external series resistor.

When either ENA1 or ENA2 is low, diagnostics are disabled. When both ENA1 and ENA2 are high, diagnostics are enabled.

Shorted load (or short to V_{LOAD}) faults can be detected when a driver is on. Open load or short to GND faults can be detected when a driver is off.

On−state faults will initiate MOSFET protection behavior, set the FLTB flag and the respective channel's D_X bits in the device's fault latches. Off−state faults will simply set the FLTB flag and the channel's D_X bits.

Fault types are uniquely encoded in a 2−bit per channel format. Fault information for all channels simultaneously is retrieved by SPI read (Figure 11). Table 8 shows the fault−encoding scheme for channel 0. The remaining channels are identically encoded.

Table 8. Fault Data Encoding

CHANNEL 0		STATUS
D_1	D_0	
0	0	NO FAULT
0	1	OPEN LOAD
1	0	SHORT TO GND
1	1	SHORTED LOAD

Blanking and Filter Timers

Blanking timers are used to allow drain feedback to stabilize after a channel is commanded to change states. Filter timers are used to suppress glitches while a channel is in a stable state.

A turn−on blanking timer is started when a channel is commanded on. Drain feedback is sampled after $t_{BL(ON)}$. A turn−off blanking timer is started when a channel is commanded off. Drain feedback is sampled after $t_{BL(OFF)}$.

A filter timer is started when a channel is in a stable state and a fault detection threshold associated with that state has been crossed. Drain feedback is sampled after t_{FF}.

Blanking timers for all channels are started when both ENA1 and ENA2 go high or when either ENA_X goes high while the other is high. The blanking time for each channel depends on the commanded state when ENA_X goes high.

While each channel has independent blanking and filter timers, the parameters for the $t_{BL(ON)}$, $t_{BL(OFF)}$, and t_{FF} times are the same for all channels.

Shorted Load Detection

An external reference voltage applied to the FLTREF input serves as a common reference for all channels (Figure 13). The FLTREF voltage must be within the range of 0 to V_{CC1}−2.0 V and can be derived via a voltage divider between V_{CC1} and GND.

Shorted load detection thresholds can be programmed via SPI in four 25% increments that are ratiometric to the applied FLTREF voltage. Separate thresholds can be selected for channels 0−2 and for channels 3−5 (Table 4).

A shorted load fault is detected when a channel's DRN_X feedback is greater than its selected fault reference after either the turn−on blanking or the filter has timed out.

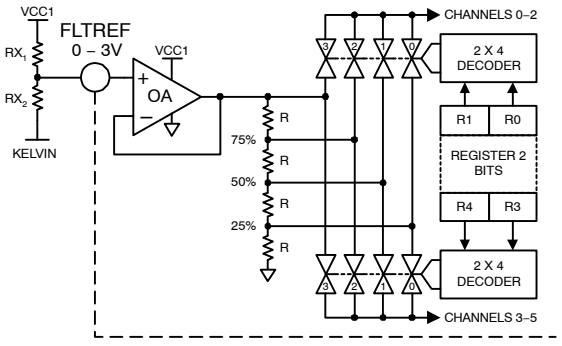


Figure 13. Shorted Load Reference Generator

Shorted Load Fault Recovery

Shorted load fault disable mode for each channel is individually SPI programmable via the M_X bits in the device's Disable Mode register (Table 3).

When latch−off mode is selected the corresponding GAT_X output is turned off upon detection of a fault. Fault recovery is initiated by toggling (ON→OFF→ON) the channel's respective IN_X parallel input, serial G_X bit, or ENA2.

When auto−retry mode is selected (default mode) the corresponding GAT_X output is turned off for the duration of the programmed fault refresh time (t_{FR}) upon detection of a fault. The output is automatically turned back on (if still commanded on) when the refresh time ends. The channel's DRN_X feedback is resampled after the turn−on blanking time. The output will automatically be turned off if a fault is again detected. This behavior will continue for as long as the channel is commanded on and the fault persists.

In either mode, a fault may exist at turn−on or may occur some time afterward. To be detected, the fault must exist longer than either $t_{BL(ON)}$ at turn−on or longer than t_{FF} some time after turn−on. The length of time that a MOSFET stays on during a shorted load fault is thus limited to either $t_{BL(ON)}$ or t_{FF}.

In auto−retry mode, a persistent shorted load fault will result in a low duty cycle ($t_{FD} \approx t_{BL(ON)}/t_{FR}$) for the affected channel and help prevent thermal failure of the channel's MOSFET.

CAUTION – CONTINUOUS INPUT TOGGLING VIA IN_X, G_X or ENA2 WILL OVERRIDE EITHER DISABLE MODE. Care should be taken to service a shorted load fault quickly when one has been detected.

Fault Recovery Refresh Time

Refresh time for shorted load faults is SPI programmable to one of two values for channels 0−2 (register bit R2) and for channels 3−5 (register bit R5) via the Refresh and Reference register (Table 4).

A global refresh timer with taps at nominally 10 ms and 40 ms is used for auto−retry timing. The first faulted channel triggers the timer and the full refresh period is guaranteed for that channel. An additional faulted channel may initially retry immediately after its turn−on blanking time, but subsequent retries will have the full refresh time period.

If all channels in a group (e.g. channels 0−2) become faulted, they will become synchronized to the selected refresh period for that group. If all channels become faulted and are set for the same refresh time, all will become synchronized to the refresh period.

Open Load and Short to GND Detection

A window comparator with fixed references proportional to V_{CC1} along with a pair of bias currents is used to detect open load or short to GND faults when a channel is off. Each channel's DRN_X feedback is compared to the references after either the turn−off blanking or the filter has timed out. Figure 14 shows the DRN_X bias and fault detection zones. The diagnostics are disabled and the bias currents are turned off when ENA_X is low.

No fault is detected if the feedback voltage at DRN_X is greater than the V_{OL} open load reference. If the feedback is less than the V_{SG} short to GND reference, a short to GND fault is detected. If the feedback is less than V_{OL} and greater than V_{SG}, an open load fault is detected.

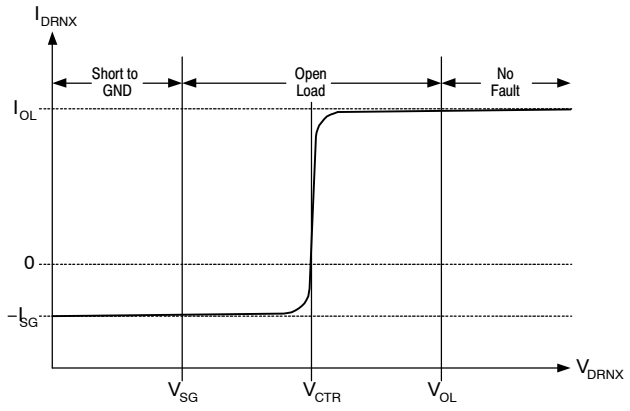


Figure 14. DRN_X Bias and Fault Detection Zones

Figure 15 shows the simplified detection circuitry. Bias currents I_{SG} and I_{OL} are applied to a bridge along with bias voltage V_{CTR} (50% V_{CC1} typ.).

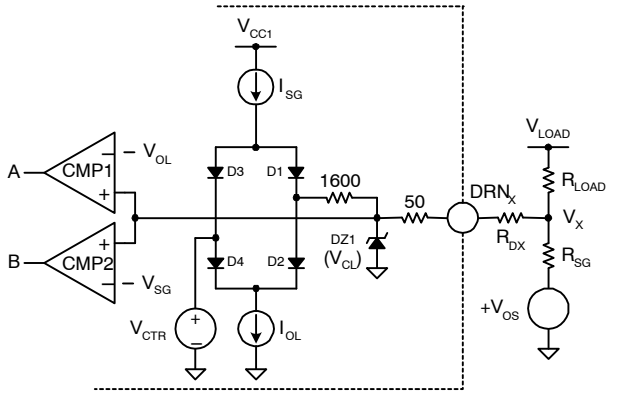


Figure 15. Short to GND/Open−Load Detection

When a channel is off and V_{LOAD} and R_{LOAD} are present, R_{SG} is absent, and $V_{DRNX} >> V_{CTR}$, bias current I_{OL} is supplied from V_{LOAD} to ground through external resistors R_{LOAD} and R_{DX}, and through the internal 1650 Ω resistance and bridge diode D2. Bias current I_{SG} is supplied from V_{CC1} to V_{CTR} through D3. No fault is detected if the feedback voltage (V_{LOAD} minus the total voltage drop caused by I_{SG} and the resistance in the path) is greater than V_{OL}.

When either V_{LOAD} or R_{LOAD} and R_{SG} are absent, the bridge will self−bias so that the voltage at DRN_X will settle to about V_{CTR}. An open load fault can be detected since the feedback is between V_{SG} and V_{OL}.

Short to GND detection can tolerate up to a 1.0 V offset (V_{OS}) between the NCV7517's GND and the short. When R_{SG} is present and $V_{DRNX} << V_{CTR}$, bias current I_{SG} is supplied from V_{CC1} to V_{OS} through D1, the internal 1650 Ω, and the external R_{DX} and R_{SG} resistances. Bias current I_{OL} is supplied from V_{CTR} to ground through D4.

A "weak" short to GND can be detected when either V_{LOAD} or R_{LOAD} is absent and the feedback (V_{OS} plus the total voltage rise caused by I_{OL} and the resistance in the path) is less than V_{OL}.

When V_{LOAD} and R_{LOAD} are present, a voltage divider between V_{LOAD} and V_{OS} is formed by R_{LOAD} and R_{SG}. A "hard" short to GND may be detected in this case depending on the ratio of R_{LOAD} and R_{SG} and the values of R_{DX}, V_{LOAD}, and V_{OS}.

Note that the comparators see a voltage drop or rise due only to the 50 Ω internal resistance and the bias currents. This produces a small difference in the comparison to the actual feedback voltage at the DRN_X input.

Several equations for choosing R_{DX} and for predicting open load or short to GND resistances, and a discussion of the dynamic behavior of the short to GND/open load diagnostic are provided in the Applications Information section of this data sheet.

Status Flag (STAB)

The open−drain active−low status flag output can be used to provide a host controller with information about the state of a channel's DRN_x feedback. Feedback from all channels is logically ORed to the flag (Figure 16). The STAB outputs from several devices can be wire−ORed to a common pullup resistor connected to the controller's 3.3 or 5.0 V V_{DD} supply.

When ENA1 is high, the drain feedback from a channel's DRN_x input is compared to the V_{OL} reference without regard to ENA2 or the commanded state of the channel's driver. The flag is reset and disabled when ENA1 is low or when all mask bits are set. See Table 9 for additional details.

The flag is set (low) when the feedback voltage is less than V_{OL}, and the channel's mask bit (Table 5) is cleared. The flag is reset (hi−Z) when the feedback voltage is greater than V_{OL}, and the channel's mask bit is cleared.

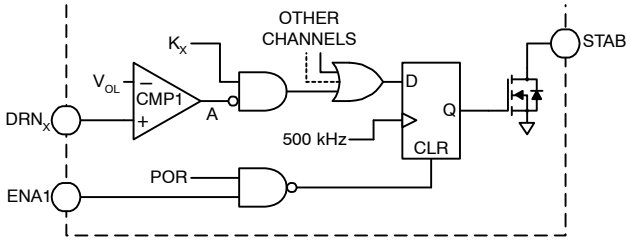


Figure 16. STAB Flag Logic

Fault Flag (FLTB)

The open−drain active−low fault flag output can be used to provide immediate fault notification to a host controller. Fault detection from all channels is logically ORed to the flag (Figure 17). The FLTB outputs from several devices can be wire−ORed to a common pullup resistor connected to the controller's 3.3 or 5.0 V V_{DD} supply.

The flag is set (low) when a channel detects any fault, the channel's mask bit (Table 5) is cleared, and both ENA_x and CSB are high. The flag is reset (hi−Z) and disabled when either ENA1 or CSB is low. See Table 9 for additional details.

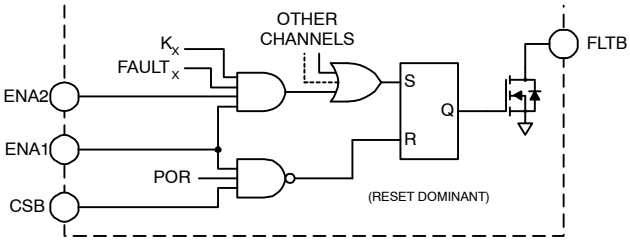


Figure 17. FLTB Flag Logic

Fault Detection and Capture

Each channel of the NCV7517 is capable of detecting shorted load faults when the channel is on, and short to ground or open load faults when the channel is off. Each fault type is uniquely encoded into two−bit per channel fault data. A drain feedback input for each channel compares the voltage at the drain of the channel's external MOSFET to several internal reference voltages. Separate detection references are used to distinguish the three fault types, and blanking and filter timers are used respectively to allow for output state transition settling and for glitch suppression.

Fault diagnostics are disabled when either enable input is low. When both enable inputs are high, each channel's drain feedback input is continuously compared to references appropriate to the channel's input state to detect faults, but the comparison result is only latched at the end of either a blanking or filter timer event.

Blanking timers for all channels are triggered when either enable input changes state from low to high while the other enable input is high, or when both enable inputs go high simultaneously. A single channel's blanking timer is triggered when its input state changes. If the comparison of the feedback to a reference indicates an abnormal condition when the blanking time ends, a fault has been detected and the fault data is latched into the channel's fault latch.

A channel's filter timer is triggered when its drain feedback comparison state changes. If the change indicates an abnormal condition when the filter time ends, a fault has been detected and the fault data is latched into the channel's fault latch.

Thus, a state change of the inputs (ENA_X, IN_X or G_X) or a state change of an individual channel's feedback (DRN_X) comparison must occur for a timer to be triggered and a detected fault to be captured.

Fault Capture, SPI Communication, and SPI Frame Error Detection

The fault capture and frame error detection strategies of the NCV7517 combine to ensure that intermittent faults can be captured and identified, and that the device cannot be inadvertently reprogrammed by a communication error.

The NCV7517 latches a fault when it is detected, and frame error detection will not allow any register to accept data if an invalid frame occurred.

When a fault has been detected, the FLTB flag is set and fault data is latched into a channel's fault latch. The latch captures and holds the fault data and ignores subsequent fault data for that channel until a valid SPI frame occurs.

Fault data from all channels is transferred from each channel's fault latch into the SPI shift register and the FLTB flag is reset when CSB goes low at the start of the SPI frame. Fault latches are cleared and re−armed when CSB goes high at the end of the SPI frame only if a valid frame has occurred; otherwise the latches retain the detected fault data until a valid frame occurs. The FLTB flag will be set if a fault is still present.

Fault latches for all channels and the FLTB flag can also be cleared and re−armed by toggling ENA1 H−L−H. A full I/O truth table is given in Table 9.

Fault Data Readback Examples

Several examples are shown to illustrate fault detection, capture and SPI read−back of fault data for one channel. A normal SPI frame returns 16 bits of data but only the two bits of serial data for the single channel are shown for clarity.

The examples assume:

- The NCV7517 is configured as in Figure 2
- Both enable inputs are high
- The channel's flag mask bit is cleared
- Disable mode is set to auto−retry
- The parallel input commands the channel
- SPI frame is always valid

Shorted Load Detected

Refer to Figure 18. The channel is commanded on when IN_X goes high. GAT_X goes high and the timers are started. At "A", the STAB flag is set as the DRN_X feedback falls through the V_{OL} threshold. A SPI frame sent soon after the IN_X command returns data indicating "no fault."

The blanking time ends and the filter timer is triggered as DRN_X rises through the FLTREF threshold. The STAB flag is reset as DRN_X passes through the V_{OL} threshold. DRN_X is nearly at V_{LOAD} when the filter time ends at "B". A shorted load fault is detected and captured by the fault latch, GAT_X goes low, the FLTB flag is set, and the auto−retry timer is started.

An SPI frame sent soon after "B" returns data indicating "shorted load". The FLTB flag is reset when CSB goes low. At "C" when CSB goes high at the end of the frame, the fault latch is cleared and re−armed. Since IN_X and the DRN_X feedback are unchanged, FLTB and the fault latch are set and the fault is recaptured.

When the auto−retry timer ends at "D", GAT_X goes high and the blanking and filter timers are started. Since IN_X and DRN_X are unchanged, GAT_X goes low when the blanking time ends at "E" and the auto−retry timer is started. Read−back data continues to indicate a "shorted load" and the FLTB flag continues to be set while the fault persists.

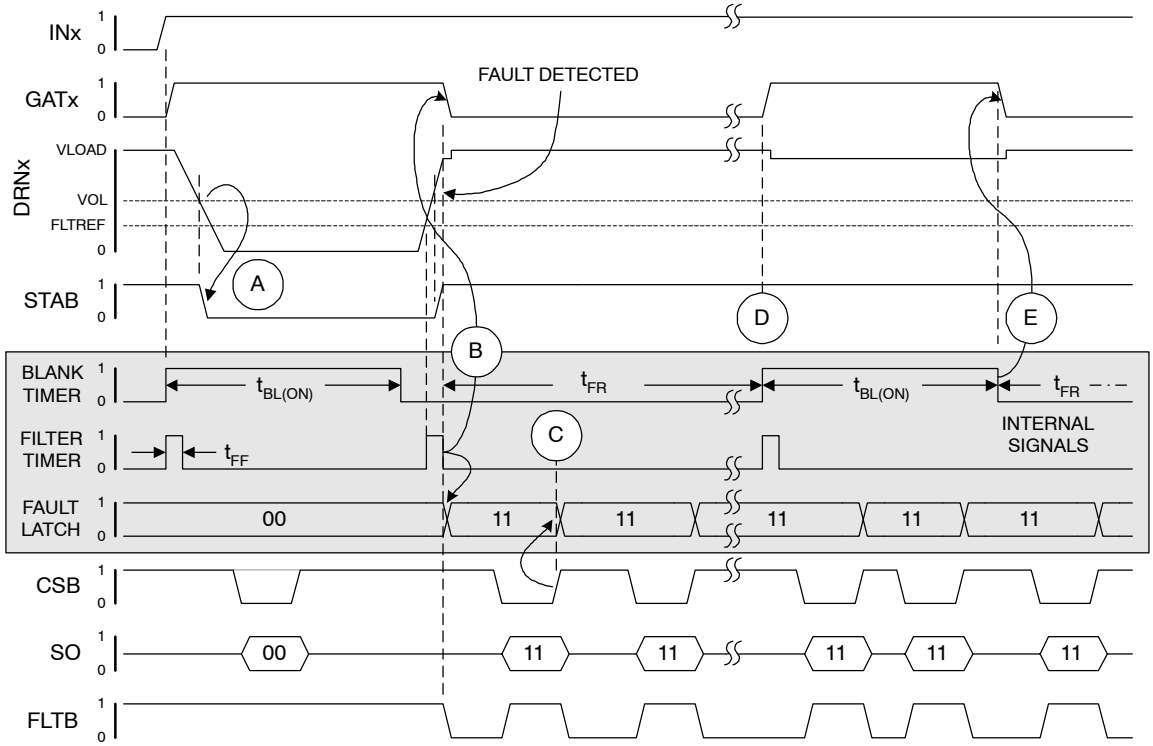


Figure 18. Shorted Load Detected

Shorted Load Recovery

Figure 19 is a continuation of Figure 18. IN_X is high when the auto−retry timer ends. GAT_X goes high and the blanking and filter timers are started. The fault is removed before the blanking timer ends, and DRN_X starts to fall. As DRN_X passes through the V_{OL} threshold at “A”, the STAB flag is set. DRN_X continues to fall and settles below the FLTREF threshold.

An SPI frame is sent during the blanking time and returns data indicating a “shorted load” fault. Although the fault is removed, updates to the fault latches are suppressed while a blanking or filter timer is active. The same fault is captured again and FLTB is set when CSB goes high. At “B” the blanking time ends and the channel’s fault bits will indicate “no fault” but because the latched data has not yet been read, the data remains unchanged.

The SPI frame sent after the blanking time ends returns a “shorted load” fault because the previous frame occurred during the blanking time. Since the channel’s fault bits indicate “no fault”, FLTB is reset and the fault latch is updated at “C” when CSB goes high. If another SPI frame is sent before “D”, the returned data will indicate “no fault”.

The channel is commanded off at “D”. GAT_X goes low and the timers are started. DRN_X starts to rise and the STAB flag is reset as DRN_X passes through the V_{OL} threshold. The SPI frame sent at “E” returns data indicating “no fault”.

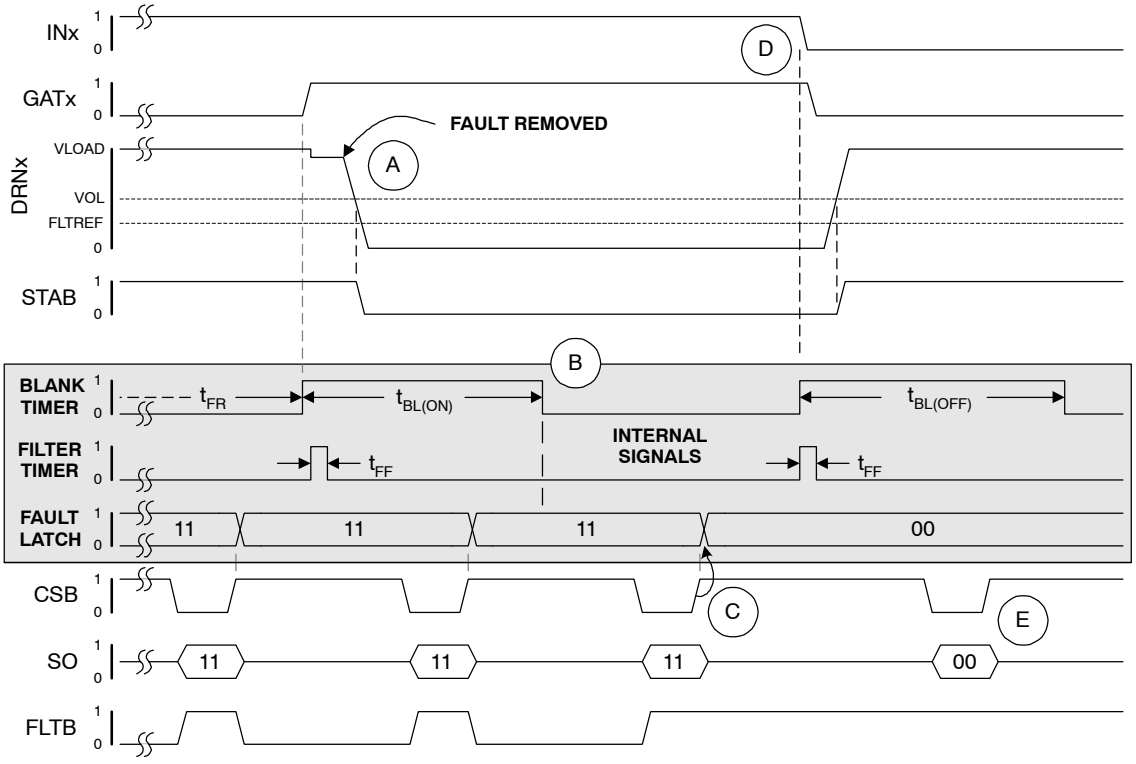


Figure 19. Shorted Load Recovery

Short to GND/Open Load

Figure 20 illustrates turn−off with an open or high resistance load when some capacitance is present at DRN_X. In the case of an open load, DRN_X rises and settles to V_{CTR}. In the case of a high resistance load, DRN_X may continue to rise and may eventually settle to V_{LOAD}.

The channel is commanded off. GAT_X goes low and the timers are started. DRN_X starts to rise and is below the V_{SG} threshold when the blanking time ends at “A”. A short to GND fault is detected and captured by the fault latch, and the FLTB flag is set.

DRN_X continues to rise and as it passes through the V_{SG} threshold at “B”, the filter timer is triggered. At the end of the filter time, the channel’s fault bits will indicate an “open load” but because the latched data has not yet been read, the data remains unchanged.

An SPI frame sent shortly after “B” returns data indicating “short to GND” and the fault latch is updated at “C” when CSB goes high. The next three frames sent after “C” return data indicating an “open load”.

The STAB flag is reset at “D” as DRN_X passes through the V_{OL} threshold. Note that the filter timer is not triggered as DRN_X passes from a fault state to a good state. The channel’s fault bits will indicate “no fault” but because the latched data has not yet been read, the data remains unchanged.

The fault latch is updated at “E” when CSB goes high and the FLTB flag remains reset. The next SPI frame sent returns data indicating “no fault”.

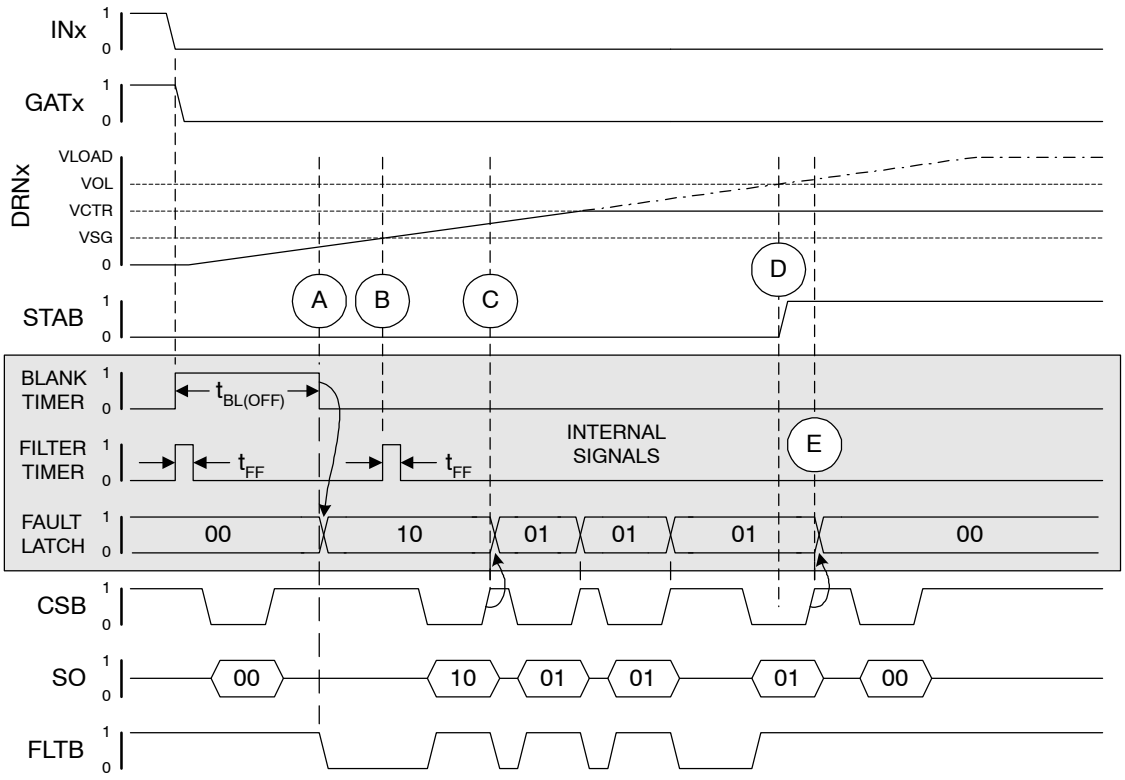


Figure 20. Short to GND/Open Load

Table 9. I/O Truth Table

Inputs								Outputs*				
POR	**ENA1**	**ENA2**	**CSB**	**K_X**	**IN_X**	**G_X**	**DRN_X**	**GAT_X**	**FLTB**	**STAB**	**$D_{X1}D_{X0}$**	**COMMENT**
0	X	X	X	→0	X	→0	X	→L	→Z	→Z	→00	POR RESET
1	0	X	X	X	X	X	X	L	Z	Z	00	ENA1
1	1	0	X	K_X	X	G_X	X	L	FLTB	STAB	$D_{X1}D_{X0}$	ENA2
1	1→0	1	X	K_X	X	→0	X	→L	→Z	→Z	→00	ENA1 RESET
1	1	1→0	X	K_X	X	G_X	X	→L	FLTB	STAB	$D_{X1}D_{X0}$	ENA2 DISABLE
1	1	X	X	0	X	X	X	L	Z	Z	–	FLAGS MASKED
1	1	0	X	1	X	X	> V_{OL}	L	–	Z	–	STAB RESET
1	1	0	X	1	X	X	< V_{OL}	L	–	L	–	STAB SET
1	1	0	X	1→0	X	X	< V_{OL}	L	–	L→Z	–	STAB RESET
1	1	0	X	0→1	X	X	< V_{OL}	L	–	Z→L	–	STAB SET
1	1	1	X	1	0	0	> V_{OL}	L	Z	Z	00	FLAGS RESET
1	1	1	1	1	0	0	V_{SG}<V<V_{OL}	L	L	L	01	FLAGS SET
1	1	1	X	1→0	0	0	V_{SG}<V<V_{OL}	L	L	L→Z	01	STAB RESET
1	1	1	X	0→1	0	0	V_{SG}<V<V_{OL}	L	L		01	STAB SET
1	1	1	1→0	1	0	0	V_{SG}<V<V_{OL}	L	L→Z	L	01	FLTB RESET
1	1	1	0→1	1	0	0	V_{SG}<V<V_{OL}	L	Z→L	L	01	FLTB SET
1	1	1	1	1	0	0	< V_{SG}	L	L	L	10	FLAGS SET
1	1	1	X	1→0	0	0	< V_{SG}	L	L	L→Z	10	STAB RESET
1	1	1	X	0→1	0	0	< V_{SG}	L	L	Z→L	10	STAB SET
1	1	1	1→0	1	0	0	< V_{SG}	L	L→Z	L	10	FLTB RESET
1	1	1	0→1	1	0	0	< V_{SG}	L	Z→L	L	10	FLTB SET
1	1	1	X	1	1	X	< V_{FLTREF}	H	Z	L	00	STAB SET
1	1	1	1	1	1	X	V_{FLTREF}<V<V_{OL}	L	L	L	11	FLAGS SET
1	1	1	X	1→0	1	X	V_{FLTREF}<V<V_{OL}	L	L	L→Z	11	STAB RESET
1	1	1	X	0→1	1	X	V_{FLTREF}<V<V_{OL}	L	L	Z→L	11	STAB SET
1	1	1	1→0	1	1	X	V_{FLTREF}<V<V_{OL}	L	L→Z	L	11	FLTB RESET
1	1	1	0→1	1	1	X	V_{FLTREF}<V<V_{OL}	L	Z→L	L	11	FLTB SET
1	1	1	1	1	1	X	> V_{OL}	L	L	Z	11	STAB RESET
1	1	1	X	1	X	1	< V_{FLTREF}	H	Z	L	00	STAB SET
1	1	1	1	1	X	1	V_{FLTREF}<V<V_{OL}	L	L	L	11	FLAGS SET
1	1	1	X	1→0	X	1	V_{FLTREF}<V<V_{OL}	L	L	L→Z	11	STAB RESET
1	1	1	X	0→1	X	1	V_{FLTREF}<V<V_{OL}	L	L	Z→L	11	STAB SET
1	1	1	1→0	1	X	1	V_{FLTREF}<V<V_{OL}	L	L→Z	L	11	FLTB RESET
1	1	1	0→1	1	X	1	V_{FLTREF}<V<V_{OL}	L	Z→L	L	11	FLTB SET
1	1	1	1	1	X	1	> V_{OL}	L	L	Z	11	STAB RESET

* Output states after blanking and filter timers end and when channel is set to latch−off mode.

APPLICATION GUIDELINES

General

Unused DRN_X inputs should be connected to V_{CC1} to prevent false open load faults. Unused parallel inputs should be connected to GND and unused enable inputs should be connected to V_{CC1}. The mask bit for each unused channel should be 'set' (see Table 5) to prevent activation of the flags and the user's software should be designed to ignore fault information for unused channels. For best shorted−load detection accuracy, the external MOSFET source terminals should be star−connected and the NCV7517's GND pin, and the lower resistor in the fault reference voltage divider should be Kelvin connected to the star (see Figures 2 and 13).

Consideration of auto−retry fault recovery behavior is necessary from a power dissipation viewpoint (for both the NCV7517 and the MOSFETs) and also from an EMI viewpoint.

Driver slew rate and turn−on/off symmetry can be adjusted externally to the NCV7517 in each channel's gate circuit by the use of series resistors for slew control, or resistors and diodes for symmetry. Any benefit of EMI reduction by this method comes at the expense of increased switching losses in the MOSFETs.

The channel fault blanking timers must be considered when choosing external components (MOSFETs, slew control resistors, etc.) to avoid false faults. Component choices must ensure that gate circuit charge/discharge times stay within the turn−on/turn−off blanking times.

The NCV7517 does not have integral drain−gate flyback clamps. Clamp MOSFETs, such as ON Semiconductor's NID9N05CL, are recommended when driving unclamped inductive loads. This flexibility allows choice of MOSFET clamp voltages suitable to each application.

DRN_X Feedback Resistor

Each DRN_X feedback input has a clamp to keep the applied voltage below the breakdown voltage of the NCV7517. An external series resistor (R_{DX}) is required between each DRN_X input and MOSFET drain. Channels may be clamped sequentially or simultaneously but total clamp power is limited to the maximum allowable junction temperature.

To limit power in the DRN_X input clamps and to ensure proper open load or short to GND detection, the R_{DX} resistor must be dimensioned according to the following constraint equations:

$$R_{DX(MIN)} = \frac{V_{PK} - V_{CL(MIN)}}{I_{CL(MAX)}} \quad \text{(eq. 2)}$$

$$R_{DX(MAX)} = \frac{V_{SG} - |V_{OS}|}{|I_{SG}|} \quad \text{(eq. 3)}$$

where V_{PK} is the peak transient drain voltage, V_{CL} is the DRN_X input clamp voltage, $I_{CL(MAX)}$ is the input clamp current, and V_{SG} and I_{SG} are the respective short to GND fault detection voltage and diagnostic current, and V_{OS} is the allowable offset (1.0 V max) between the NCV7517's GND and the short.

Once R_{DX} is chosen, the open load and short to GND detection resistances in the application can be predicted:

$$R_{OL} \geq \frac{V_{LOAD} - V_{OL}}{I_{OL}} - R_{DX} \quad \text{(eq. 4)}$$

$$R_{SG} \leq \frac{R_{LOAD}(V_{SG} \pm V_{OS} - |I_{SG}|R_{DX})}{V_{LOAD} - V_{SG} + |I_{SG}|(R_{DX} + R_{LOAD})} \quad \text{(eq. 5)}$$

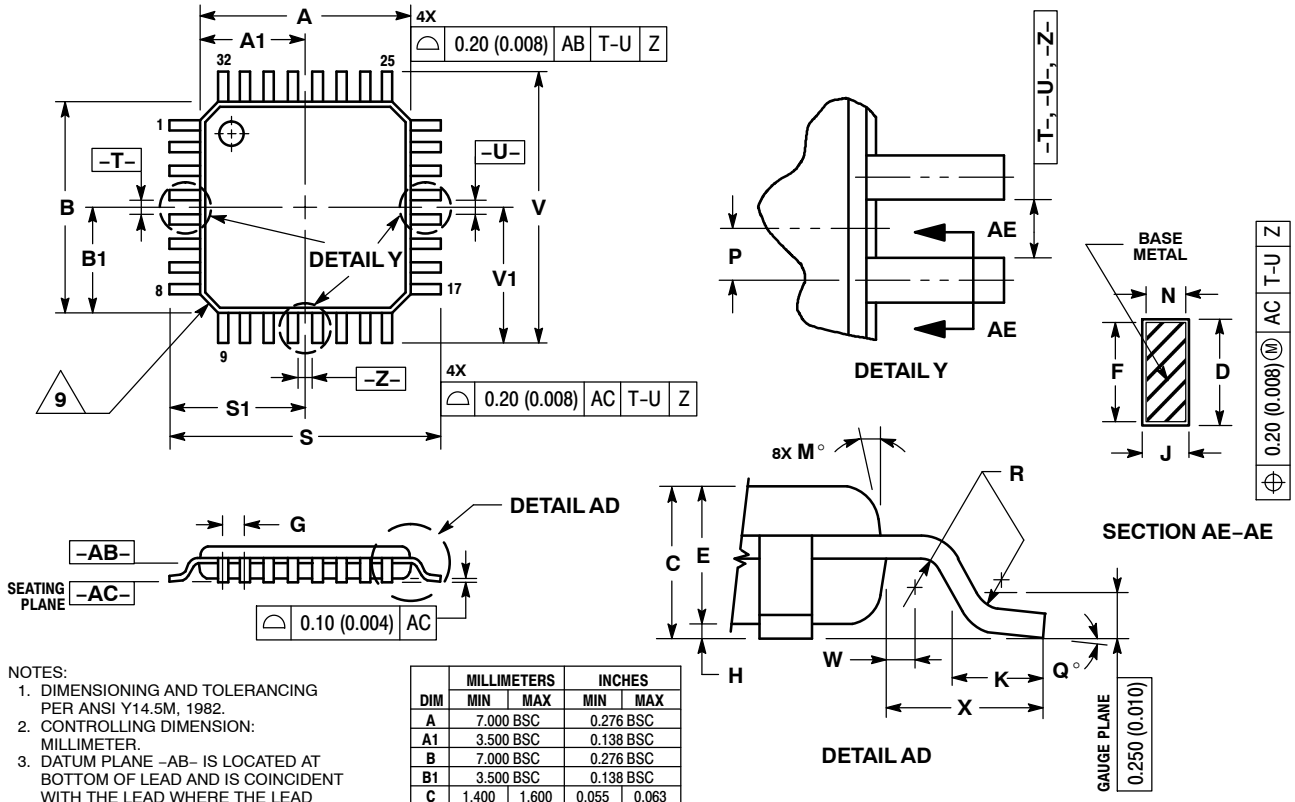
Using the data sheet values for $V_{CL(MIN)}$ = 27 V, $I_{CL(MAX)}$ = 10 mA, and choosing V_{PK} = 55 V as an example, Equation 2 evaluates to 2.8 kΩ minimum.

Choosing V_{CC1} = 5.0 V and using the typical data sheet values for V_{SG} = 30%V_{CC1}, I_{SG} = 20 μA, and choosing V_{OS} = 0, Equation 3 evaluates to 75 kΩ maximum.

Selecting R_{DX} = 6.8 kΩ ±5%, V_{CC1} = 5.0 V, V_{LOAD} = 12.0 V, V_{OS} = 0 V, R_{LOAD} = 555 Ω, and using the typical data sheet values for V_{OL}, I_{OL}, V_{SG}, and I_{SG}, Equation 4 predicts an open load detection resistance of 130.7 kΩ and Equation 5 predicts a short to GND detection resistance of 71.1 Ω. When R_{DX} and the data sheet values are taken to their extremes, the open load detection range is 94.1 kΩ ≤ R_{OL} ≤ 273.5 kΩ, and the short to GND detection range is 59.2 Ω ≤ R_{SG} ≤ 84.4 Ω.

PACKAGE DIMENSIONS

32 LEAD LQFP
CASE 873A–02
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.450	0.750	0.018	0.030
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

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