MOSFET – N-Channel, UniFET™

500 V, 20 A, 230 mΩ

FDP20N50/FDPF20N50 /FDPF20N50T

V_{DSS}	$R_{DS(on)}$ MAX	I_D MAX
500 V	230 mΩ @ 10 V	20 A

Description

UniFET™ MOSFET is **onsemi**'s high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on−state resistance, and to provide better switching performance and higher avalanche energy strength. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.

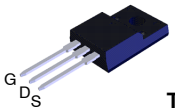
Features

- $R_{DS(on)}$ = 200 mΩ (Typ.) @ V_{GS} = 10 V, I_D = 10 A
- Low Gate Charge (Typ. 45.6 nC)
- Low C_{rss} (Typ. 27 pF)
- 100% Avalanche Tested

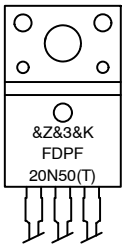
Applications

- LCD/LED/PDP TV
- Lighting
- Uninterruptible Power Supply
- AC−DC Power Supply

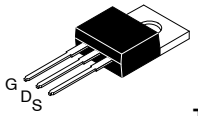
MARKING DIAGRAMS



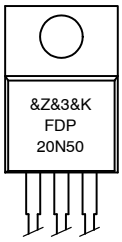
TO−220 Fullpack, 3−Lead / TO−220F−3SG CASE 221AT



&Z	= Assembly Plant Code
&3	= 3−Digit Date Code
&K	= 2−Digits Lot Run Code
FDPF20N50(T)	= Specific Device Code

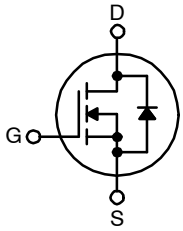


TO−220−3LD CASE 340AT



&Z	= Assembly Plant Code
&3	= 3−Digit Date Code
&K	= 2−Digits Lot Run Code
FDP20N50	= Specific Device Code

N−CHANNEL MOSFET



ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Parameter		FDP20N50	FDPF20N50/ FDPF20N50T	Unit
V_{DSS}	Drain−Source Voltage		500		V
I_D	Drain Current	Continuous (T_C = 25°C)	20	20*	A
		Continuous (T_C = 100°C)	12.9	12.9*	
I_{DM}	Drain Current	Pulsed (Note 1)	80	80*	A
V_{GSS}	Gate−Source Voltage		±30		V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		1110		mJ
I_{AR}	Avalanche Current (Note 1)		20		A
E_{AR}	Repetitive Avalanche Energy (Note 1)		25		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		4.5		V/ns
P_D	Power Dissipation	(T_C = 25°C)	250	38.5	W
		Derate above 25°C	2.0	0.3	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		−55 to +150		°C
T_L	Maximum Lead Temperature for Soldering, 1/8” from Case for 5 Seconds		300		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
*Drain current limited by maximum junction temperature.
1. Repetitive rating: pulse−width limited by maximum junction temperature.
2. L = 5.0 mH, I_{AS} = 20 A, V_{DD} = 50 V, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 20 A, di/dt ≤ 200 A/μs, V_{DD} ≤ BV_{DSS}, starting T_J = 25°C.

THERMAL CHARACTERISTICS

Symbol	Parameter	FDP20N50	FDPF20N50/ FDPF20N50T	Unit
$R_{\theta JC}$	Thermal Resistance, Junction−to−Case, Max.	0.5	3.3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient, Max.	62.5	62.5	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain−Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	500	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	–	0.5	–	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 500 V, V_{GS} = 0 V V_{DS} = 400 V, T_C = 125°C	– –	– –	1 10	μA μA
I_{GSSF}	Gate−Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	–	–	100	nA
I_{GSSR}	Gate−Body Leakage Current, Reverse	V_{GS} = −30 V, V_{DS} = 0V	–	–	−100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	3.0	–	5.0	V
$R_{DS(on)}$	Static Drain−Source On−Resistance	V_{GS} = 10 V, I_D = 10 A	–	0.20	0.23	Ω
g_{FS}	Forward Transconductance	V_{DS} = 40 V, I_D = 10 A	–	24.6	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	–	2400	3120	pF
C_{oss}	Output Capacitance		–	355	465	pF
C_{rss}	Reverse Transfer Capacitance		–	27	–	pF
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 250 V, I_D = 20 A, V_{GS} = 10 V, R_G = 25 Ω (Note 4)	–	95	200	ns
t_r	Turn−On Rise Time		–	375	760	ns
$t_{d(off)}$	Turn−Off Delay Time		–	100	210	ns
t_f	Turn−Off Fall Time		–	105	220	ns
Q_g	Total Gate Charge	V_{DS} = 400 V, I_D = 20 A, V_{GS} = 10 V (Note 4)	–	45.6	59.5	nC
Q_{gs}	Gate−Source Charge		–	14.8	–	nC
Q_{gd}	Gate−Drain Charge		–	21.6	–	nC
DRAIN−SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain−Source Diode Forward Current		–	–	30	A
I_{SM}	Maximum Pulsed Drain−Source Diode Forward Current		–	–	80	A
V_{SD}	Drain−Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 20 A	–	–	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 20 A, dI_F/dt = 100 A/μs	–	507	–	ns
Q_{rr}	Reverse Recovery Charge		–	7.20	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

TYPICAL CHARACTERISTICS

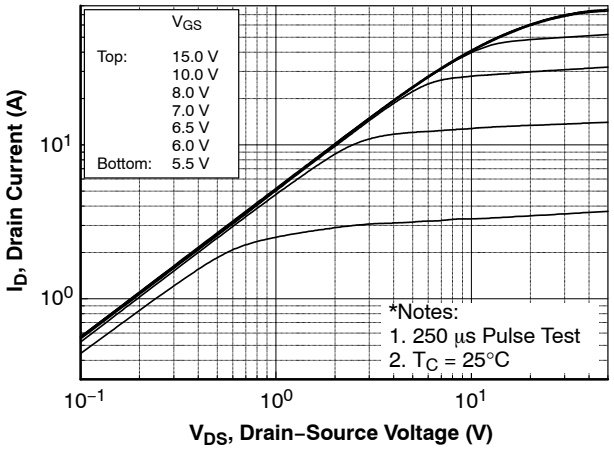


Figure 1. On−Region Characteristics

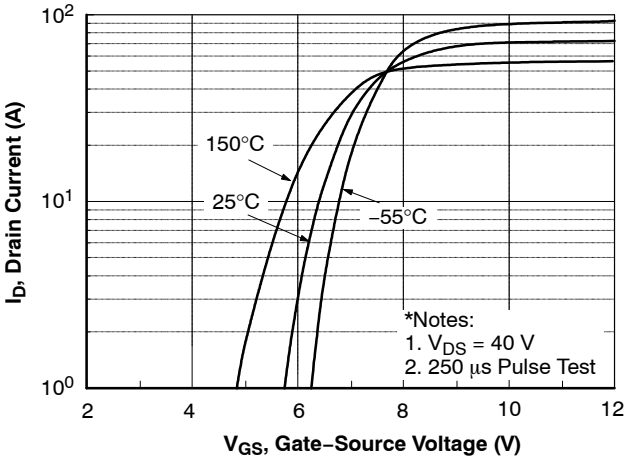


Figure 2. Transfer Characteristics

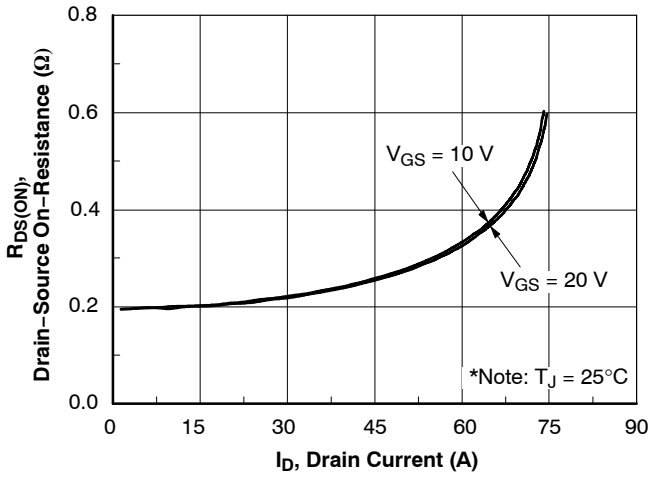


Figure 3. On−Resistance Variation vs. Drain Current and Gate voltage

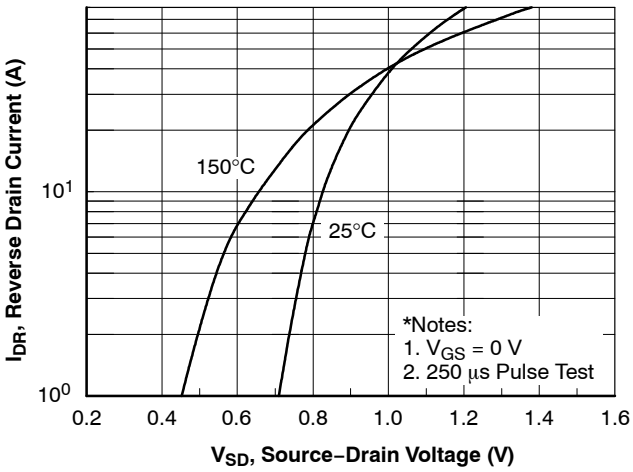


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

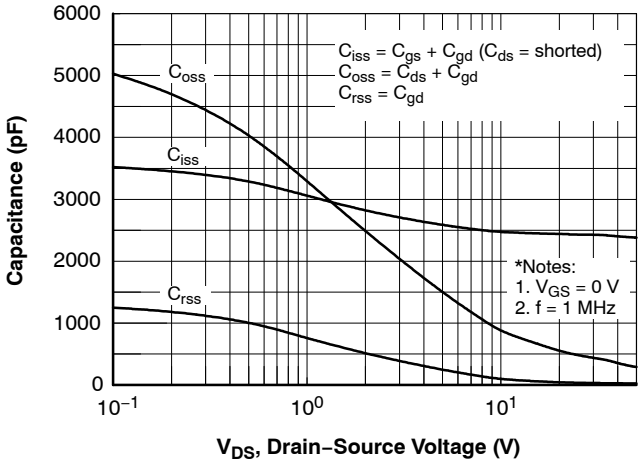


Figure 5. Capacitance Characteristics

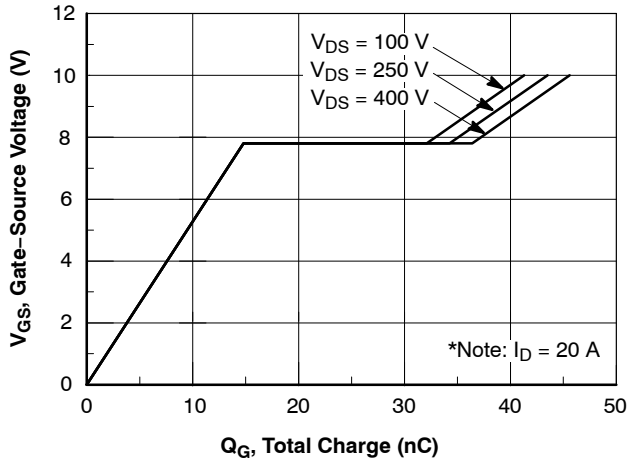


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS (Continued)

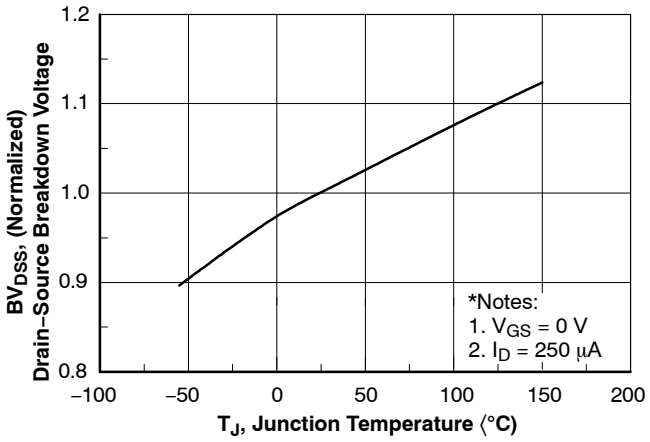


Figure 7. Breakdown Voltage Variation vs. Temperature

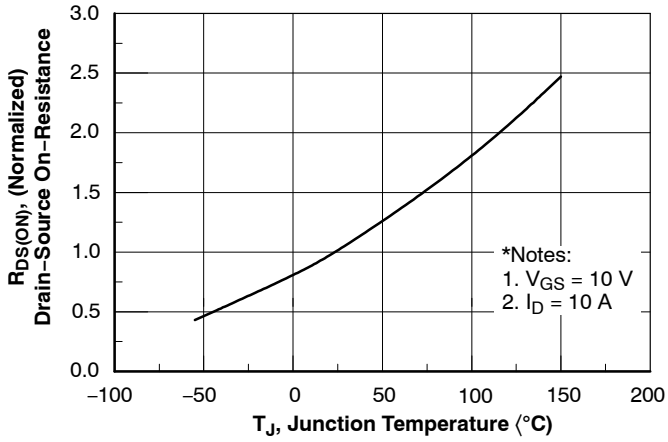


Figure 8. On–Resistance Variation vs. Temperature

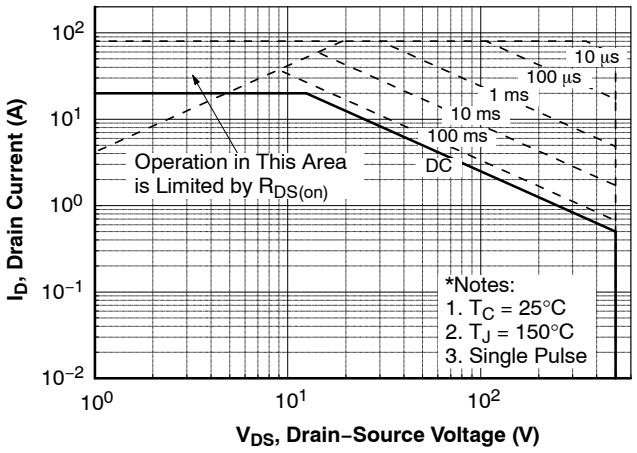


Figure 9. Maximum Safe Operating Area – FDP20N50

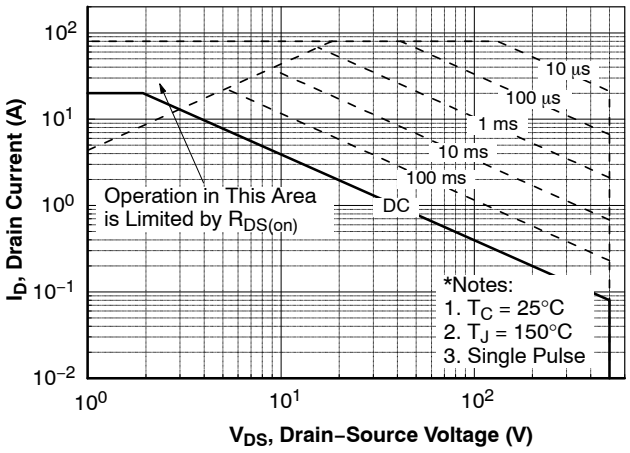


Figure 10. Maximum Safe Operating Area – FDPF20N50

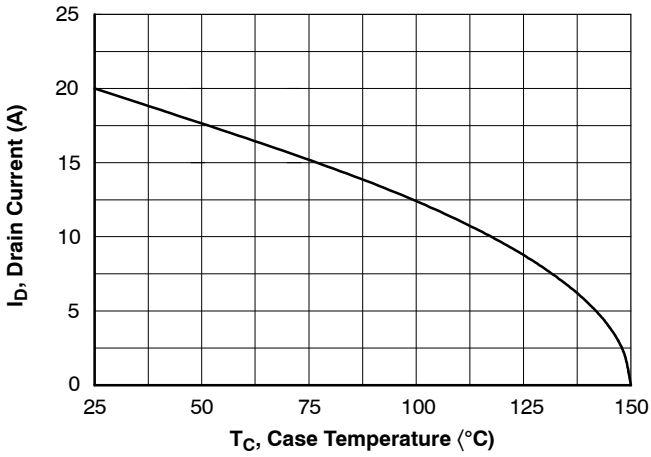


Figure 11. Maximum Drain Current vs. Case Temperature

TYPICAL CHARACTERISTICS (Continued)

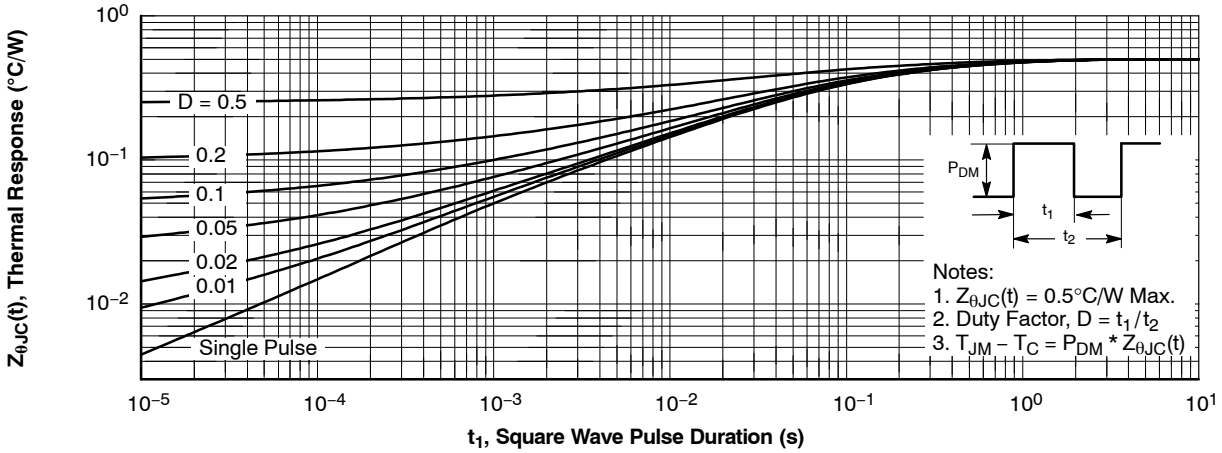


Figure 13. Transient Thermal Response Curve – FDP20N50

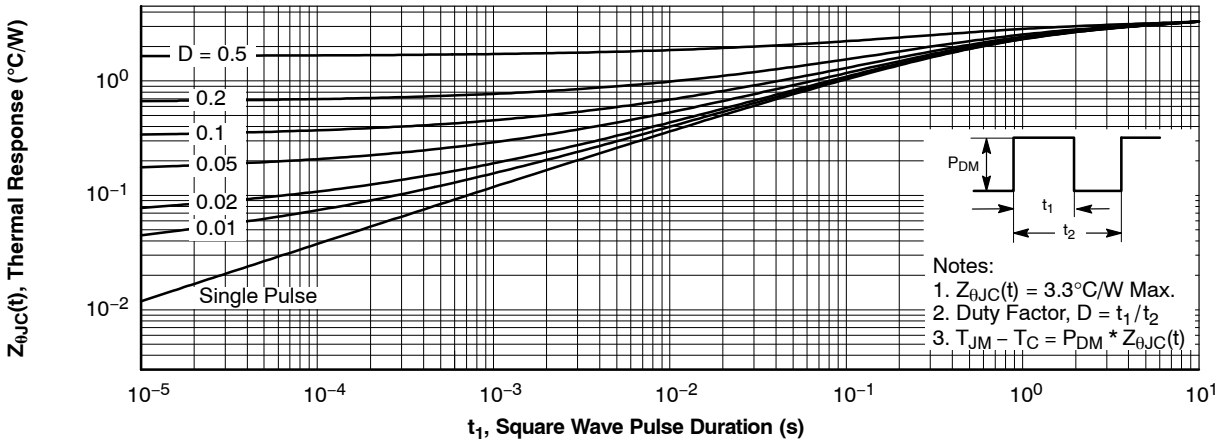


Figure 12. Transient Thermal Response Curve – FDPF20N50

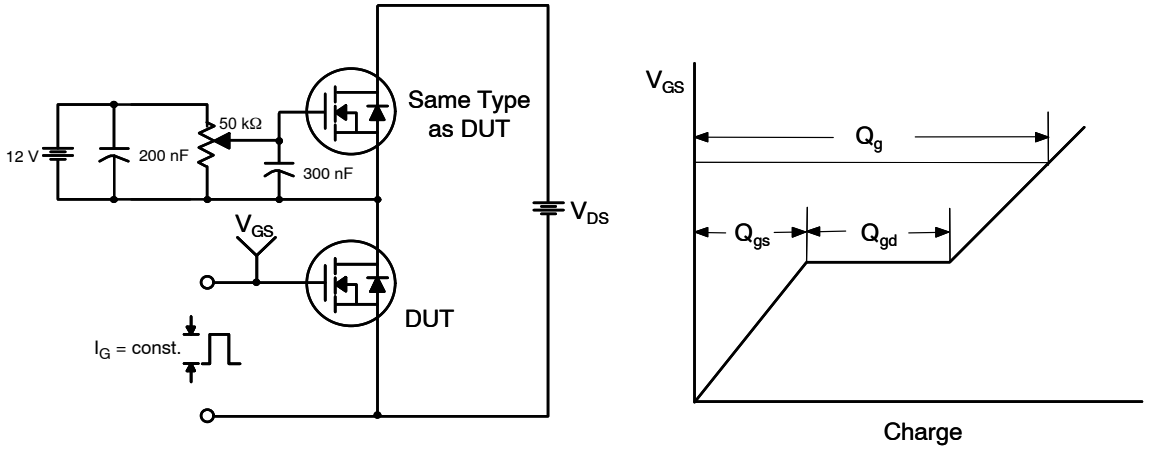


Figure 14. Gate Charge Test Circuit & Waveform

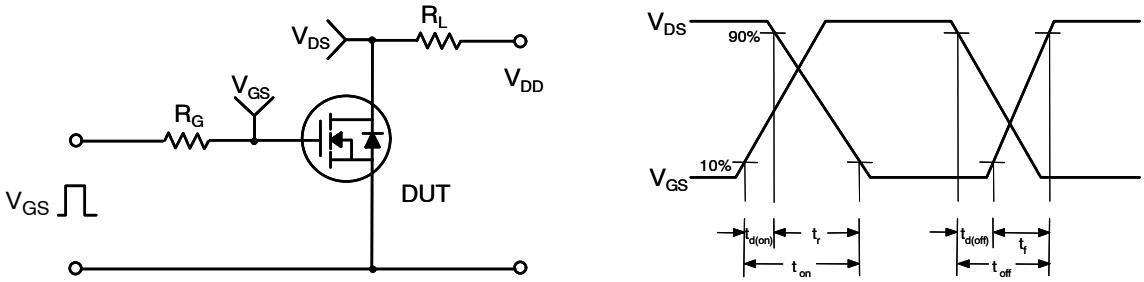


Figure 15. Resistive Switching Test Circuit & Waveforms

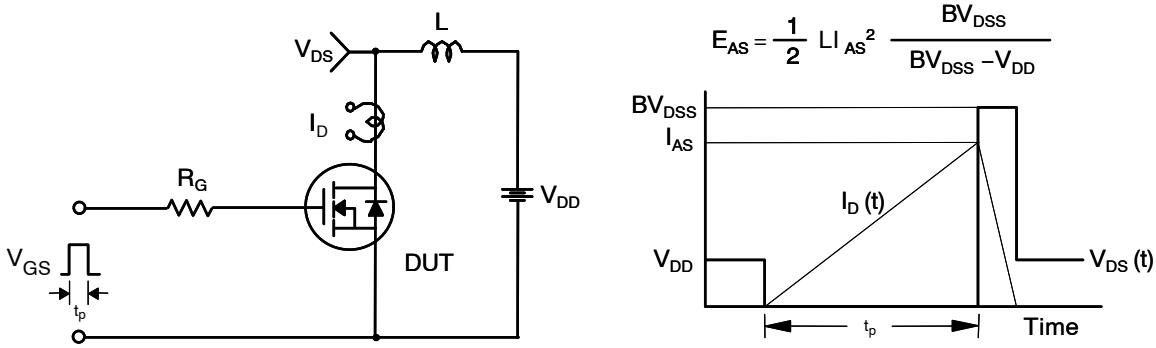


Figure 16. Unclamped Inductive Switching Test Circuit & Waveforms

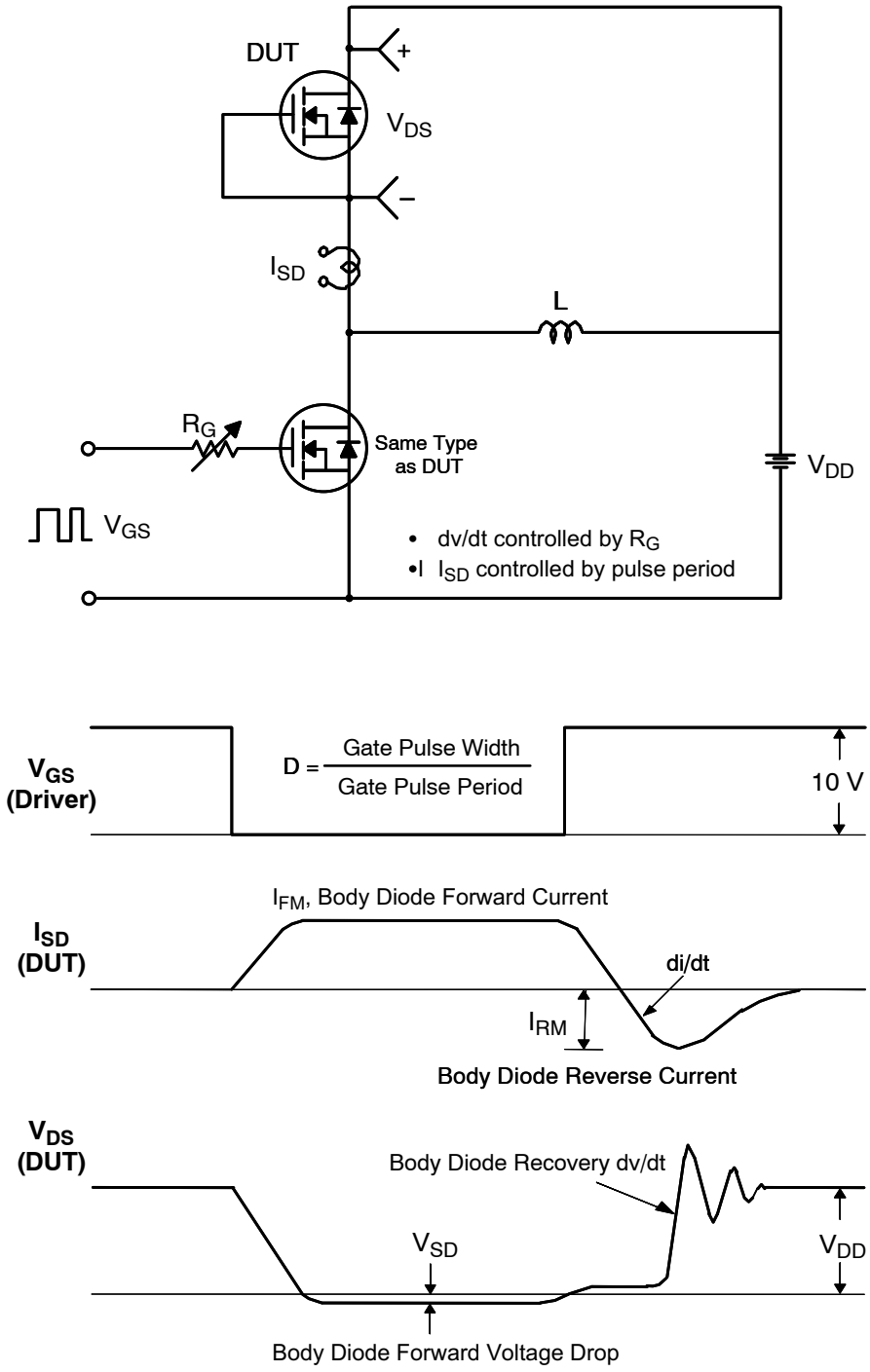


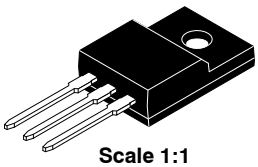
Figure 17. Peak Diode Recovery dv/dt Test Circuit & Waveforms

PACKAGE MARKING AND ORDERING INFORMATION

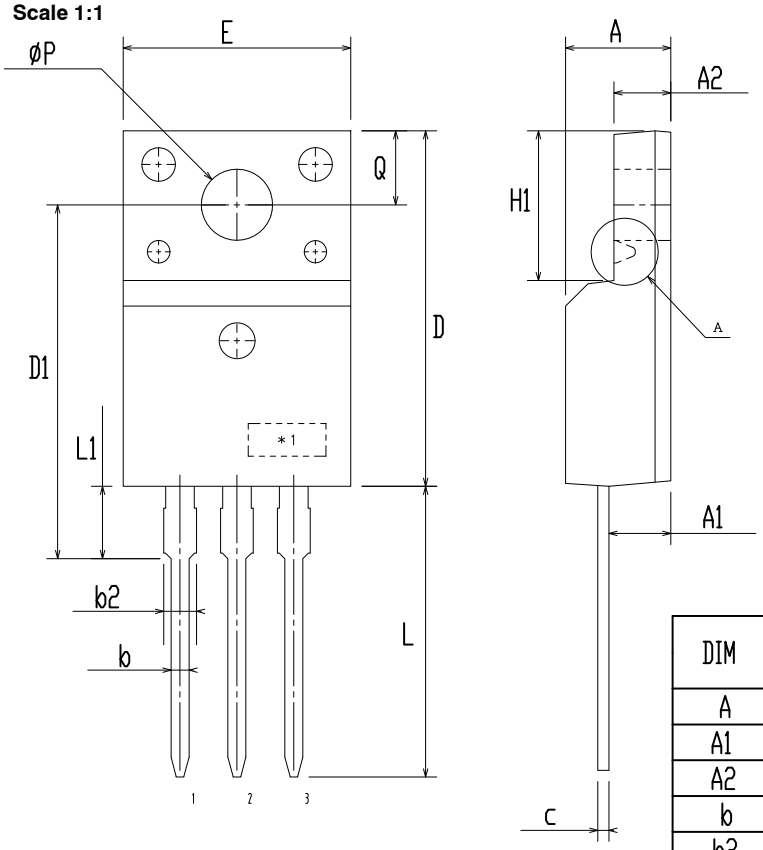
Part Number	Top Mark	Package	Quantity
FDP20N50	FDP20N50	TO−220−3LD CASE 340AT	50 Units / Tube
FDPF20N50	FDPF20N50	TO−220 Fullpack, 3−Lead / TO−220F−3SG CASE 221AT	50 Units / Tube
FDPF20N50T	FDPF20N50	TO−220 Fullpack, 3−Lead / TO−220F−3SG CASE 221AT	50 Units / Tube

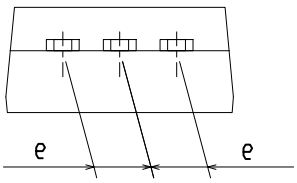
TO−220 Fullpack, 3−Lead / TO−220F−3SG
CASE 221AT
ISSUE B

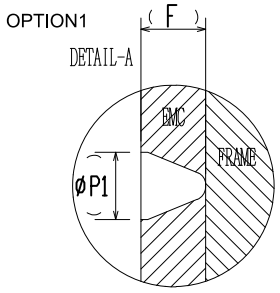
DATE 19 JAN 2021



Scale 1:1







DIM	MILLIMITERS		
	MIN	NOM	MAX
A	4.50	4.70	4.90
A1	2.56	2.76	2.96
A2	2.34	2.54	2.74
b	0.70	0.80	0.90
b2	~	~	1.47
c	0.45	0.50	0.60
D	15.67	15.87	16.07
D1	15.60	15.80	16.00
E	9.96	10.16	10.36
e	2.34	2.54	2.74
F	~	0.84	~
H1	6.48	6.68	6.88
L	12.78	12.98	13.18
L1	3.03	3.23	3.43
ø P	2.98	3.18	3.38
ø P1	~	1.00	~
Q	3.20	3.30	3.40

NOTES:
A. DIMENSION AND TOLERANCE AS ASME Y14.5-2009
B. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUCSIONS.
C. OPTION 1 - WITH SUPPORT PIN HOLE
OPTION 2 - NO SUPPORT PIN HOLE

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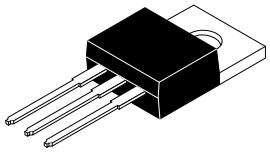
DESCRIPTION:	**TO−220 FULLPACK, 3−LEAD / TO−220F−3SG**	**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

TO−220−3LD
CASE 340AT
ISSUE A

DATE 03 OCT 2017



Scale 1:1

NOTES:
A) REFERENCE JEDEC, TO-220, VARIATION AB
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS COMMON TO ALL PACKAGE SUPPLIERS EXCEPT WHERE NOTED [ ].
D) LOCATION OF MOLDED FEATURE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
E DOES NOT COMPLY JEDEC STANDARD VALUE.
F) "A1" DIMENSIONS AS BELOW:
SINGLE GAUGE = 0.51 - 0.61
DUAL GAUGE = 1.10 - 1.45
G PRESENCE IS SUPPLIER DEPENDENT
H) SUPPLIER DEPENDENT MOLD LOCKING HOLES IN HEATSINK.

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DESCRIPTION:	**TO−220−3LD**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

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