

LDO Regulator - Ultra-Low Noise, High PSRR, RF and Analog Circuits

250 mA

NCP163

The NCP163 is a next generation of high PSRR, ultra-low noise LDO capable of supplying 250 mA output current. Designed to meet the requirements of RF and sensitive analog circuits, the NCP163 device provides ultra-low noise, high PSRR and low quiescent current. The device also offer excellent load/line transients. The NCP163 is designed to work with a 1 μ F input and a 1 μ F output ceramic capacitor. It is available in two thickness ultra-small 0.35P, WLCSP Packages, XDFN4 0.65P and industry standard SOT23-5L.

Features

- Operating Input Voltage Range: 2.2 V to 5.5 V
- Available in Fixed Voltage Option: 1.2 V to 5.3 V
- $\pm 2\%$ Accuracy Over Load/Temperature
- Ultra Low Quiescent Current Typ. 12 μ A
- Standby Current: Typ. 0.1 μ A
- Very Low Dropout: 80 mV at 250 mA
- Ultra High PSRR: Typ. 92 dB at 20 mA, $f = 1$ kHz
- Ultra Low Noise: 6.5 μ V_{RMS}
- Stable with a 1 μ F Small Case Size Ceramic Capacitors
- Available in – WLCSP4: 0.64 mm x 0.64 mm x 0.33 mm
– WLCSP4: 0.64 mm x 0.64 mm x 0.4 mm
– XDFN4: 1 mm x 1 mm x 0.4 mm
– SOT23-5: 2.9 mm x 2.8 mm x 1.2 mm
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Battery-powered Equipment
- Wireless LAN Devices
- Smartphones, Tablets
- Cameras, DVRs, STB and Camcorders

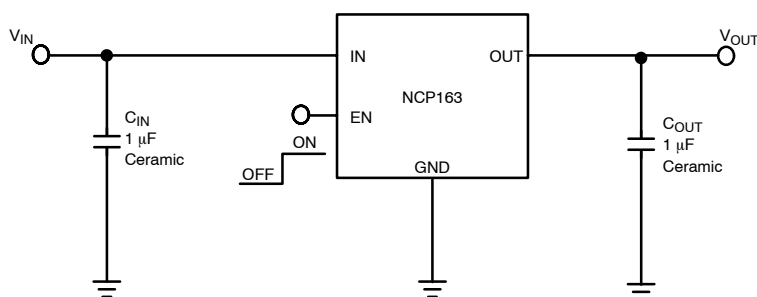
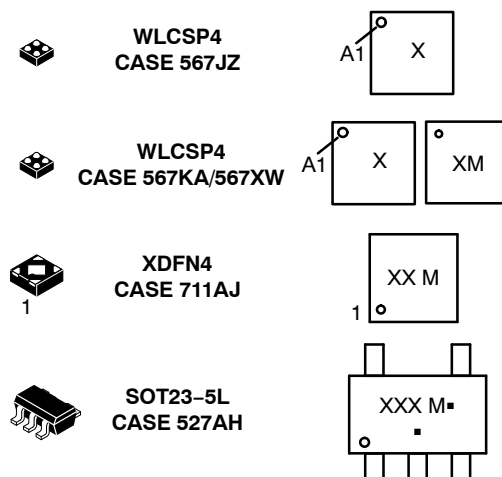


Figure 1. Typical Application Schematics

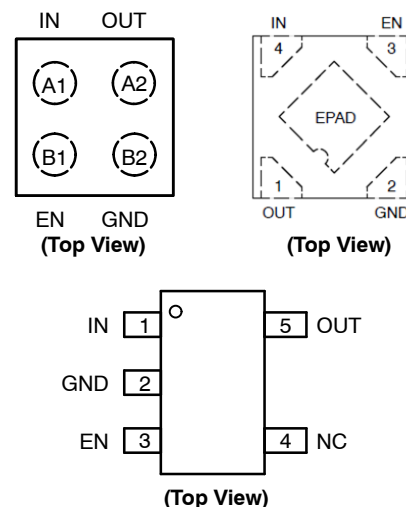
MARKING DIAGRAMS



X, XXX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 18 of this data sheet.

NCP163

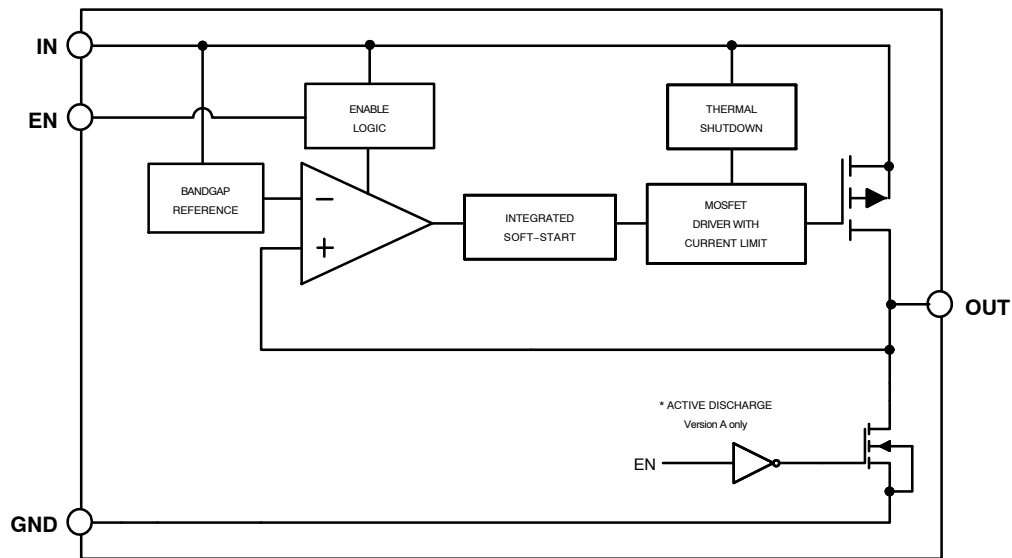


Figure 2. Simplified Schematic Block Diagram

PIN FUNCTION DESCRIPTION

| Pin No. WLCSP4 | Pin No. SOT23-5L | Pin No. XDFN4 | Pin Name | Description |
|----------------|------------------|---------------|----------|--|
| A1 | 1 | 4 | IN | Input voltage supply pin |
| A2 | 5 | 1 | OUT | Regulated output voltage. The output should be bypassed with small 1 μ F ceramic capacitor. |
| B1 | 3 | 3 | EN | Chip enable: Applying $V_{EN} < 0.4$ V disables the regulator, Pulling $V_{EN} > 1.2$ V enables the LDO. |
| B2 | 2 | 2 | GND | Common ground connection |
| – | 4 | – | NC | Not connected. Can be tied to ground plane. |
| – | – | EPAD | EPAD | Exposed pad. Can be tied to ground plane for better power dissipation. |

ABSOLUTE MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|-------------|-----------------------------------|------|
| Input Voltage (Note 1) | V_{IN} | –0.3 V to 6 | V |
| Output Voltage | V_{OUT} | –0.3 to $V_{IN} + 0.3$, max. 6 V | V |
| Chip Enable Input | V_{CE} | –0.3 to 6 V | V |
| Output Short Circuit Duration | t_{SC} | unlimited | s |
| Maximum Junction Temperature | T_J | 150 | °C |
| Storage Temperature | T_{STG} | –55 to 150 | °C |
| ESD Capability, Human Body Model (Note 2) | ESD_{HBM} | 2000 | V |
| ESD Capability, Machine Model (Note 2) | ESD_{MM} | 200 | V |
| ESD Capability, Charged Device Model (Note 2) | ESD_{CDM} | 1000 | V |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
- This device series incorporates ESD protection and is tested by the following methods:
 ESD Human Body Model tested per EIA/JESD22–A114
 ESD Machine Model tested per EIA/JESD22–A115
 ESD Charged Device Model tested per EIA/JESD22–C101, Field Induced Charge Model
 Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

NCP163

THERMAL CHARACTERISTICS

| Rating | Symbol | Value | Unit |
|--|------------------|-------|------|
| Thermal Characteristics, WLCSP4 (Note 3), Thermal Resistance, Junction-to-Air | R _{θJA} | 108 | °C/W |
| Thermal Characteristics, XDFN4 (Note 3), Thermal Resistance, Junction-to-Air | | 198.1 | |
| Thermal Characteristics, SOT23-5 (Note 3), Thermal Resistance, Junction-to-Air | | 218 | |

3. Measured according to JEDEC board specification. Detailed description of the board can be found in JESD51-7

ELECTRICAL CHARACTERISTICS $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$; $V_{IN} = V_{OUT(NOM)} + 1\text{ V}$; $I_{OUT} = 1\text{ mA}$, $C_{IN} = C_{OUT} = 1\text{ }\mu\text{F}$, unless otherwise noted. $V_{EN} = 1.2\text{ V}$. Typical values are at $T_J = +25^{\circ}\text{C}$ (Note 4).

| Parameter | Test Conditions | | Symbol | Min | Typ | Max | Unit |
|------------------------------|---|--|---------------------|-----|----------------------|-------|------|
| Operating Input Voltage | | | V _{IN} | 2.2 | | 5.5 | V |
| Output Voltage Accuracy | V _{IN} = (V _{OUT(NOM)} + 1 V) to 5.5 V 0 mA ≤ I _{OUT} ≤ 250 mA | | V _{OUT} | −2 | | +2 | % |
| | V _{IN} = (V _{OUT(NOM)} + 1 V) to 5.5 V 0 mA ≤ I _{OUT} ≤ 250 mA (for V _{OUT} < 1.8 V, XDFN4 package) | | | −3 | | +3 | |
| | V _{IN} = (V _{OUT(NOM)} + 1 V) to 5.5 V SOT23–5L Package Only | | | −2 | | +2 | |
| Line Regulation | V _{OUT(NOM)} + 1 V ≤ V _{IN} ≤ 5.5 V | | Line _{Reg} | | 0.02 | | %/V |
| Load Regulation | I _{OUT} = 1mA to 250mA | WLCSP, XDFN4 | Load _{Reg} | | 0.001 | | %/mA |
| | | SOT23–5L | | | 0.008 | 0.015 | |
| Dropout Voltage (Note 5) | I _{OUT} = 250 mA (WLCSP, XDFN4 Packages) | V _{OUT(NOM)} = 1.8 V | V _{DO} | | 180 | 250 | mV |
| | | V _{OUT(NOM)} = 2.5 V | | | 110 | 175 | |
| | | V _{OUT(NOM)} = 2.8 V | | | 95 | 160 | |
| | | V _{OUT(NOM)} = 3.0 V | | | 90 | 155 | |
| | | V _{OUT(NOM)} = 3.2 V | | | 85 | 149 | |
| | | V _{OUT(NOM)} = 3.3 V | | | 80 | 145 | |
| | | V _{OUT(NOM)} = 3.5 V | | | 75 | 140 | |
| | | V _{OUT(NOM)} = 4.5 V | | | 65 | 120 | |
| | | V _{OUT(NOM)} = 5.0 V | | | 75 | 105 | |
| Dropout Voltage (Note 5) | I _{OUT} = 250 mA (SOT23–5L Package) | V _{OUT(NOM)} = 1.8 V | V _{DO} | | 205 | 280 | mV |
| | | V _{OUT(NOM)} = 2.8 V | | | 120 | 190 | |
| | | V _{OUT(NOM)} = 3.0 V | | | 115 | 185 | |
| | | V _{OUT(NOM)} = 3.3 V | | | 105 | 175 | |
| Output Current Limit | V _{OUT} = 90% V _{OUT(NOM)} | | I _{CL} | 250 | 700 | | mA |
| Short Circuit Current | V _{OUT} = 0 V | | I _{SC} | | 690 | | |
| Quiescent Current | I _{OUT} = 0 mA | | I _Q | | 12 | 20 | μA |
| Shutdown Current | V _{EN} ≤ 0.4 V, V _{IN} = 4.8 V | | I _{DIS} | | 0.01 | 1 | μA |
| EN Pin Threshold Voltage | EN Input Voltage “H” | | V _{ENH} | 1.2 | | | V |
| | EN Input Voltage “L” | | V _{ENL} | | | 0.4 | |
| EN Pull Down Current | V _{EN} = 4.8 V | | I _{EN} | | 0.2 | 0.5 | μA |
| Turn–On Time | C _{OUT} = 1 μF, From assertion of V _{EN} to V _{OUT} = 95% V _{OUT(NOM)} | “A” Option | | | 120 | | μs |
| | | “C” Option | | | 135 | | |
| Power Supply Rejection Ratio | I _{OUT} = 20 mA | f = 100 Hz f = 1 kHz f = 10 kHz f = 100 kHz | PSRR | | 91 92 85 60 | | dB |

NCP163

ELECTRICAL CHARACTERISTICS $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$; $V_{IN} = V_{OUT(NOM)} + 1\text{ V}$; $I_{OUT} = 1\text{ mA}$, $C_{IN} = C_{OUT} = 1\text{ }\mu\text{F}$, unless otherwise noted. $V_{EN} = 1.2\text{ V}$. Typical values are at $T_J = +25^{\circ}\text{C}$ (Note 4).

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Unit |
|------------------------------------|--|-----------------------------|-----|------------|-----|----------------------------|
| Output Voltage Noise | $f = 10\text{ Hz to }100\text{ kHz}$ $I_{OUT} = 1\text{ mA}$ $I_{OUT} = 250\text{ mA}$ | V_N | | 8.0 6.5 | | μV_{RMS} |
| Thermal Shutdown Threshold | Temperature rising | T_{SDH} | | 160 | | $^{\circ}\text{C}$ |
| | Temperature falling | T_{SDL} | | 140 | | $^{\circ}\text{C}$ |
| Active Output Discharge Resistance | $V_{EN} < 0.4\text{ V}$, Version A only | R_{DIS} | | 280 | | Ω |
| Line Transient (Note 6) | $V_{IN} = (V_{OUT(NOM)} + 1\text{ V})$ to $(V_{OUT(NOM)} + 1.6\text{ V})$ in $30\text{ }\mu\text{s}$, $I_{OUT} = 1\text{ mA}$ | $\text{Tran}_{\text{LINE}}$ | -1 | | | mV |
| | $V_{IN} = (V_{OUT(NOM)} + 1.6\text{ V})$ to $(V_{OUT(NOM)} + 1\text{ V})$ in $30\text{ }\mu\text{s}$, $I_{OUT} = 1\text{ mA}$ | | | | +1 | |
| Load Transient (Note 6) | $I_{OUT} = 1\text{ mA to }200\text{ mA}$ in $10\text{ }\mu\text{s}$ | $\text{Tran}_{\text{LOAD}}$ | -40 | | | mV |
| | $I_{OUT} = 200\text{ mA to }1\text{ mA}$ in $10\text{ }\mu\text{s}$ | | | | +40 | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at $T_A = 25^{\circ}\text{C}$. Low duty cycle pulse techniques are used during the testing to maintain the junction temperature as close to ambient as possible.
- Dropout voltage is characterized when V_{OUT} falls 100 mV below $V_{OUT(NOM)}$.
- Guaranteed by design.

TYPICAL CHARACTERISTICS

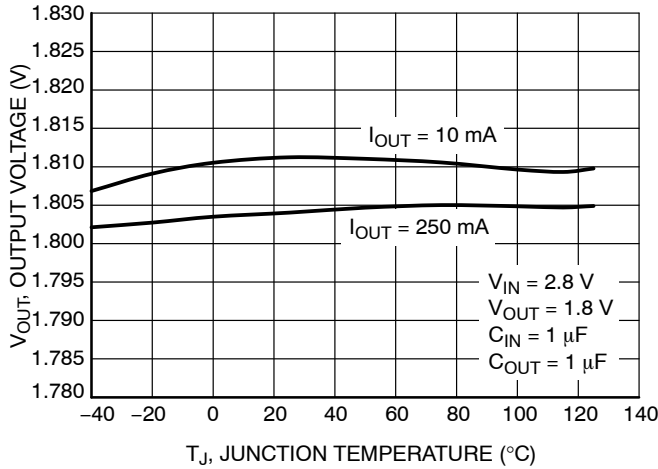


Figure 3. Output Voltage vs. Temperature – $V_{OUT} = 1.8\text{ V}$ – XDFN Package

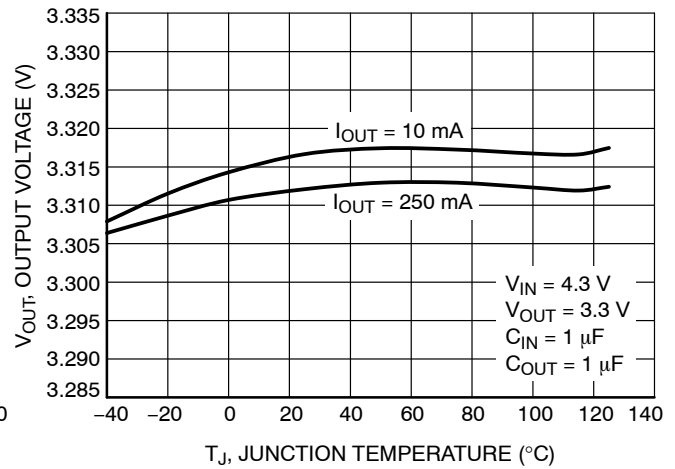


Figure 4. Output Voltage vs. Temperature – $V_{OUT} = 3.3\text{ V}$ – XDFN Package

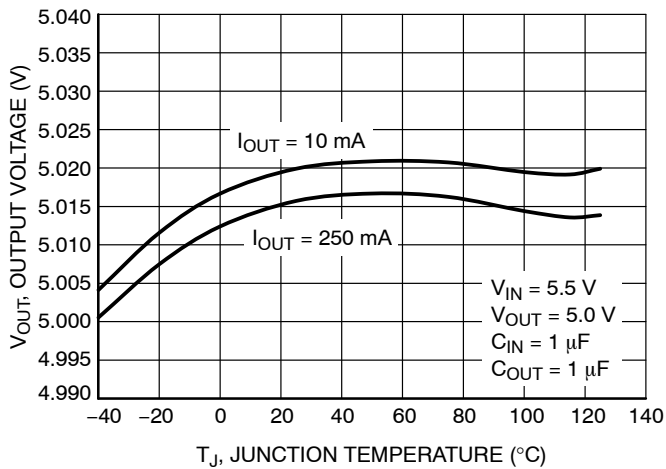


Figure 5. Output Voltage vs. Temperature – $V_{OUT} = 5.0\text{ V}$ – XDFN Package

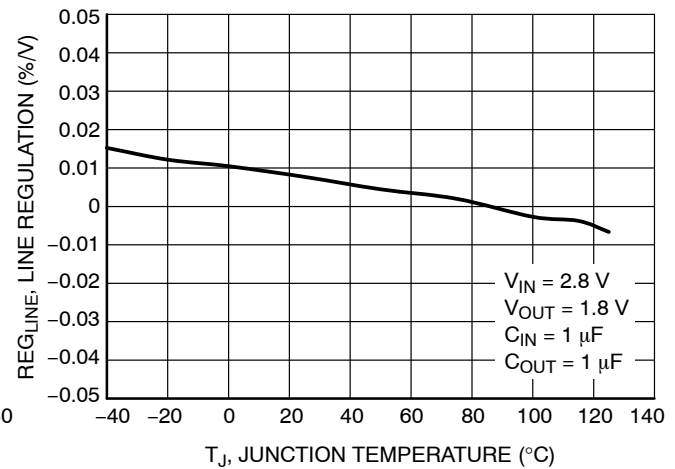


Figure 6. Line Regulation vs. Temperature – $V_{OUT} = 1.8\text{ V}$

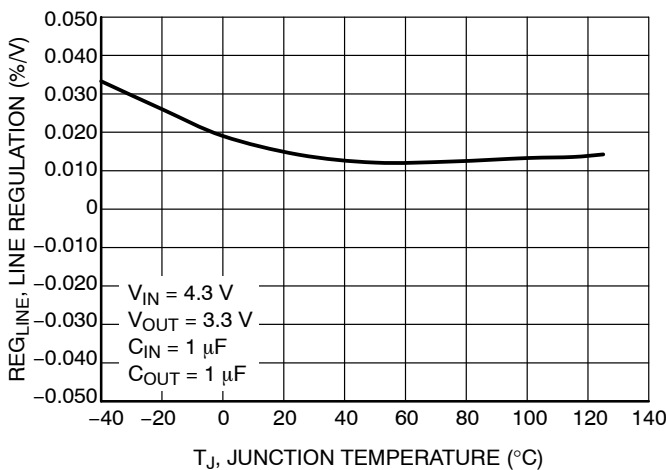


Figure 7. Line Regulation vs. Temperature – $V_{OUT} = 3.3\text{ V}$

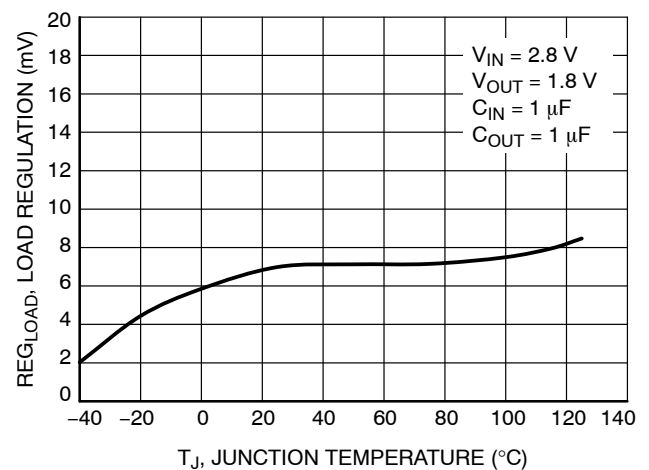


Figure 8. Load Regulation vs. Temperature – $V_{OUT} = 1.8\text{ V}$

TYPICAL CHARACTERISTICS

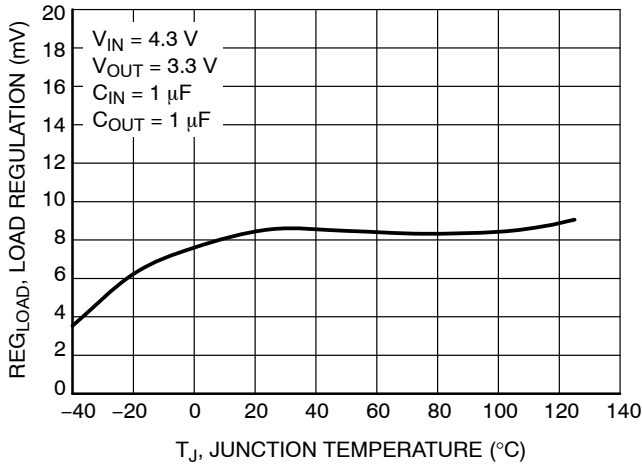


Figure 9. Load Regulation vs. Temperature – $V_{OUT} = 3.3\text{ V}$

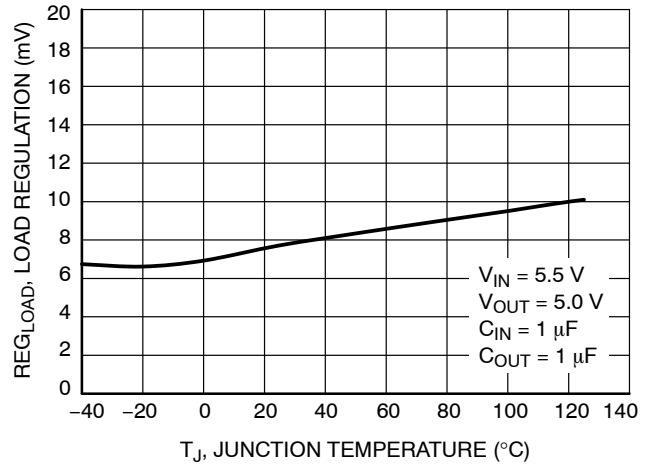


Figure 10. Load Regulation vs. Temperature – $V_{OUT} = 5.0\text{ V}$

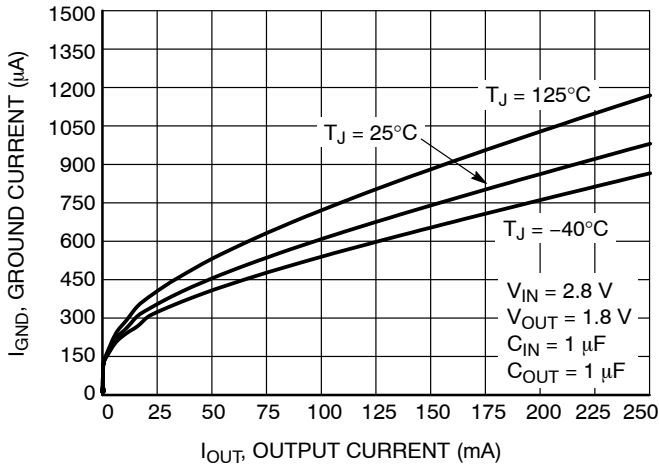


Figure 11. Ground Current vs. Load Current – $V_{OUT} = 1.8\text{ V}$

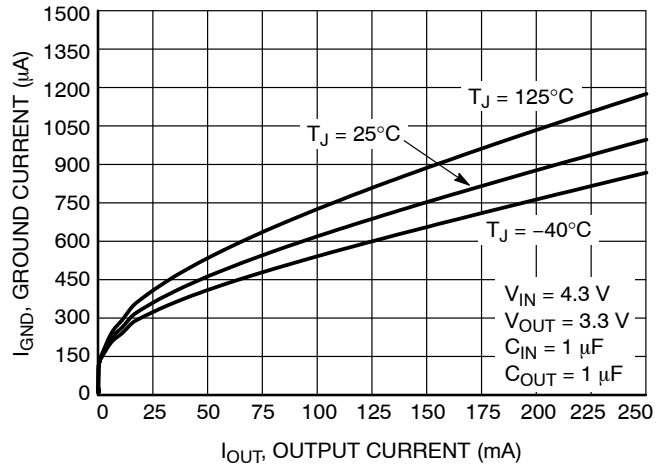


Figure 12. Ground Current vs. Load Current – $V_{OUT} = 3.3\text{ V}$

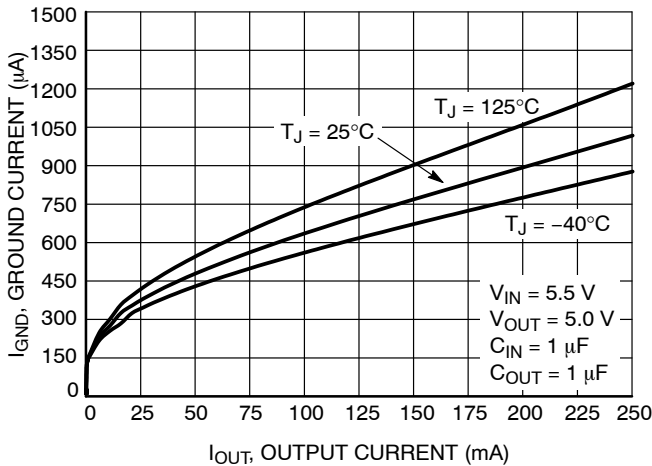


Figure 13. Ground Current vs. Load Current – $V_{OUT} = 5.0\text{ V}$

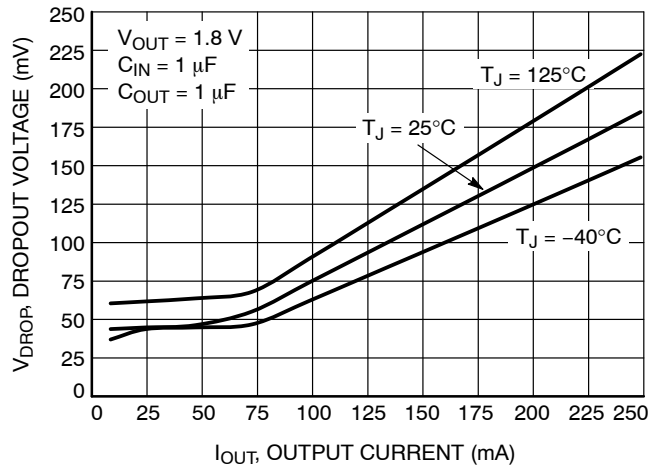


Figure 14. Dropout Voltage vs. Load Current – $V_{OUT} = 1.8\text{ V}$

TYPICAL CHARACTERISTICS

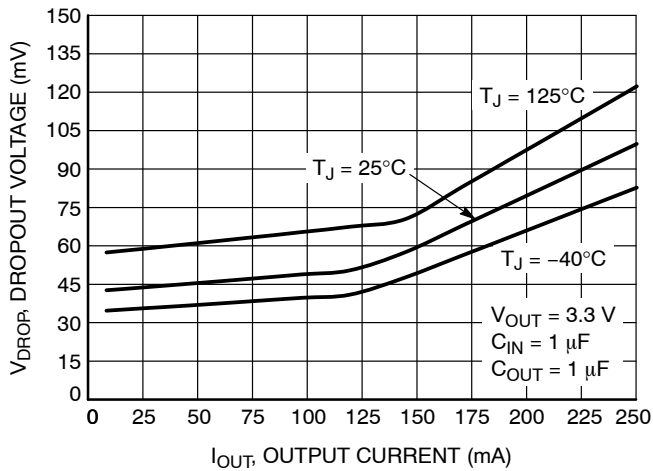


Figure 15. Dropout Voltage vs. Load Current – $V_{OUT} = 3.3\text{ V}$

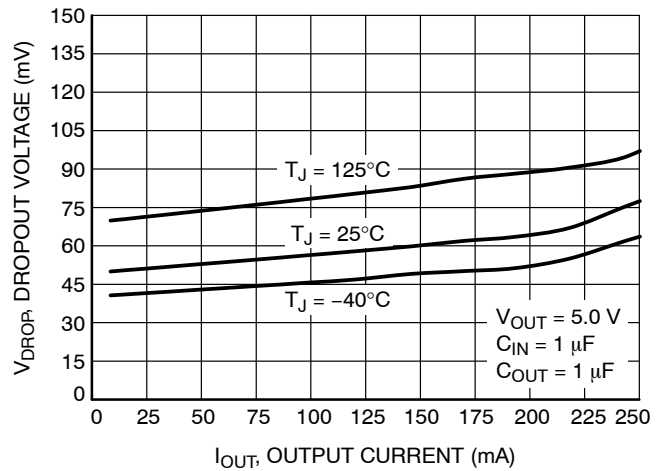


Figure 16. Dropout Voltage vs. Load Current – $V_{OUT} = 5.0\text{ V}$

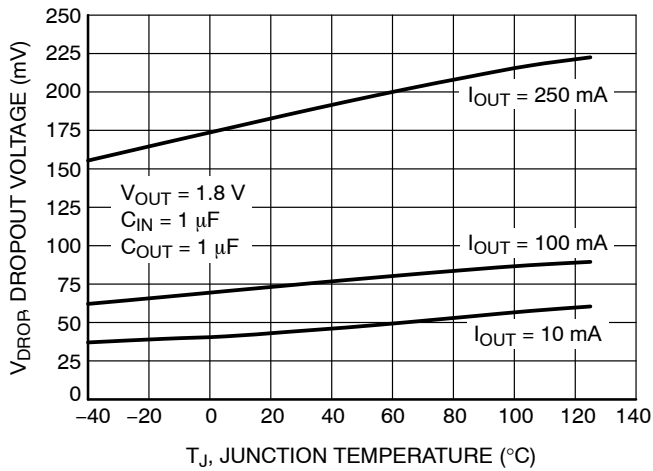


Figure 17. Dropout Voltage vs. Temperature – $V_{OUT} = 1.8\text{ V}$

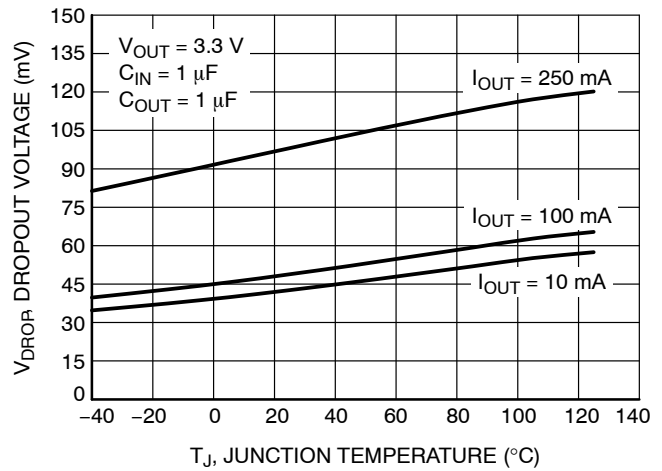


Figure 18. Dropout Voltage vs. Temperature – $V_{OUT} = 3.3\text{ V}$

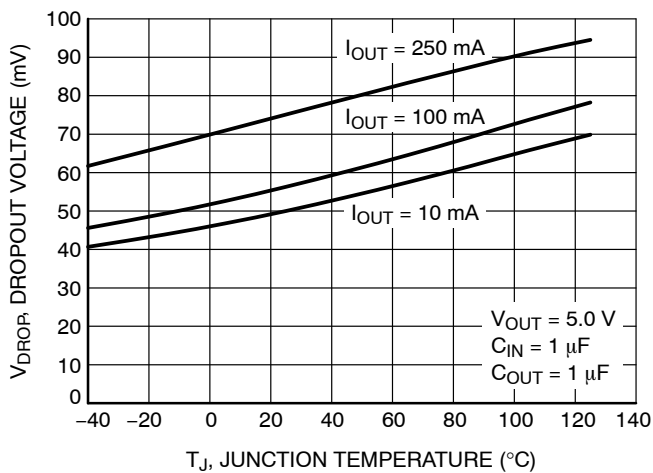


Figure 19. Dropout Voltage vs. Temperature – $V_{OUT} = 5.0\text{ V}$

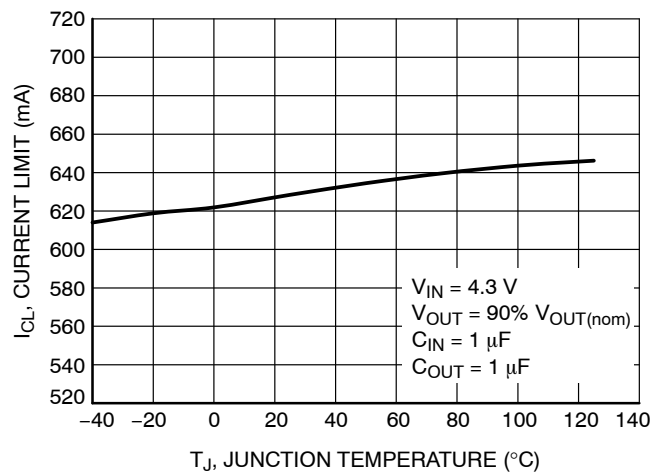


Figure 20. Current Limit vs. Temperature

TYPICAL CHARACTERISTICS

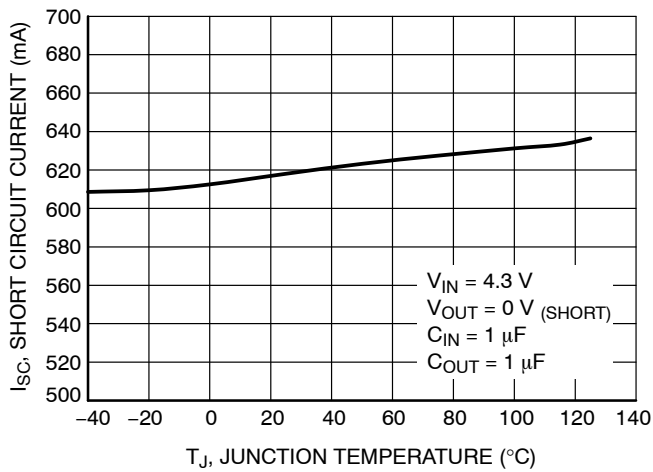


Figure 21. Short Circuit Current vs. Temperature

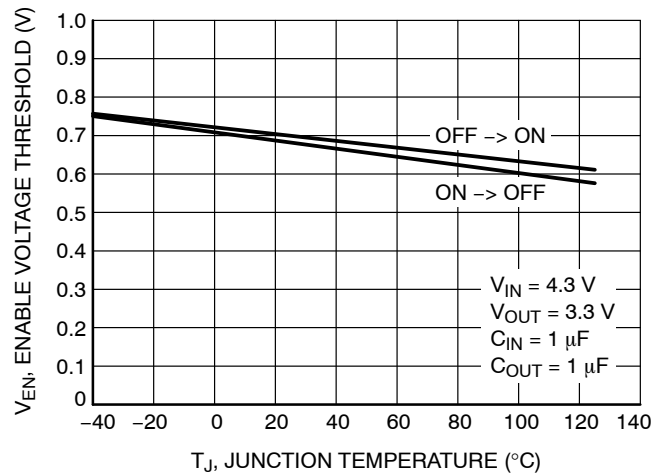


Figure 22. Enable Thresholds Voltage

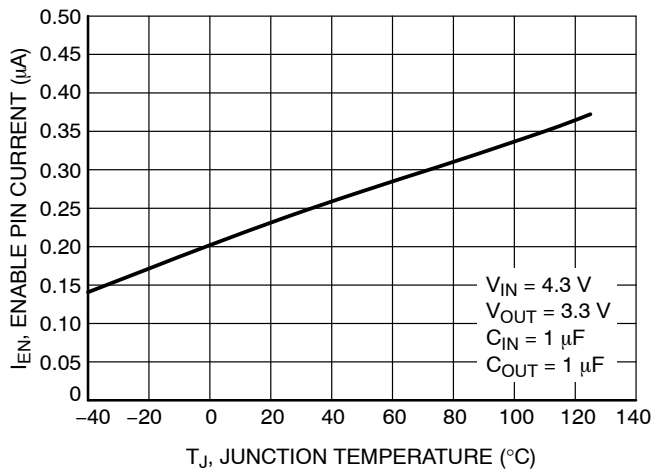


Figure 23. Current to Enable Pin vs. Temperature

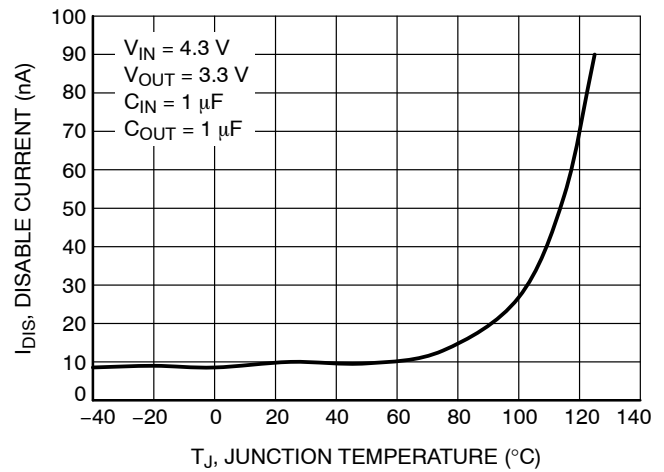


Figure 24. Disable Current vs. Temperature

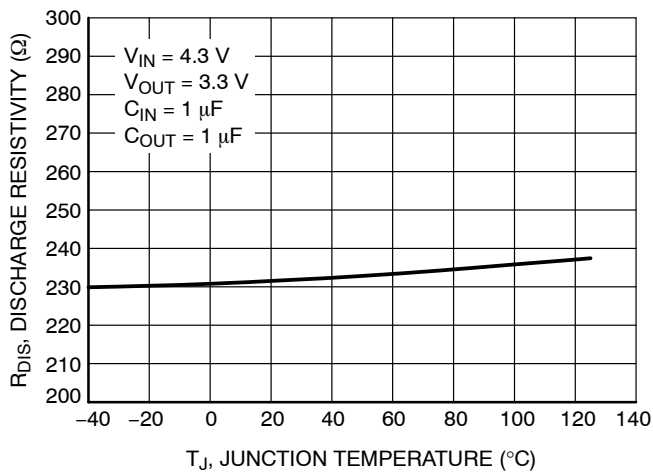


Figure 25. Discharge Resistance vs. Temperature

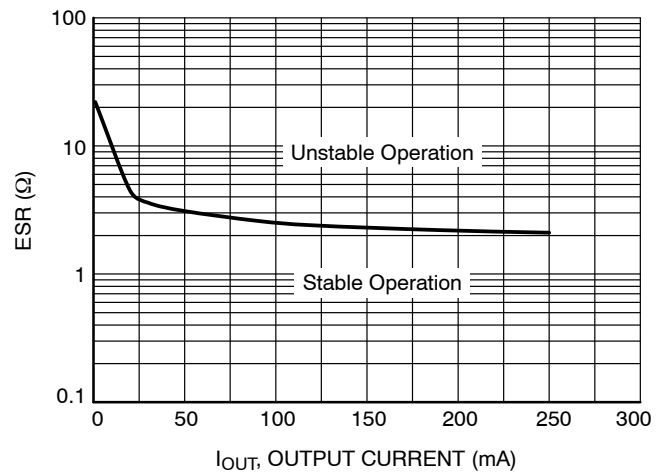


Figure 26. Maximum C_{OUT} ESR Value vs. Load Current

TYPICAL CHARACTERISTICS

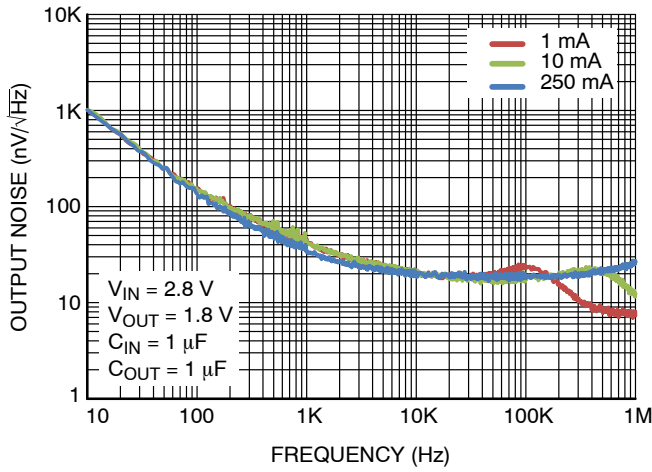


Figure 27. Output Voltage Noise Spectral Density – $V_{OUT} = 1.8\text{ V}$

| I_{OUT} | RMS Output Noise (μV) | |
|-----------|------------------------------------|------------------|
| | 10 Hz – 100 kHz | 100 Hz – 100 kHz |
| 1 mA | 7.73 | 6.99 |
| 10 mA | 7.12 | 6.26 |
| 250 mA | 7.11 | 6.33 |

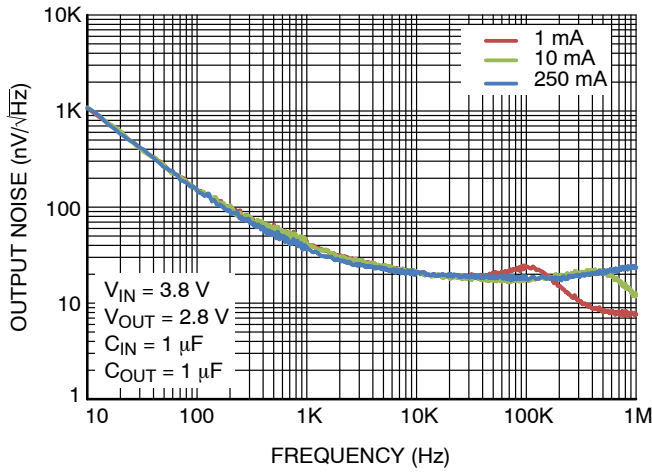


Figure 28. Output Voltage Noise Spectral Density – $V_{OUT} = 2.8\text{ V}$

| I_{OUT} | RMS Output Noise (μV) | |
|-----------|------------------------------------|------------------|
| | 10 Hz – 100 kHz | 100 Hz – 100 kHz |
| 1 mA | 7.9 | 7.07 |
| 10 mA | 7.19 | 6.25 |
| 250 mA | 7.29 | 6.38 |

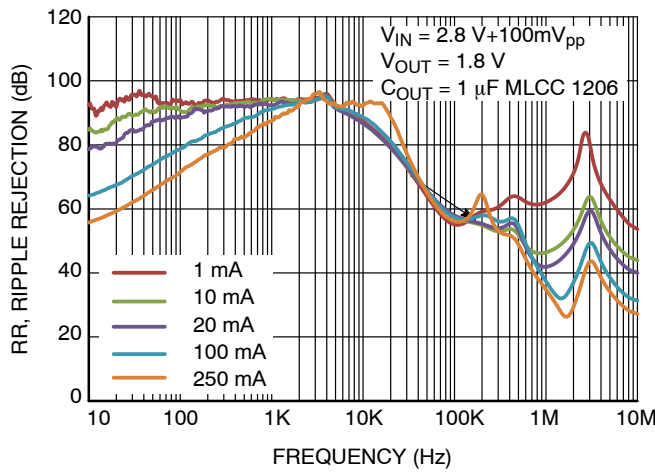


Figure 29. Power Supply Rejection Ratio – $V_{OUT} = 1.8\text{ V}$

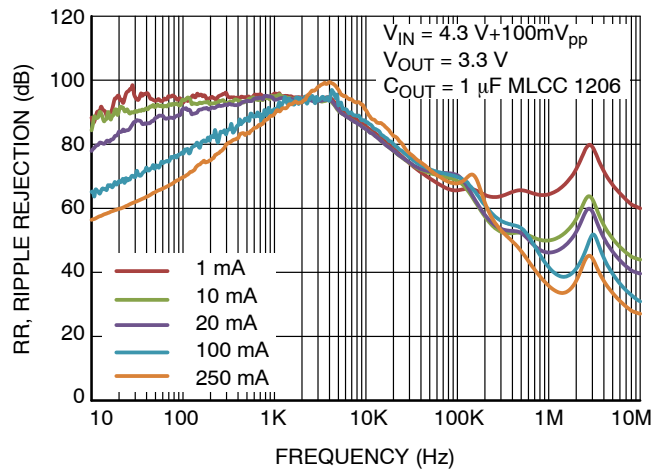


Figure 30. Power Supply Rejection Ratio – $V_{OUT} = 3.3\text{ V}$

TYPICAL CHARACTERISTICS

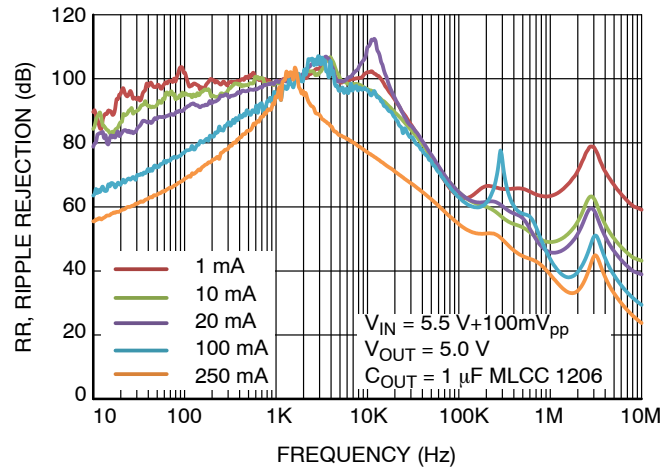


Figure 31. Power Supply Rejection Ratio – $V_{OUT} = 5.0\text{ V}$

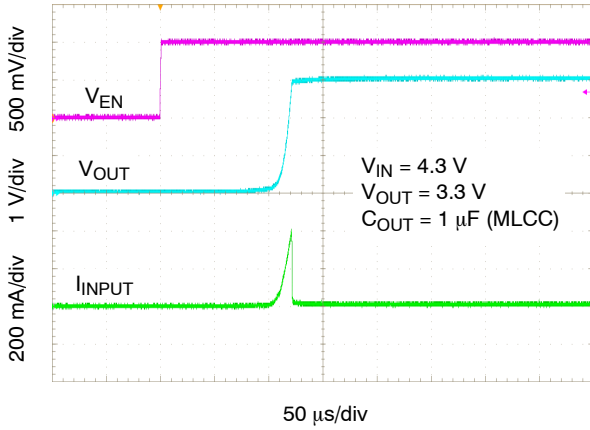


Figure 32. Enable Turn-on Response – $C_{OUT} = 1\text{ }\mu\text{F}$, $I_{OUT} = 10\text{ mA}$ – “A” Option

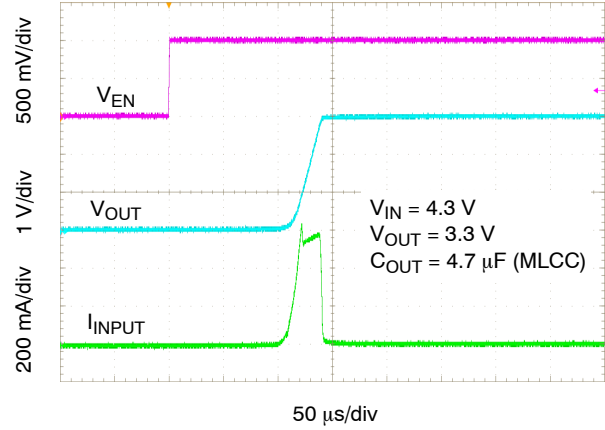


Figure 33. Enable Turn-on Response – $C_{OUT} = 4.7\text{ }\mu\text{F}$, $I_{OUT} = 10\text{ mA}$ – “A” Option

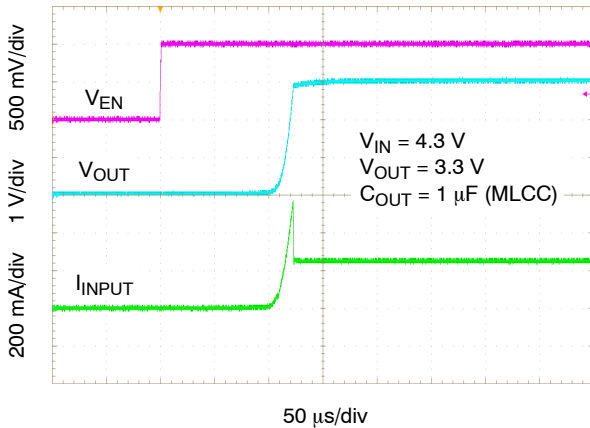


Figure 34. Enable Turn-on Response – $C_{OUT} = 1\text{ }\mu\text{F}$, $I_{OUT} = 250\text{ mA}$ – “A” Option

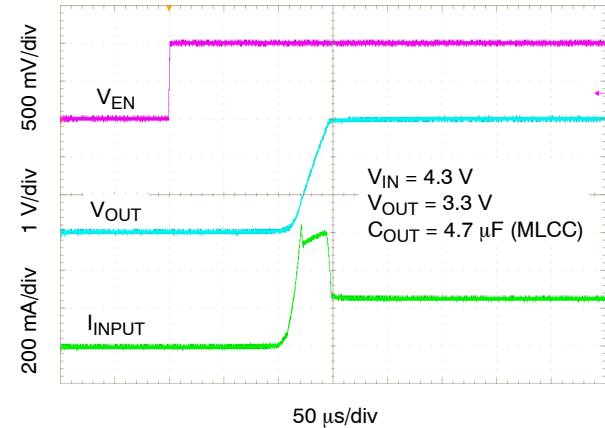
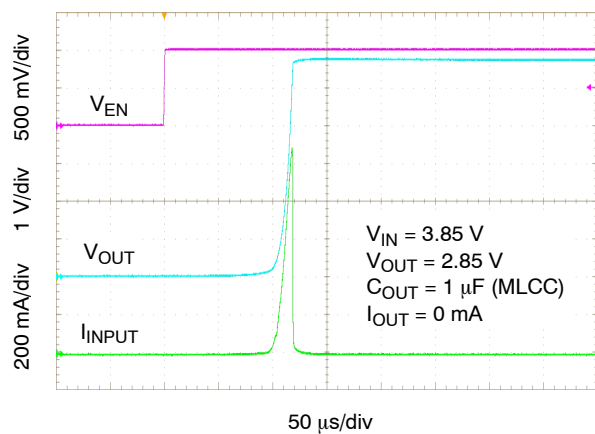
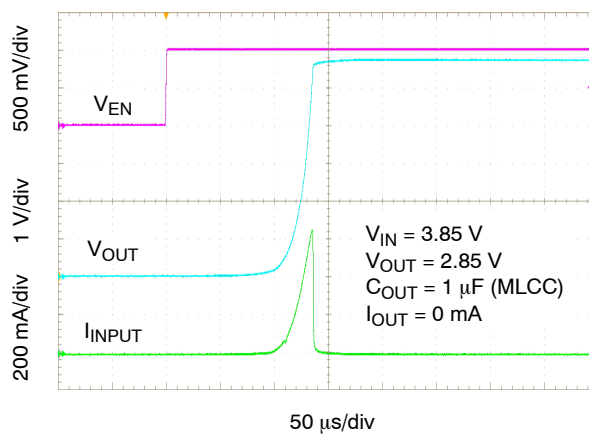


Figure 35. Enable Turn-on Response – $C_{OUT} = 4.7\text{ }\mu\text{F}$, $I_{OUT} = 250\text{ mA}$ – “A” Option

TYPICAL CHARACTERISTICS

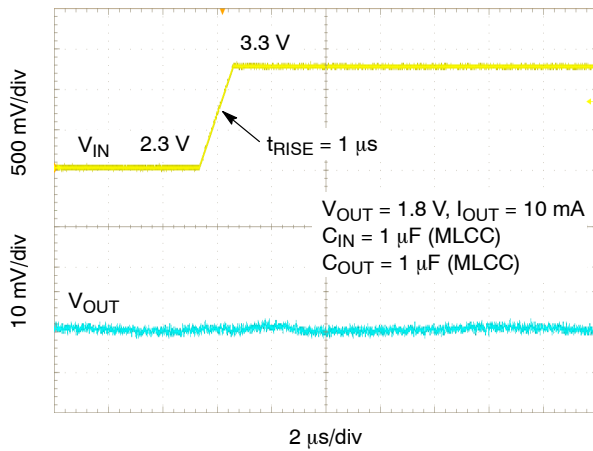


**Figure 36. Enable Turn-on Response –
 $C_{OUT} = 1$ μ F – “A” Option – Normal**

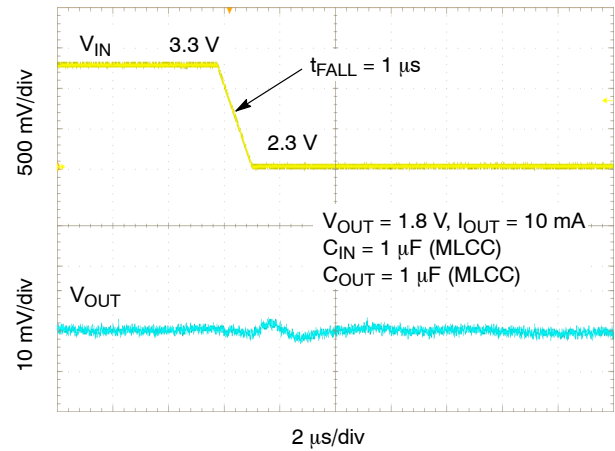


**Figure 37. Enable Turn-on Response –
 $C_{OUT} = 1$ μ F – “C” Option – Slow**

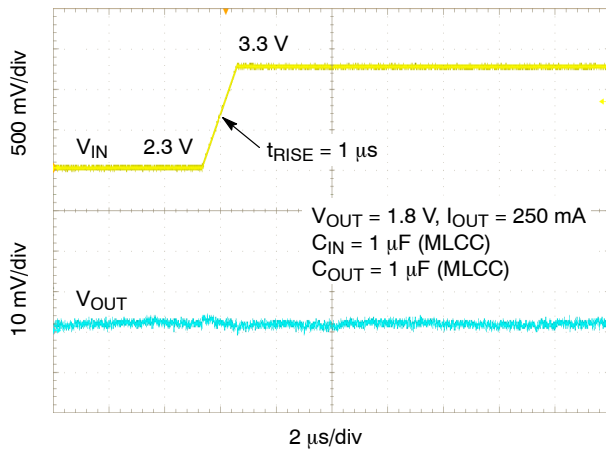
TYPICAL CHARACTERISTICS



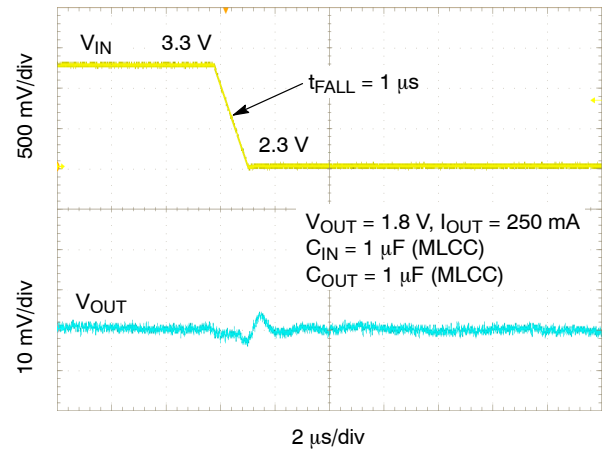
**Figure 38. Line Transient Response –
 $I_{OUT} = 10\text{ mA}$**



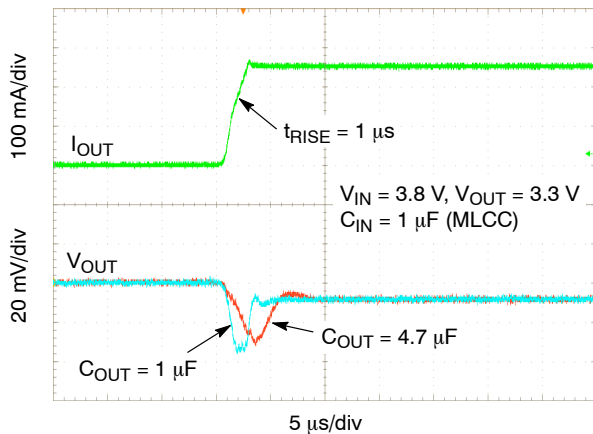
**Figure 39. Line Transient Response –
 $I_{OUT} = 10\text{ mA}$**



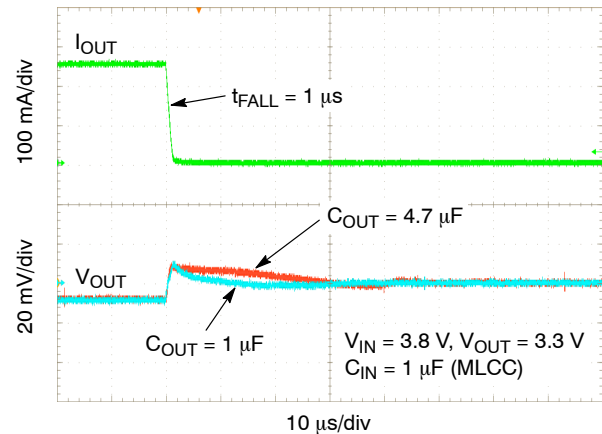
**Figure 40. Line Transient Response –
 $I_{OUT} = 250\text{ mA}$**



**Figure 41. Line Transient Response –
 $I_{OUT} = 250\text{ mA}$**



**Figure 42. Load Transient Response –
1 mA to 250 mA**



**Figure 43. Load Transient Response –
250 mA to 1 mA**

TYPICAL CHARACTERISTICS

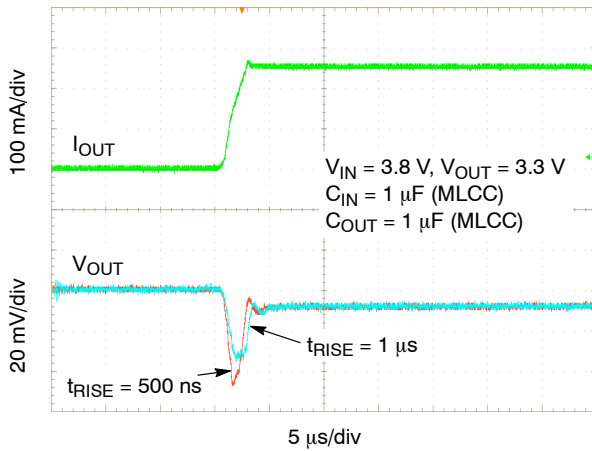


Figure 44. Load Transient Response –
1 mA to 250 mA

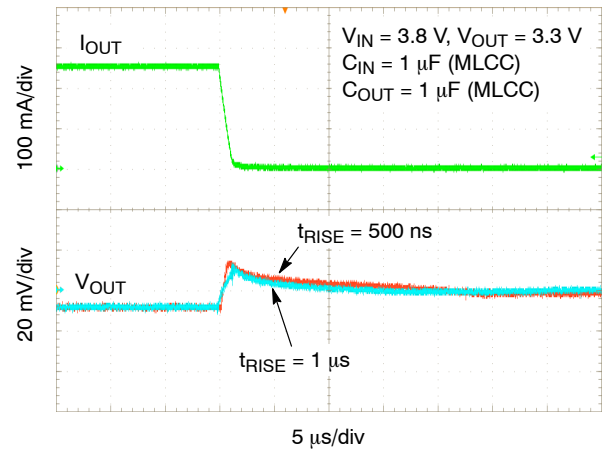


Figure 45. Load Transient Response –
250 mA to 1 mA

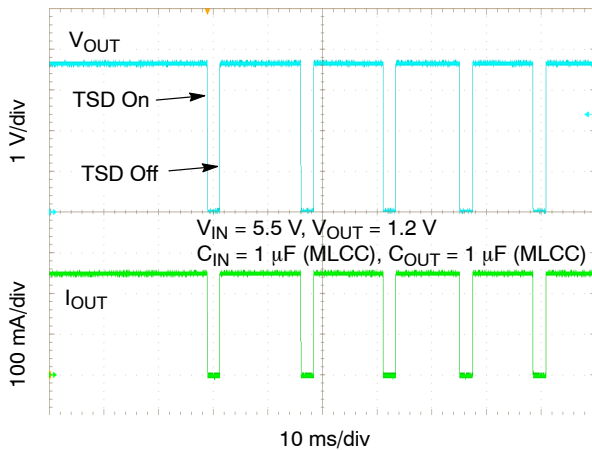


Figure 46. Overheating Protection – TSD

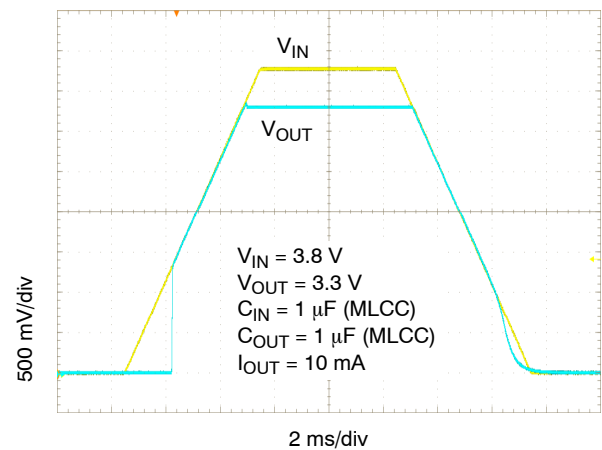


Figure 47. Turn-on/off – Slow Rising V_{IN}

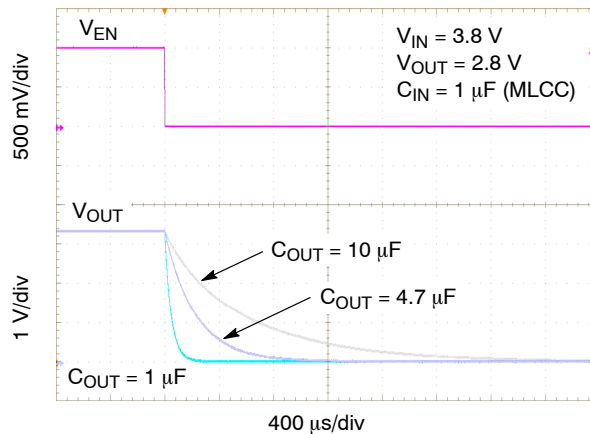


Figure 48. Enable Turn-off – Various Output
Capacitors

APPLICATIONS INFORMATION

General

The NCP163 is an ultra-low noise 250 mA low dropout regulator designed to meet the requirements of RF applications and high performance analog circuits. The NCP163 device provides very high PSRR and excellent dynamic response. In connection with low quiescent current this device is well suitable for battery powered application such as cell phones, tablets and other. The NCP163 is fully protected in case of current overload, output short circuit and overheating.

Input Capacitor Selection (C_{IN})

Input capacitor connected as close as possible is necessary for ensure device stability. The X7R or X5R capacitor should be used for reliable performance over temperature range. The value of the input capacitor should be 1 μ F or greater to ensure the best dynamic performance. This capacitor will provide a low impedance path for unwanted AC signals or noise modulated onto constant input voltage. There is no requirement for the ESR of the input capacitor but it is recommended to use ceramic capacitors for their low ESR and ESL. A good input capacitor will limit the influence of input trace inductance and source resistance during sudden load current changes.

Output Decoupling (C_{OUT})

The NCP163 requires an output capacitor connected as close as possible to the output pin of the regulator. The recommended capacitor value is 1 μ F and X7R or X5R dielectric due to its low capacitance variations over the specified temperature range. The NCP163 is designed to remain stable with minimum effective capacitance of 0.7 μ F to account for changes with temperature, DC bias and package size. Especially for small package size capacitors such as 0201 the effective capacitance drops rapidly with the applied DC bias. Please refer Figure 49.

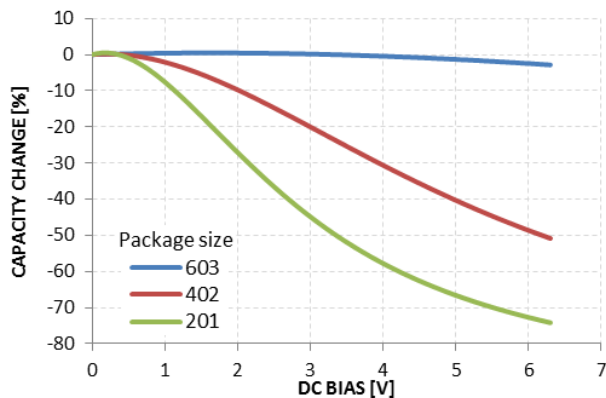


Figure 49. Capacity vs DC Bias Voltage

There is no requirement for the minimum value of Equivalent Series Resistance (ESR) for the C_{OUT} but the maximum value of ESR should be less than 2 Ω . Larger output capacitors and lower ESR could improve the load

transient response or high frequency PSRR. It is not recommended to use tantalum capacitors on the output due to their large ESR. The equivalent series resistance of tantalum capacitors is also strongly dependent on the temperature, increasing at low temperature.

Enable Operation

The NCP163 uses the EN pin to enable/disable its device and to deactivate/activate the active discharge function.

If the EN pin voltage is <0.4 V the device is guaranteed to be disabled. The pass transistor is turned-off so that there is virtually no current flow between the IN and OUT. The active discharge transistor is active so that the output voltage V_{OUT} is pulled to GND through a 280 Ω resistor. In the disable state the device consumes as low as typ. 10 nA from the V_{IN} .

If the EN pin voltage >1.2 V the device is guaranteed to be enabled. The NCP163 regulates the output voltage and the active discharge transistor is turned-off.

The EN pin has internal pull-down current source with typ. value of 200 nA which assures that the device is turned-off when the EN pin is not connected. In the case where the EN function isn't required the EN should be tied directly to IN.

The NCP163 provides soft-start feature ensures smooth monotonous output voltage rising. It prevents excessive input current after EN pin turn-on when big output capacitance is connected.

There are two slew-rate options of start-up ramp. The normal "A" option and slower "C" option. For more information please refer ordering information table.

Output Current Limit

Output Current is internally limited within the IC to a typical 700 mA. The NCP163 will source this amount of current measured with a voltage drops on the 90% of the nominal V_{OUT} . If the Output Voltage is directly shorted to ground ($V_{OUT} = 0$ V), the short circuit protection will limit the output current to 690 mA (typ). The current limit and short circuit protection will work properly over whole temperature range and also input voltage range. There is no limitation for the short circuit duration.

Thermal Shutdown

When the die temperature exceeds the Thermal Shutdown threshold ($T_{SD} = 160^\circ\text{C}$ typical), Thermal Shutdown event is detected and the device is disabled. The IC will remain in this state until the die temperature decreases below the Thermal Shutdown Reset threshold ($T_{SDU} = 140^\circ\text{C}$ typical). Once the IC temperature falls below the 140°C the LDO is enabled again. The thermal shutdown feature provides the protection from a catastrophic device failure due to accidental overheating. This protection is not intended to be used as a substitute for proper heat sinking.

Power Dissipation

As power dissipated in the NCP163 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part.

The maximum power dissipation the NCP163 can handle is given by:

$$P_{D(MAX)} = \frac{[125^{\circ}\text{C} - T_A]}{\theta_{JA}} \quad (\text{eq. 1})$$

The power dissipated by the NCP163 for given application conditions can be calculated from the following equations:

$$P_D \approx V_{IN} \cdot I_{GND} + I_{OUT}(V_{IN} - V_{OUT}) \quad (\text{eq. 2})$$

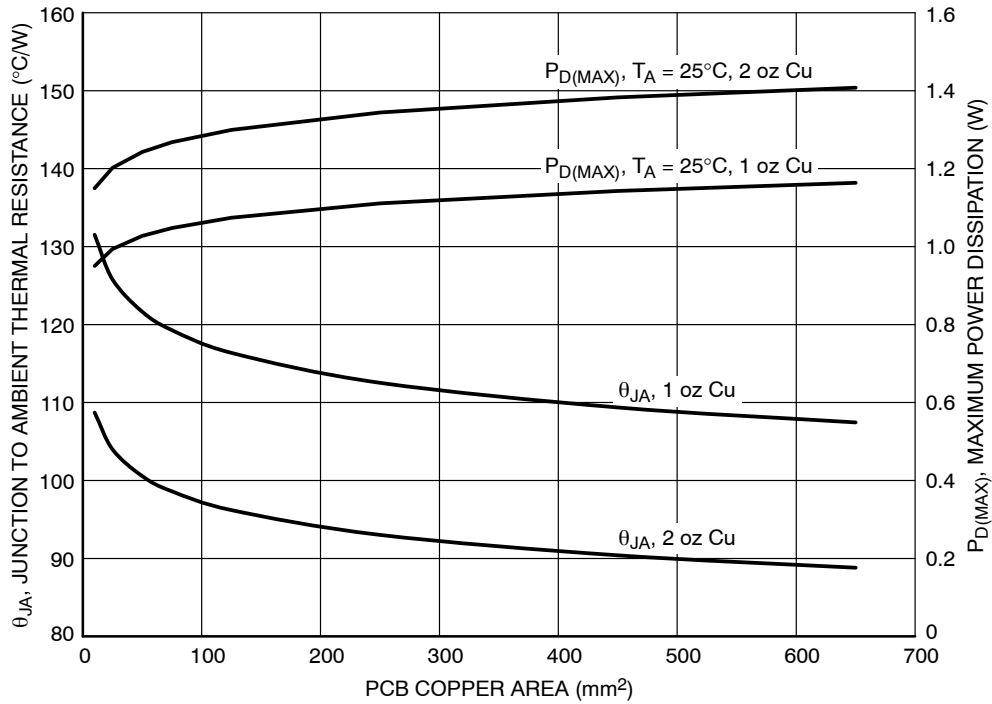


Figure 50. θ_{JA} and $P_{D(MAX)}$ vs. Copper Area (CSP4)

NCP163

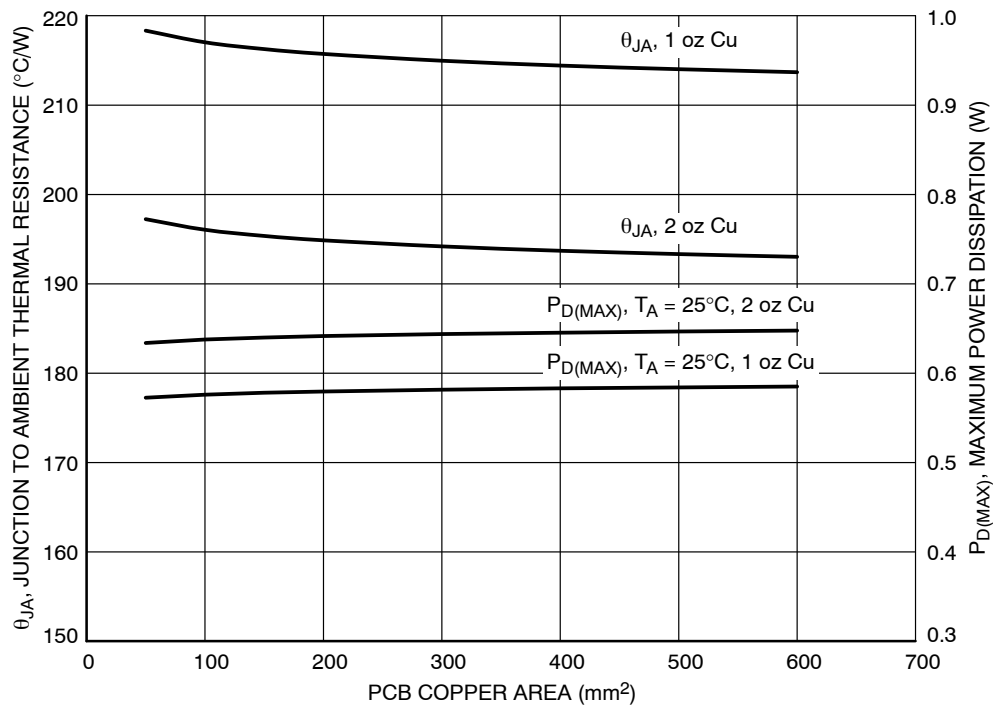


Figure 51. θ_{JA} and $P_{D(MAX)}$ vs. Copper Area (XDFN4)

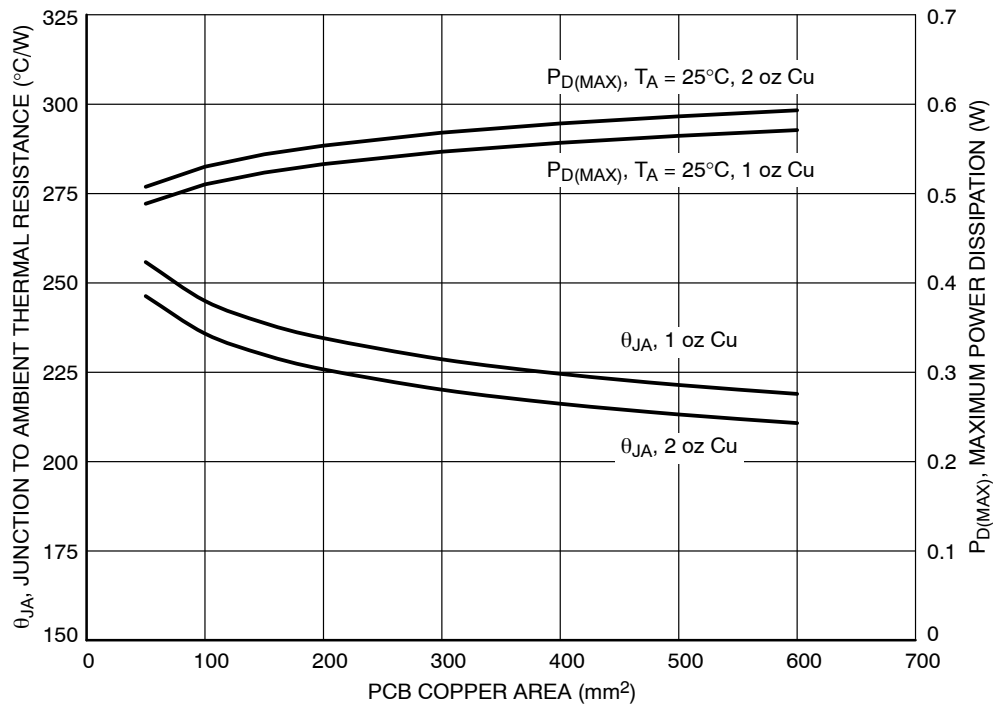


Figure 52. θ_{JA} and $P_{D(MAX)}$ vs. Copper Area (SOT23-5L)

NCP163

Reverse Current

The PMOS pass transistor has an inherent body diode which will be forward biased in the case that $V_{OUT} > V_{IN}$. Due to this fact in cases, where the extended reverse current condition can be anticipated the device may require additional external protection.

Power Supply Rejection Ratio

The NCP163 features very high Power Supply Rejection ratio. If desired the PSRR at higher frequencies in the range 100 kHz – 10 MHz can be tuned by the selection of C_{OUT} capacitor and proper PCB layout.

Turn-On Time

The turn-on time is defined as the time period from EN assertion to the point in which V_{OUT} will reach 98% of its nominal value. This time is dependent on various application conditions such as $V_{OUT(NOM)}$, C_{OUT} , T_A .

PCB Layout Recommendations

To obtain good transient performance and good regulation characteristics place C_{IN} and C_{OUT} capacitors close to the device pins and make the PCB traces wide. In order to minimize the solution size, use 0402 or 0201 capacitors with appropriate capacity. Larger copper area connected to the pins will also improve the device thermal resistance. The actual power dissipation can be calculated from the equation above (Equation 2). Expose pad can be tied to the GND pin for improvement power dissipation and lower device temperature.

NCP163

ORDERING INFORMATION (WLCSP4)

| Device | Voltage Option | Marking | Rotation | Description | Package | Shipping [†] |
|-------------------|----------------|----------------|----------|---|-----------------------------------|---------------------------|
| NCP163AFCS120T2G | 1.2 V | 2 | 0 | 250 mA, Active Discharge | WLCSP4 CASE 567KA (Pb-Free) | 5000 / Tape & Reel |
| NCP163AFCS180T2G | 1.8 V | Y | 180 | | | |
| NCP163AFCS250T2G | 2.5 V | T | 270 | | | |
| NCP163AFCS260T2G | 2.6 V | 4 | 180 | | | |
| NCP163AFCS270T2G | 2.7 V | V | 270 | | | |
| NCP163AFCS280T2G | 2.8 V | 3 | 180 | | | |
| NCP163AFCS285T2G | 2.85 V | 5 | 180 | | | |
| NCP163AFCS290T2G | 2.9 V | 6 | 180 | | | |
| NCP163AFCS2925T2G | 2.925 V | 2 | 180 | | | |
| NCP163BFCS180T2G | 1.8 V | Y | 270 | 250 mA, Non-Active Discharge | | |
| NCP163BFCS2925T2G | 2.925 V | 2 | 270 | | | |
| | | | | | | |
| NCP163CFCS285T2G | 2.85 V | P | 180 | 250 mA, Active Discharge Slow Turn-On Slew | WLCSP4 CASE 567XW (Pb-Free) | 10000 / Tape & Reel |
| | | | | | | |
| NCP163AFCT120T2G | 1.2 V | \overline{A} | 0 | 250 mA, Active Discharge | WLCSP4 CASE 567JZ (Pb-Free) | 5000 / Tape & Reel |
| NCP163AFCT180T2G | 1.8 V | Y | 180 | | | |
| NCP163AFCT250T2G | 2.5 V | Y | 90 | | | |
| NCP163AFCT260T2G | 2.6 V | 6 | 270 | | | |
| NCP163AFCT270T2G | 2.7 V | 5 | 180 | | | |
| NCP163AFCT280T2G | 2.8 V | 3 | 180 | | | |
| NCP163AFCT285T2G | 2.85 V | 5 | 270 | | | |
| NCP163AFCT290T2G | 2.9 V | 4 | 270 | | | |
| NCP163AFCT2925T2G | 2.925 V | 2 | 180 | | | |
| NCP163AFCT300T2G | 3.0 V | 3 | 270 | | | |
| NCP163AFCT330T2G | 3.3 V | 6 | 90 | | | |
| NCP163BFCT180T2G | 1.8 V | Y | 270 | 250 mA, Non-Active Discharge | | |
| NCP163BFCT2925T2G | 2.925 V | 2 | 270 | | | |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

NCP163

ORDERING INFORMATION (XDFN4)

| Device | Voltage Option | Marking | Description | Package | Shipping [†] |
|-------------------------------------|----------------|---------|---------------------------------|----------------------------------|---|
| NCP163AMX120TBG* (Note 7) | 1.2 V | ME | 250 mA, Active Discharge | XDFN4 CASE 711AJ (Pb-Free) | 3000 or 5000 / Tape & Reel (Note 7) |
| NCP163AMX130TBG* (Note 7) | 1.3 V | MG | | | |
| NCP163AMX150TBG | 1.5 V | MV | | | |
| NCP163AMX180TBG (Note 7) | 1.8 V | MA | | | |
| NCP163AMX1825TBG (Note 7) | 1.825 V | MC | | | |
| NCP163AMX185TBG (In Development) | 1.85 V | MZ | | | |
| NCP163AMX190TBG | 1.9 V | MH | | | |
| NCP163AMX250TBG | 2.5 V | MU | | | |
| NCP163AMX260TBG | 2.6 V | MN | | | |
| NCP163AMX270TBG (Note 7) | 2.7 V | MX | | | |
| NCP163AMX275TBG | 2.75 V | MD | | | |
| NCP163AMX280TBG (Note 7) | 2.8 V | MM | | | |
| NCP163AMX285TBG | 2.85 V | MQ | | | |
| NCP163AMX290TBG (Note 7) | 2.9 V | MR | | | |
| NCP163AMX300TBG (Note 7) | 3.0 V | MJ | | | |
| NCP163AMX330TBG (Note 7) | 3.3 V | MK | | | |
| NCP163AMX500TBG (Note 7) | 5.0 V | ML | | | |
| NCP163BMX180TBG (Note 7) | 1.8 V | PA | 250 mA, Non-Active Discharge | XDFN4 CASE 711AJ (Pb-Free) | 3000 or 5000 / Tape & Reel (Note 7) |
| NCP163BMX1825TBG (Note 7) | 1.825 V | PC | | | |
| NCP163BMX275TBG | 2.75 V | PD | | | |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

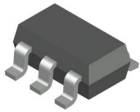
*Contact sales office for availability information.

7. Product processed after October 1, 2022 are shipped with quantity 5000 units / tape & reel.

ORDERING INFORMATION (SOT23-5L)

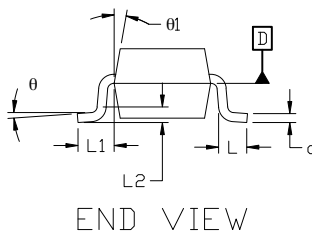
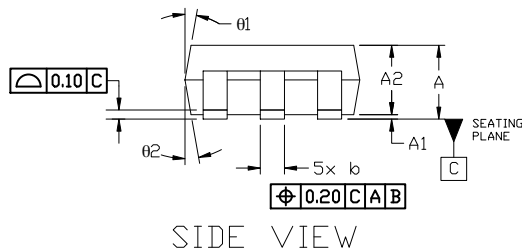
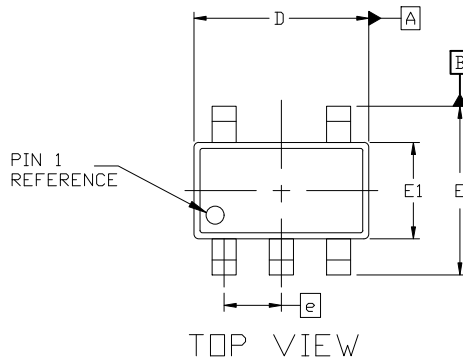
| Device | Voltage Option | Marking | Description | Package | Shipping [†] |
|-----------------|----------------|---------|--------------------------|-------------------------------------|-----------------------|
| NCP163ASN150T1G | 1.5 V | KAK | 250 mA, Active Discharge | SOT23-5L CASE 527AH (Pb-Free) | 3000 / Tape & Reel |
| NCP163ASN180T1G | 1.8 V | KAA | | | |
| NCP163ASN250T1G | 2.5 V | KAD | | | |
| NCP163ASN270T1G | 2.7 V | KAL | | | |
| NCP163ASN280T1G | 2.8 V | KAE | | | |
| NCP163ASN300T1G | 3.0 V | KAF | | | |
| NCP163ASN330T1G | 3.3 V | KAG | | | |
| NCP163ASN350T1G | 3.5 V | KAH | | | |
| NCP163ASN500T1G | 5.0 V | KAJ | | | |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

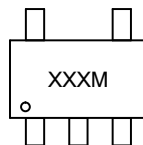


SOT-23, 5 Lead CASE 527AH ISSUE A

DATE 09 JUN 2021



GENERIC MARKING DIAGRAM*



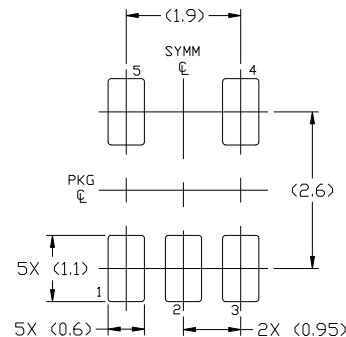
XXX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1989A
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.25 PER SIDE. D AND E1 DIMENSIONS ARE DETERMINED AT DATUM D.
5. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL NOT BE LESS THAN 0.07mm.

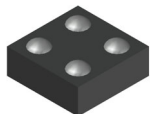
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|-----|-------------|------|------|
| | MIN. | NOM. | MAX. |
| A | 0.90 | — | 1.45 |
| A1 | 0.00 | — | 0.15 |
| A2 | 0.90 | 1.15 | 1.30 |
| b | 0.30 | — | 0.50 |
| c | 0.08 | — | 0.22 |
| D | 2.90 BSC | | |
| E | 2.80 BSC | | |
| E1 | 1.60 BSC | | |
| e | 0.95 BSC | | |
| L | 0.30 | 0.45 | 0.60 |
| L1 | 0.60 REF | | |
| L2 | 0.25 REF | | |
| θ | 0° | 4° | 8° |
| θ1 | 0° | 10° | 15° |
| θ2 | 0° | 10° | 15° |



For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

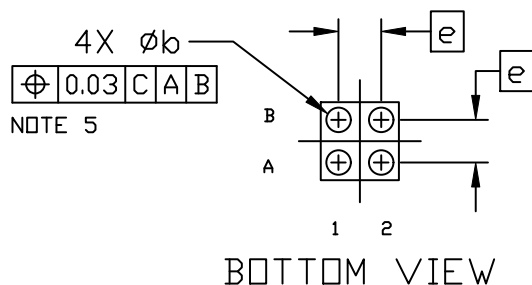
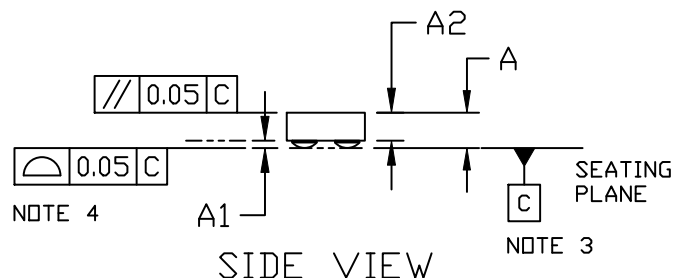
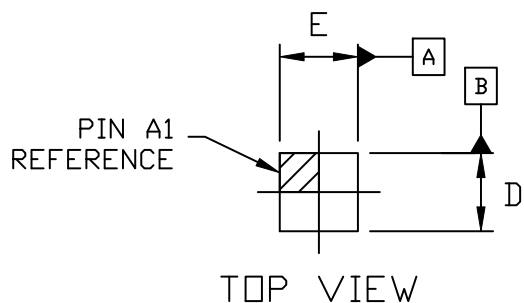
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WLCSP4, 0.64x0.64x0.33
CASE 567JZ
ISSUE B

DATE 16 MAY 2022



GENERIC MARKING DIAGRAM*



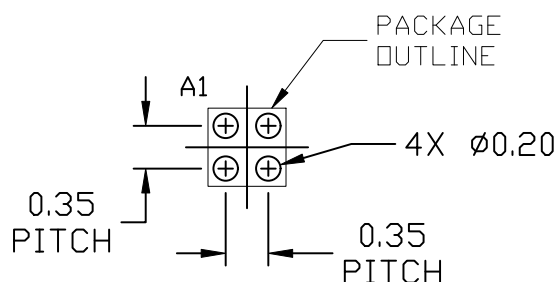
X = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BUMPS.
4. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BUMPS.
5. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM C.

| DIM | MILLIMETERS | | |
|-----|-------------|-------|-------|
| | MIN. | NOM. | MAX. |
| A | --- | --- | 0.33 |
| A1 | 0.04 | 0.06 | 0.08 |
| A2 | 0.23 REF | | |
| b | 0.180 | 0.200 | 0.220 |
| D | 0.610 | 0.640 | 0.670 |
| E | 0.610 | 0.640 | 0.670 |
| e | 0.35 BSC | | |



RECOMMENDED MOUNTING FOOTPRINT * (NSMD PAD TYPE)

- * For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

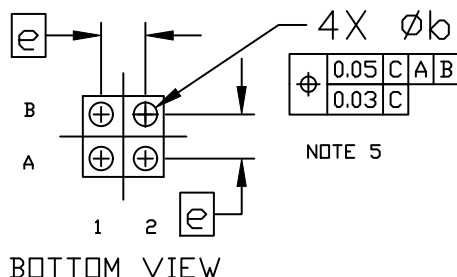
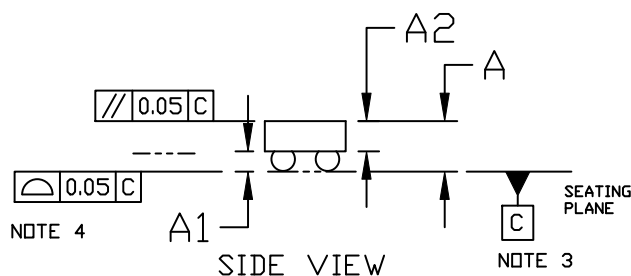
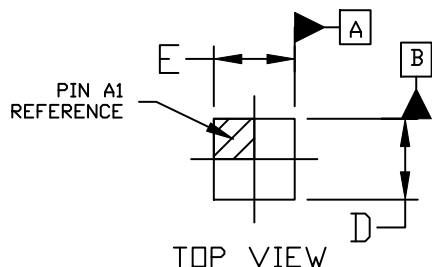
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SCALE 4:1

WLCSP4, 0.64x0.64
CASE 567KA
ISSUE B

DATE 24 MAR 2020



GENERIC MARKING DIAGRAM*



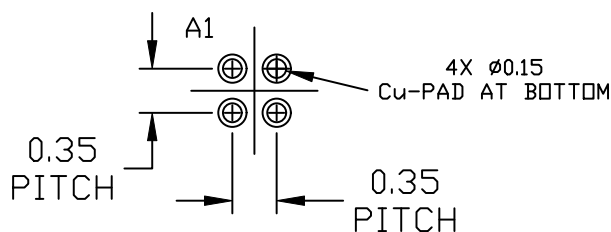
X = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE CONTACT BALLS.
4. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE CONTACT BALLS.
5. DIMENSION b IS MEASURED AT THE MAXIMUM CONTACT BALL DIAMETER PARALLEL TO DATUM C.

| DIM | MILLIMETERS | | |
|-----|-------------|-------|-------|
| | MIN. | NOM. | MAX. |
| A | 0.355 | 0.405 | 0.455 |
| A1 | 0.13 | 0.15 | 0.17 |
| A2 | 0.255 REF | | |
| b | 0.167 | 0.187 | 0.207 |
| D | 0.610 | 0.640 | 0.670 |
| E | 0.610 | 0.640 | 0.670 |
| e | 0.35 BSC | | |



RECOMMENDED MOUNTING FOOTPRINT* (NSMD PAD TYPE)

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

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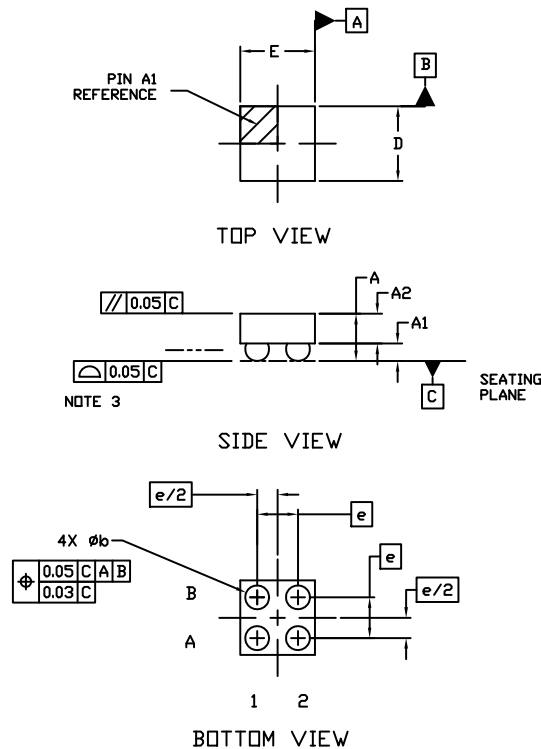
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WLCSP4, 0.64x0.64x0.40

CASE 567XW

ISSUE A

DATE 13 NOV 2019



GENERIC MARKING DIAGRAM*



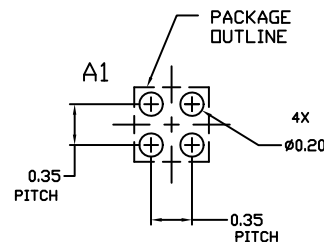
X = Specific Device Code
M = Month

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM C.

| DIM | MILLIMETERS | | |
|-----|-------------|-------|-------|
| | MIN. | NOM. | MAX. |
| A | 0.360 | 0.405 | 0.450 |
| A1 | 0.130 | 0.150 | 0.170 |
| A2 | 0.255 REF | | |
| b | 0.180 | 0.210 | 0.240 |
| D | 0.610 | 0.640 | 0.670 |
| E | 0.610 | 0.640 | 0.670 |
| e | 0.350 BSC | | |



RECOMMENDED MOUNTING FOOTPRINT

- * For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| | | |
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| DESCRIPTION: | WLCSP4, 0.64x0.64x0.40 | PAGE 1 OF 1 |

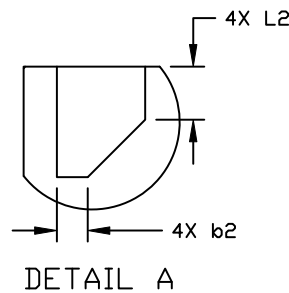
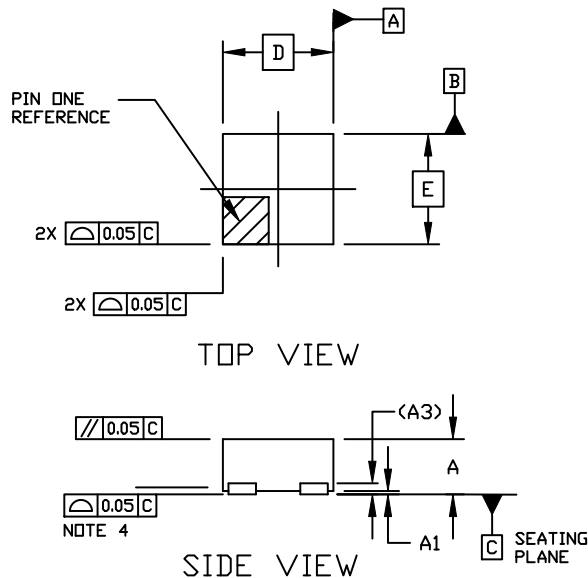
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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



XDFN4 1.0x1.0, 0.65P
CASE 711AJ
ISSUE C

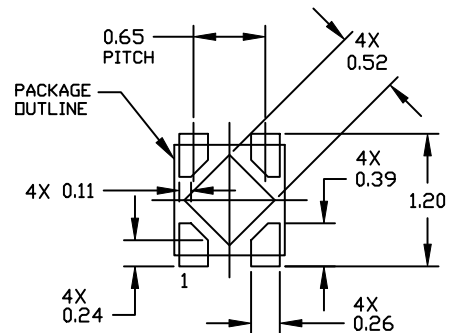
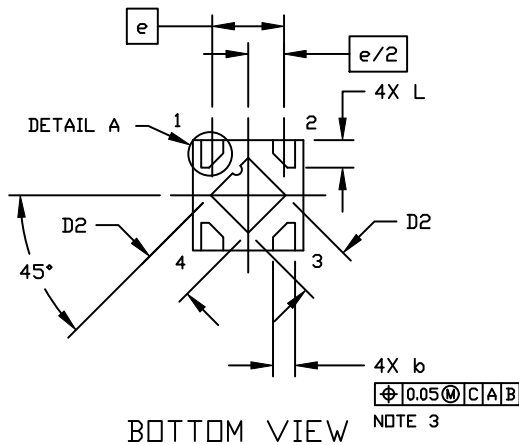
DATE 08 MAR 2022



NOTES:

1. DIMENSIONING AND TOLERANCING PER. ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO THE PLATED TERMINALS AND IS MEASURED BETWEEN 0.15 AND 0.20 FROM THE TERMINAL TIPS.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

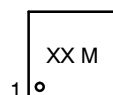
| DIM | MILLIMETERS | | |
|-----|-------------|------|------|
| | MIN | NOM | MAX |
| A | 0.33 | 0.38 | 0.43 |
| A1 | 0.00 | --- | 0.05 |
| A3 | 0.10 REF | | |
| b | 0.15 | 0.20 | 0.25 |
| b2 | 0.02 | 0.07 | 0.12 |
| D | 0.90 | 1.00 | 1.10 |
| D2 | 0.43 | 0.48 | 0.53 |
| E | 0.90 | 1.00 | 1.10 |
| e | 0.65 BSC | | |
| L | 0.20 | | 0.30 |
| L2 | 0.07 | | 0.17 |



RECOMMENDED MOUNTING FOOTPRINT

* FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNT TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

| | | |
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