

Silicon Carbide (SiC) Schottky Diode – EliteSiC, 12 A, 650 V, D1, TO-220-2L

FFSP1265A

Description

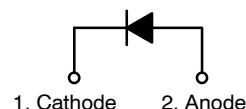
Silicon Carbide (SiC) Schottky Diodes use a completely new technology that provides superior switching performance and higher reliability compared to Silicon. No reverse recovery current, temperature independent switching characteristics, and excellent thermal performance sets Silicon Carbide as the next generation of power semiconductor. System benefits include highest efficiency, faster operating frequency, increased power density, reduced EMI, and reduced system size and cost.

Features

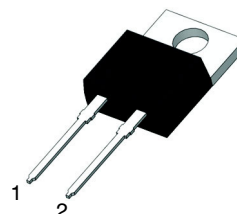
- Max Junction Temperature 175°C
- Avalanche Rated 72 mJ
- High Surge Current Capacity
- Positive Temperature Coefficient
- Ease of Paralleling
- No Reverse Recovery/No Forward Recovery
- This Device is Pb-Free, Halogen Free/BFR Free and RoHS Compliant

Applications

- General Purpose
- SMPS, Solar Inverter, UPS
- Power Switching Circuits

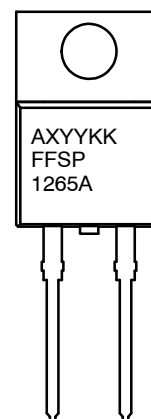


Schottky Diode



TO-220-2LD
CASE 340BB

MARKING DIAGRAM



A	= Assembly Plant Code
XY	= Date Code (Year & Week)
KK	= Lot Traceability Code
FFSP1265A	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FFSP1265A

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
V _{RRM}	Peak Repetitive Reverse Voltage	650	V
E _{AS}	Single Pulse Avalanche Energy (Note 1)	72	mJ
I _F	Continuous Rectified Forward Current @ T _C < 147°C	12	A
	Continuous Rectified Forward Current @ T _C < 135°C	15	A
I _{F,Max}	Non-Repetitive Peak Forward Surge Current	T _C = 25°C, 10 μs	940
		T _C = 150°C, 10 μs	890
I _{F,SM}	Non-Repetitive Forward Surge Current	Half-Sine Pulse, t _p = 8.3 ms	70
I _{F,RM}	Repetitive Forward Surge Current	Half-Sine Pulse, t _p = 8.3 ms	43
P _{TOT}	Power Dissipation	T _C = 25°C	115
		T _C = 150°C	19
T _J , T _{STG}	Operating and Storage Temperature Range	-55 to +175	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. E_{AS} of 72 mJ is based on starting T_J = 25°C, L = 0.5 mH, I_{AS} = 17 A, V = 50 V.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
R _{θJC}	Thermal Resistance, Junction to Case, Max	1.3	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V _F	Forward Voltage	I _F = 12 A, T _C = 25°C	–	1.50	1.75	V
		I _F = 12 A, T _C = 125°C	–	1.6	2.0	
		I _F = 12 A, T _C = 175°C	–	1.72	2.4	
I _R	Reverse Current	V _R = 650 V, T _C = 25°C	–	–	200	μA
		V _R = 650 V, T _C = 125°C	–	–	400	
		V _R = 650 V, T _C = 175°C	–	–	600	
Q _C	Total Capacitive Charge	V = 400 V	–	40	–	nC
C	Total Capacitance	V _R = 1 V, f = 100 kHz	–	665	–	pF
		V _R = 200 V, f = 100 kHz	–	74	–	
		V _R = 400 V, f = 100 kHz	–	54	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

ORDERING INFORMATION

Part Number	Top Marking	Package	Packing Method	Quantity
FFSP1265A	FFSP1265A	TO-220-2LD	Tube	50 Units

TYPICAL CHARACTERISTICS
($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

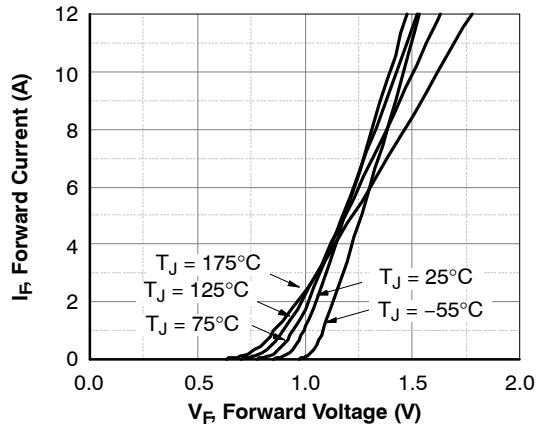


Figure 1. Forward Characteristics

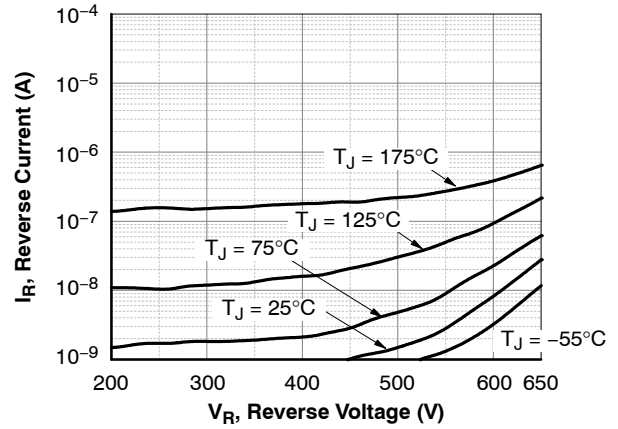


Figure 2. Reverse Characteristics

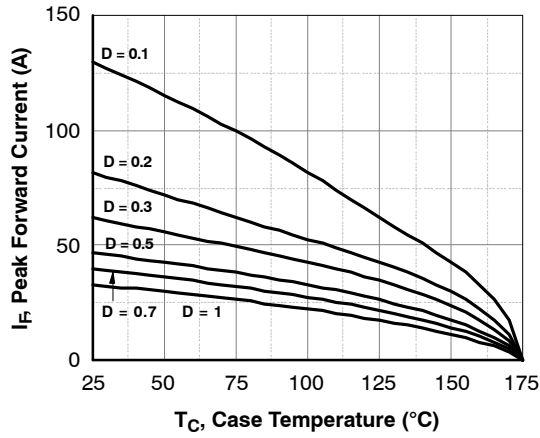


Figure 3. Current Derating

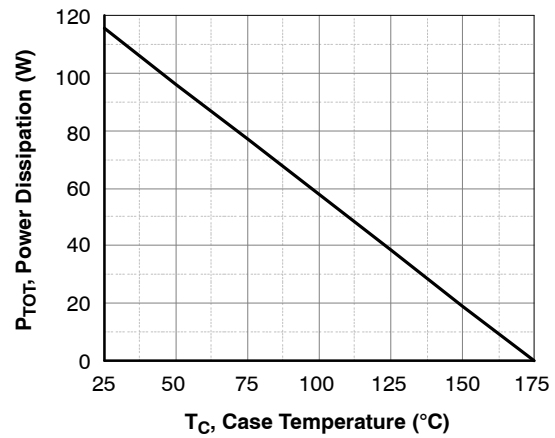


Figure 4. Power Derating

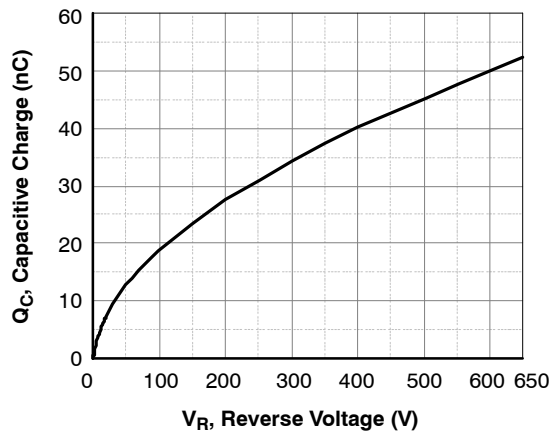


Figure 5. Capacitive Charge vs. Reverse Voltage

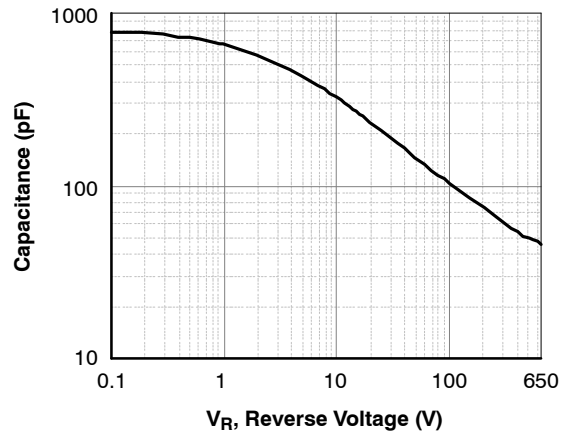


Figure 6. Capacitance vs. Reverse Voltage

TYPICAL CHARACTERISTICS (CONTINUED)

($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

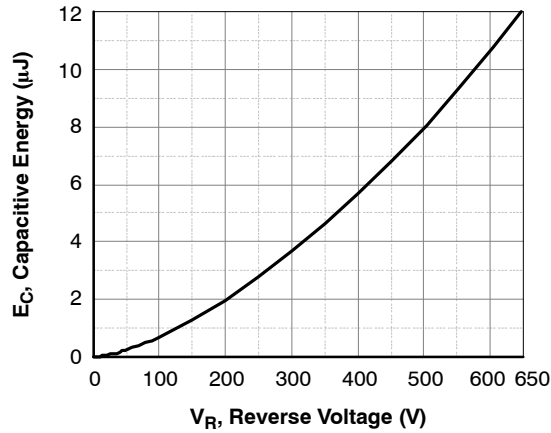


Figure 7. Capacitance Stored Energy

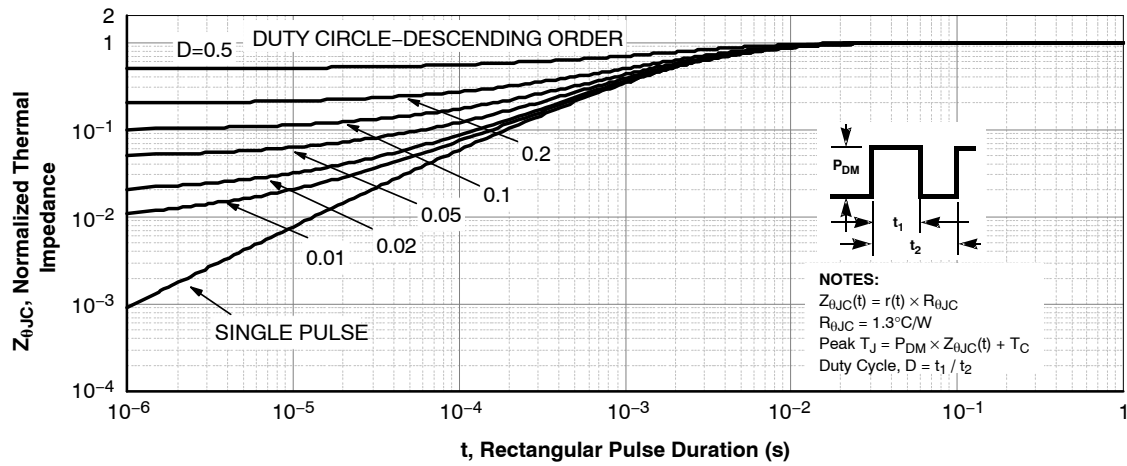


Figure 8. Junction-to-Case Transient Thermal Response Curve

TEST CIRCUIT AND WAVEFORMS

$L = 0.5 \text{ mH}$
 $R < 0.1 \Omega$
 $V_{DD} = 50 \text{ V}$
 $E_{AVL} = 1/2LI^2 [V_{R(AVL)} / (V_{R(AVL)} - V_{DD})]$
 $Q1 = \text{IGBT (BV}_{CES} > \text{DUT } V_{R(AVL)})$

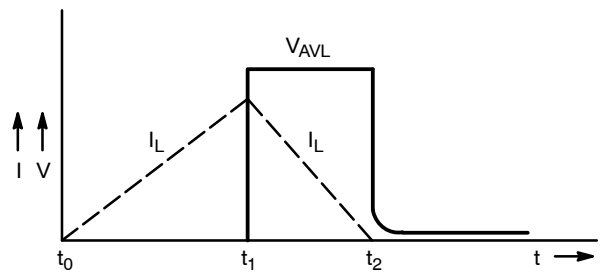
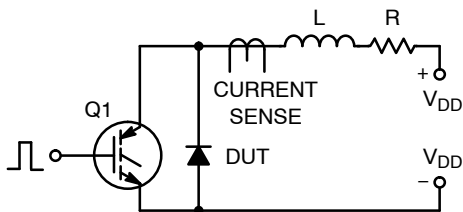


Figure 9. Unclamped Inductive Switching Test Circuit & Waveform

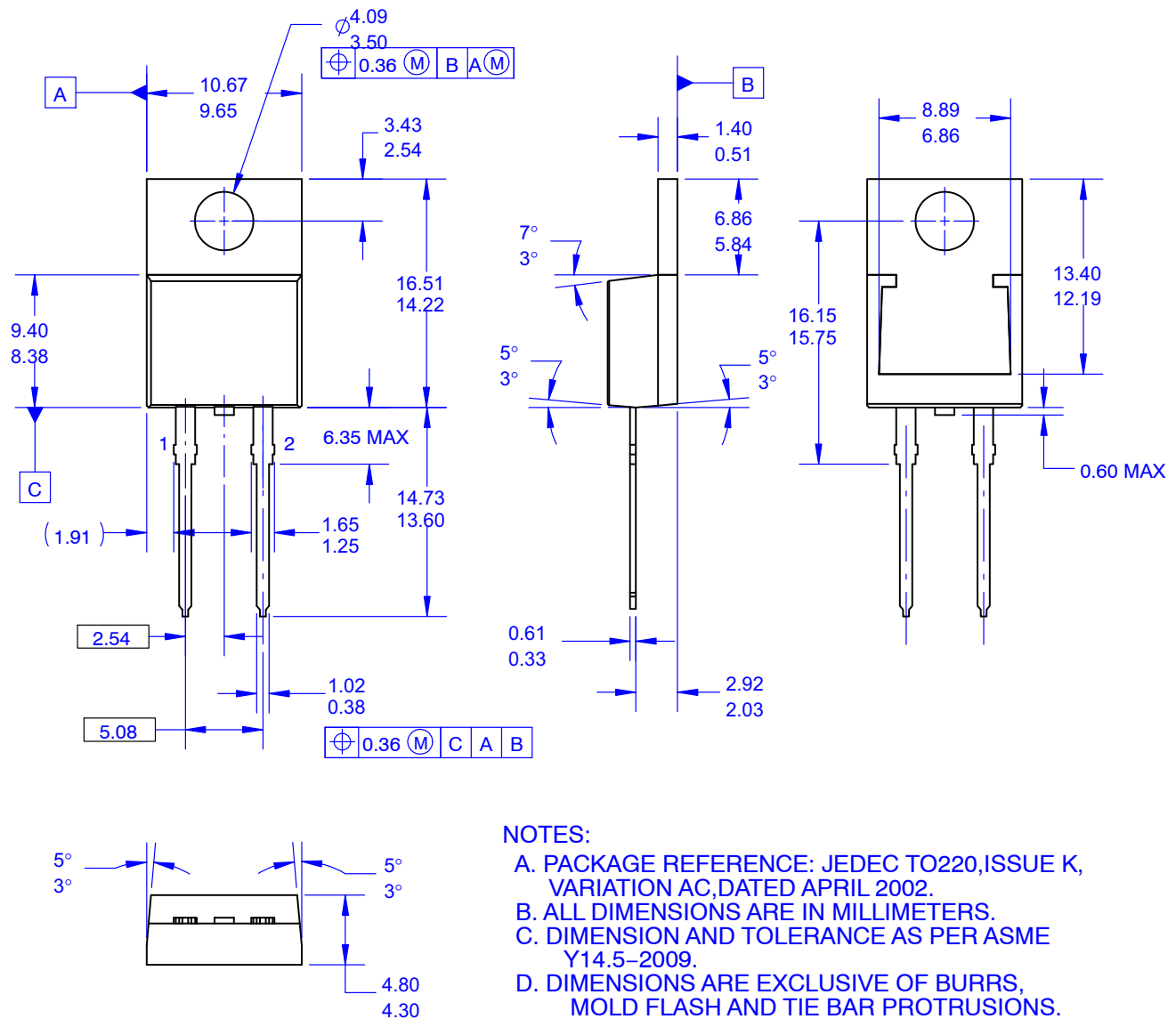
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®

ON

TO-220-2LD
CASE 340BB
ISSUE O

DATE 31 AUG 2016



NOTES:

- PACKAGE REFERENCE: JEDEC TO220,ISSUE K, VARIATION AC,DATED APRIL 2002.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- DIMENSION AND TOLERANCE AS PER ASME Y14.5-2009.
- DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.

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