

N-Channel JFET Low-Frequency Low-Noise Amplifier

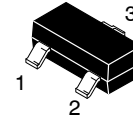
BSR57

- This device is designed for low-power chopper or switching application sourced from process 51

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain–Gate Voltage	V_{DGO}	40	V
Gate–Source Voltage	V_{GSO}	–40	V
Forward Gate Current	I_{GF}	50	mA
Total Power Dissipation Up to $T_{amb} = 40^\circ\text{C}$	P_{tot}	250	mW
Storage Temperature Range	T_{STG}	–55 to +150	$^\circ\text{C}$
Junction Temperature	T_J	150	$^\circ\text{C}$

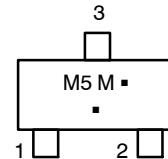
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



1. Drain
2. Source
3. Gate

SOT-23
CASE 318-08
STYLE 10

MARKING DIAGRAM



M5 = Specific Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
BSR57	SOT-23-3/5 (Pb-Free)	3000 / Tape & Reel

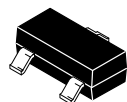
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
BV_{GSS}	Gate–Source Voltage	$V_{DS} = 0\text{ V}$, $I_C = 1.0\text{ }\mu\text{A}$	40	–	–	V
I_{GSS}	Gate Reverse Current	$V_{GS} = 20\text{ V}$, $V_{DS} = 0\text{ V}$	–	–	1.0	nA
I_{DSS}	Zero–Gate Voltage Drain Current	$V_{DS} = 15\text{ V}$, $V_{GS} = 0\text{ V}$	20	–	100	mA
$V_{GS(off)}$	Gate–Source Cut–off Voltage	$V_{DS} = 15\text{ V}$, $I_D = 0.5\text{ nA}$	2.0	–	6.0	V
$V_{DS(on)}$	Drain–Source On Voltage	$V_{GS} = 0\text{ V}$, $I_D = 10\text{ mA}$	–	–	0.5	V
$r_{ds(on)}$	Drain–Source On Reverse	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	–	–	40	Ω
C_{rss}	Reverse Transfer Capacitance	$V_{DS} = 0\text{ V}$, $V_{GS} = 10\text{ V}$	–	–	5.0	pF
t_d	Delay Time	$V_{DD} = 10\text{ V}$, $V_{GS(on)} = 0\text{ V}$ $I_D = 10\text{ mA}$, $V_{GS(off)} = 6.0\text{ V}$	–	–	6.0	ns
t_r	Rise Time		–	–	4.0	
t_{off}	Turn–off Time		–	–	50	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

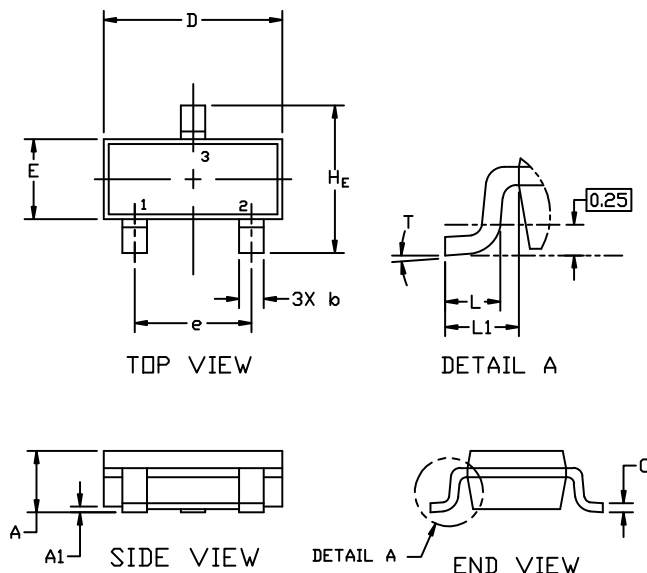
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 4:1

SOT-23 (TO-236)
CASE 318
ISSUE AT

DATE 01 MAR 2023

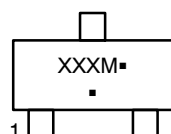


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

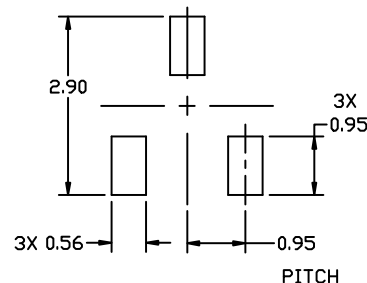
DIM	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
c	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
H _E	2.10	2.40	2.64	0.083	0.094	0.104
T	0°	---	10°	0°	---	10°

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS



SOT-23 (TO-236) CASE 318 ISSUE AT

DATE 01 MAR 2023

STYLE 1 THRU 5: CANCELLED	STYLE 6: PIN 1. BASE 2. EMITTER 3. COLLECTOR	STYLE 7: PIN 1. EMITTER 2. BASE 3. COLLECTOR	STYLE 8: PIN 1. ANODE 2. NO CONNECTION 3. CATHODE		
STYLE 9: PIN 1. ANODE 2. ANODE 3. CATHODE	STYLE 10: PIN 1. DRAIN 2. SOURCE 3. GATE	STYLE 11: PIN 1. ANODE 2. CATHODE 3. CATHODE-ANODE	STYLE 12: PIN 1. CATHODE 2. CATHODE 3. ANODE	STYLE 13: PIN 1. SOURCE 2. DRAIN 3. GATE	STYLE 14: PIN 1. CATHODE 2. GATE 3. ANODE
STYLE 15: PIN 1. GATE 2. CATHODE 3. ANODE	STYLE 16: PIN 1. ANODE 2. CATHODE 3. CATHODE	STYLE 17: PIN 1. NO CONNECTION 2. ANODE 3. CATHODE	STYLE 18: PIN 1. NO CONNECTION 2. CATHODE 3. ANODE	STYLE 19: PIN 1. CATHODE 2. ANODE 3. CATHODE-ANODE	STYLE 20: PIN 1. CATHODE 2. ANODE 3. GATE
STYLE 21: PIN 1. GATE 2. SOURCE 3. DRAIN	STYLE 22: PIN 1. RETURN 2. OUTPUT 3. INPUT	STYLE 23: PIN 1. ANODE 2. ANODE 3. CATHODE	STYLE 24: PIN 1. GATE 2. DRAIN 3. SOURCE	STYLE 25: PIN 1. ANODE 2. CATHODE 3. GATE	STYLE 26: PIN 1. CATHODE 2. ANODE 3. NO CONNECTION
STYLE 27: PIN 1. CATHODE 2. CATHODE 3. CATHODE	STYLE 28: PIN 1. ANODE 2. ANODE 3. ANODE				

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