MC74HC597A

8-Bit Serial or Parallel-Input/Serial-Output Shift Register with Input Latch

High−Performance Silicon−Gate CMOS

The MC74HC597A is identical in pinout to the LS597. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of an 8−bit input latch which feeds parallel data to an 8−bit shift register. Data can also be loaded serially.

The HC597A is similar in function to the HC589A, which is a 3−state device.

Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 516 FETs or 129 Equivalent Gates
- These are Pb−Free Devices*

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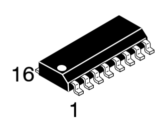
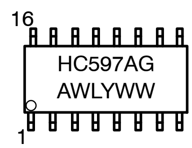
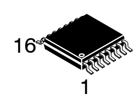
MARKING DIAGRAMS



SOIC−16
D SUFFIX
CASE 751B





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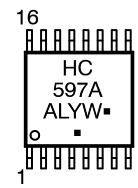
DT SUFFIX
CASE 948F



A	=	Assembly Location
WL, L	=	Wafer Lot
YY, Y	=	Year
WW, W	=	Work Week
G or ▪	=	Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

July, 2013 − Rev. 3

Publication Order Number:
MC74HC597A/D

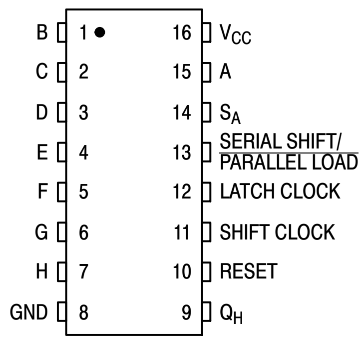


Figure 1. Pin Assignment

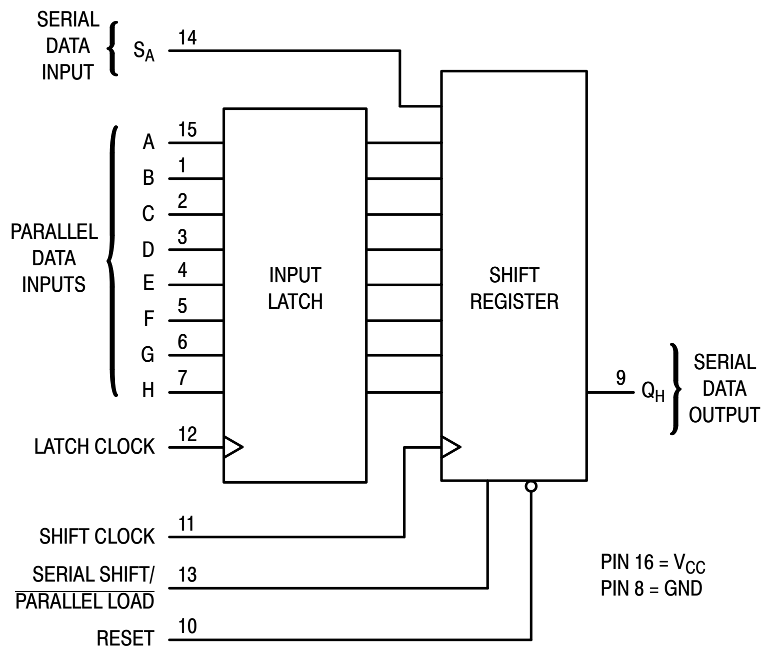


Figure 2. Logic Diagram

ORDERING INFORMATION

Device	Package	Shipping†
MC74HC597ADG	SOIC−16 (Pb−Free)	48 Units / Rail
MC74HC597ADR2G	SOIC−16 (Pb−Free)	2500 Units / Reel
MC74HC597ADTR2G	TSSOP−16 (Pb−Free)	2500 Units / Reel
MC74HC597ADTG	TSSOP−16 (Pb−Free)	96 Units / Tube

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC or TSSOP Package) (Ceramic DIP)	 260 300	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
Ceramic DIP: – 10 mW/°C from 100° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} = 2.0 V V_{CC} = 3.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0 0	1000 600 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit – 55 to 25°C	≤ 85°C	≤ 125°C	Unit
V_{IH}	Minimum High−Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\lvert I_{out} \rvert \le$ 20 µA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low−Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\lvert I_{out} \rvert \le$ 20 µA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V_{OH}	Minimum High−Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\lvert I_{out} \rvert \le$ 20 µA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4 4 5.9	1.9 4 4 5.9	V
		V_{in} = V_{IH} or V_{IL} $\lvert I_{out} \rvert \le$ 2.4 mA $\lvert I_{out} \rvert \le$ 4.0 mA $\lvert I_{out} \rvert \le$ 5.2 mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.20 3.70 5.20	
V_{OL}	Maximum Low−Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\lvert I_{out} \rvert \le$ 20 µA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\lvert I_{out} \rvert \le$ 2.4 mA $\lvert I_{out} \rvert \le$ 4.0 mA $\lvert I_{out} \rvert \le$ 5.2 mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	6.0	± 0.1	± 1.0	± 1.0	µA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND I_{out} = 0 µA	6.0	4	40	160	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle), Shift Clock (Figures 4 and 10)	2.0 3.0 4.5 6.0	10 15 30 50	9 14 28 45	8 12 25 40	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Latch Clock to Q_H (Figures 3 and 10)	2.0 3.0 4.5 6.0	175 100 40 30	225 110 50 40	275 125 60 50	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Shift Clock to Q_H (Figures 4 and 10)	2.0 3.0 4.5 6.0	160 90 30 25	200 130 40 30	240 160 48 40	ns
t_{PHL}	Maximum Propagation Delay, Reset to Q_H (Figures 5 and 10)	2.0 3.0 4.5 6.0	160 90 30 25	200 130 40 30	240 160 48 40	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Serial Shift/$\overline{\text{Parallel Load}}$ to Q_H (Figures 6 and 10)	2.0 3.0 4.5 6.0	160 90 30 25	200 130 40 30	240 160 48 40	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 3 and 10)	2.0 3.0 4.5 6.0	75 27 15 13	95 32 19 16	110 36 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Package)*	40	pF

* Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

PIN DESCRIPTIONS

DATA INPUTS

A, B, C, D, E, F, G, H (Pins 15, 1, 2, 3, 4, 5, 6, 7)

Parallel data inputs. Data on these inputs is stored in the input latch on the rising edge of the Latch Clock input.

S_A (Pin 14)

Serial data input. Data on this input is shifted into the shift register on the rising edge of the Shift Clock input it Serial Shift/$\overline{\text{Parallel Load}}$ is high. Data on this input is ignored when Serial Shift/$\overline{\text{Parallel Load}}$ is low.

CONTROL INPUTS

Serial Shift/$\overline{\text{Parallel Load}}$ (Pin 13)

Shift register mode control. When a high level is applied to this pin, the shift register is allowed to serially shift data. When a low level is applied to this pin, the shift register accepts parallel data from the input latch, and serial shifting is inhibited.

Reset (Pin 10)

Asynchronous, Active-low shift register reset. A low level applied to this input resets the shift register to a low level, but does not change the data in the input latch.

Shift Clock (Pin 11)

Serial shift register clock. A low-to-high transition on this input shifts data on the Serial Data Input into the shift register and data in stage H is shifted out Q_H, being replaced by the data previously stored in stage G.

Latch Clock (Pin 12)

Latch clock. A low-to-high transition on this input loads the parallel data on inputs A-H into the input latch.

OUTPUT

Q_H (Pin 9)

Serial data output. This pin is the output from the last stage of the shift register.

TIMING REQUIREMENTS (Input t_r = t_f = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit – 55 to 25°C	Guaranteed Limit ≤ 85°C	Guaranteed Limit ≤ 125°C	Unit
t_{su}	Minimum Setup Time, Parallel Data inputs A−H to Latch Clock (Figure 7)	2.0 3.0 4.5 6.0	70 40 15 13	80 45 19 16	90 50 24 20	ns
t_{su}	Minimum Setup Time, Serial Data Input S_A to Shift Clock (Figure 8)	2.0 3.0 4.5 6.0	70 40 15 13	80 45 19 16	90 50 24 20	ns
t_{su}	Minimum Setup Time, Serial Shift/$\overline{\text{Parallel Load}}$ to Shift Clock (Figure 9)	2.0 3.0 4.5 6.0	70 40 15 13	80 45 19 16	90 50 24 20	ns
t_h	Minimum Hold Time, Latch Clock to Parallel Data Inputs A−H (Figure 7)	2.0 3.0 4.5 6.0	15 10 2 2	20 15 3 3	30 25 5 4	ns
t_h	Minimum Hold Time, Shift Clock to Serial Data Input S_A (Figure 8)	2.0 3.0 4.5 6.0	2 2 2 2	2 2 2 2	2 2 2 2	ns
t_{rec}	Minimum Recovery Time, Reset Inactive to Shift Clock (Figure 5)	2.0 3.0 4.5 6.0	70 40 15 13	80 45 19 16	90 50 24 20	ns
t_w	Minimum Pulse Width, Latch Clock and Shift Clock (Figures 3 and 4)	2.0 3.0 4.5 6.0	60 35 12 10	70 40 15 13	80 45 19 16	ns
t_w	Minimum Pulse Width, Reset (Figure 5)	2.0 3.0 4.5 6.0	60 35 12 10	70 40 15 13	80 45 19 16	ns
t_w	Minimum Pulse Width, Serial Shift/$\overline{\text{Parallel Load}}$ (Figure 6)	2.0 3.0 4.5 6.0	60 35 12 10	70 40 15 13	80 45 19 16	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 3)	2.0 3.0 4.5 6.0	1000 800 500 400	1000 800 500 400	1000 800 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High−Speed CMOS Data Book (DL129/D).

FUNCTION TABLE

Operation	Inputs						Resulting Function		
	Reset	Serial Shift/ $\overline{\text{Parallel Load}}$	Latch Clock	Shift Clock	Serial Input S_A	Parallel Inputs A–H	Latch Contents	Shift Register Contents	Output Q_H
Reset shift register	L	X	L, H, ↓	X	X	X	U	L	L
Reset shift register; load parallel data into data latch	L	X	↑	X	X	a–h	a–h	L	L
Load parallel data into data latch	H	H	↑	L,H, ↓	X	a–h	a–h	U	U
Transfer latch contents to shift register	H	L	L, H, ↓	X	X	X	U	$LR_N \rightarrow SR_N$	LR_H
Contents of data latch and shift register are unchanged	H	H	L, H, ↓	L,H, ↓	X	X	U	U	U
Load parallel data into data latch and shift register	H	L	↑	X	X	a–h	a–h	a–h	h
Shift serial data into shift register	H	H	X	↑	D	X	*	SR_A = D; $SR_N \rightarrow SR_{N+1}$	$SR_G \rightarrow SR_H$
Load parallel data into data latch and shift serial data into shift register	H	H	↑	↑	D	a–h	a–h	SR_A = D; $SR_N \rightarrow SR_{N+1}$	$SR_G \rightarrow SR_H$

LR = latch register contents
SR = shift register contents
* = depends on latch clock input

a–h = data at parallel data inputs A–H
D = data (L, H) at serial data input S_A

U = remains unchanged
X = don't care

SWITCHING WAVEFORMS

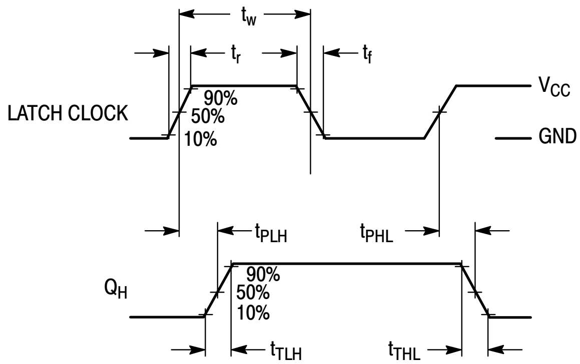


Figure 3. (Serial Shift/Parallel Load = L)

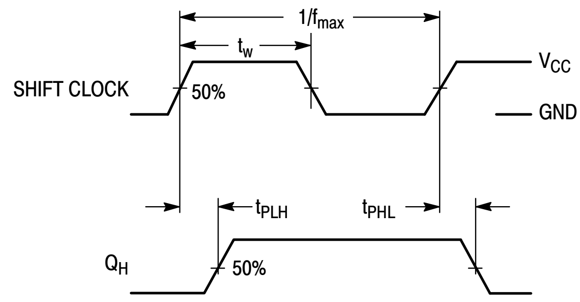
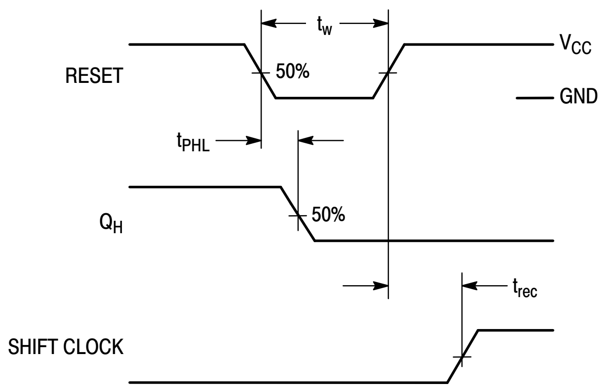


Figure 4. (Serial Shift/Parallel Load = H)



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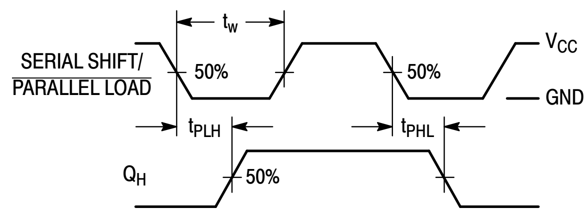

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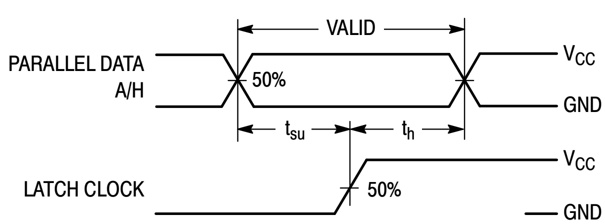

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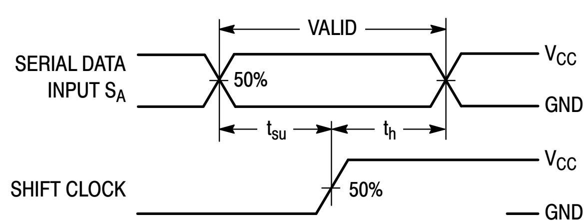

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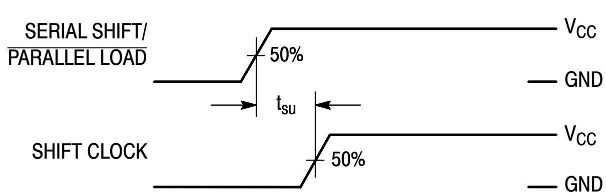
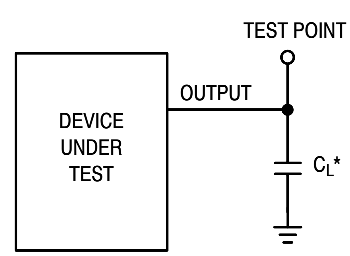


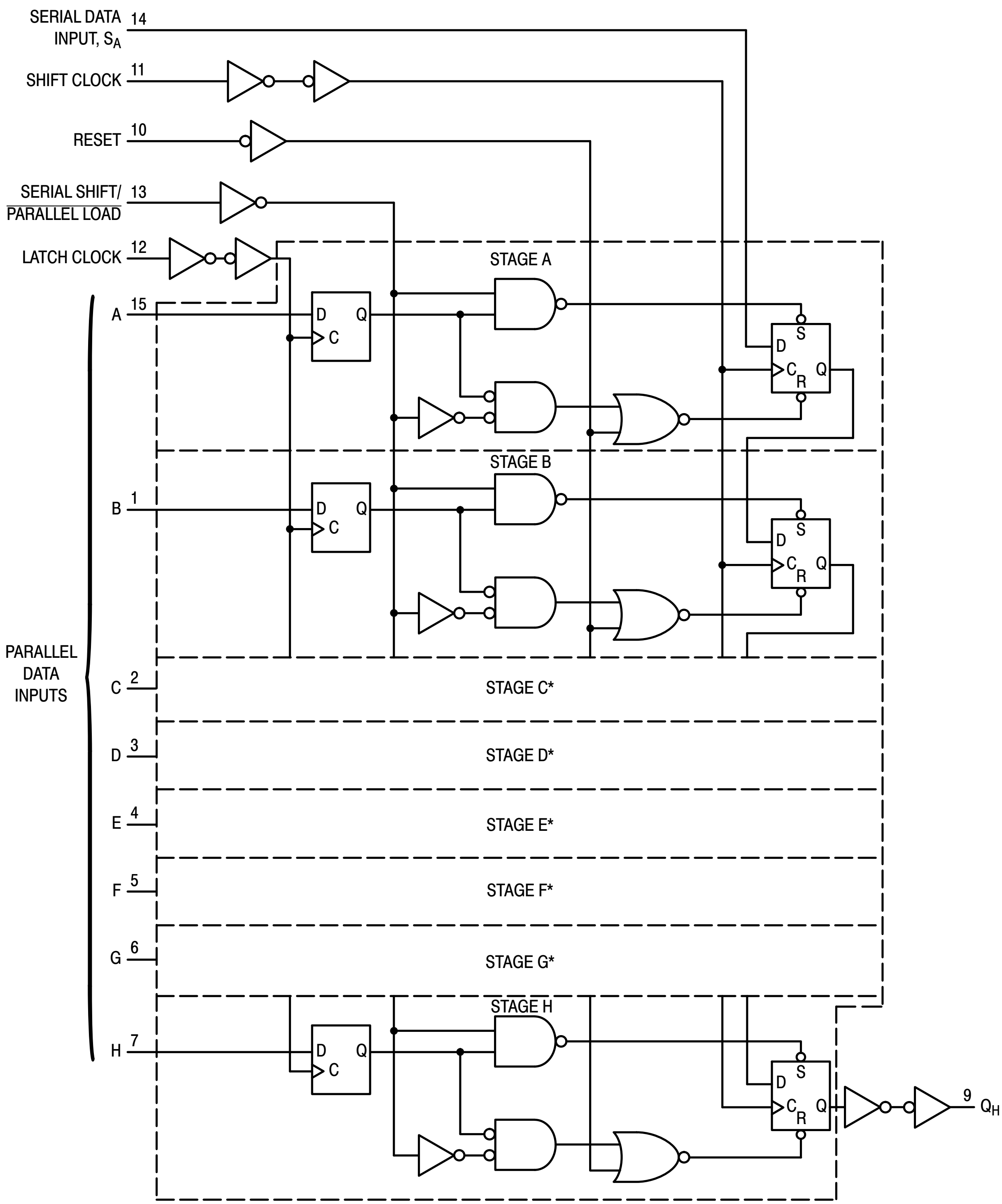
Figure 9.



*Includes all probe and jig capacitance

Figure 10. Test Circuit

EXPANDED LOGIC DIAGRAM



*NOTE: Stages C thru G (not shown in detail) are identical to stages A and B above.

Figure 11. Extended Logic Diagram

TIMING DIAGRAM

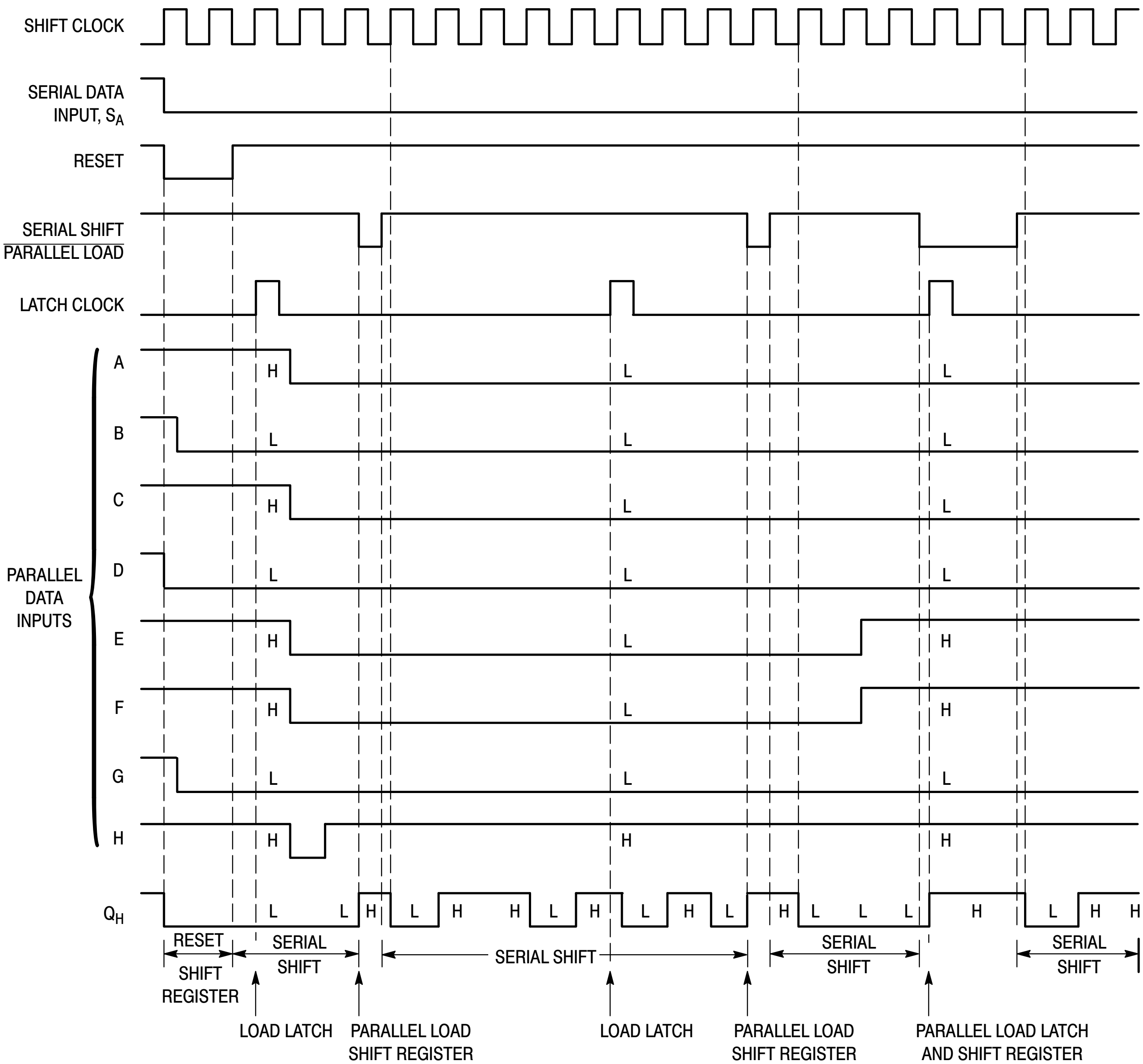
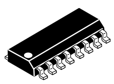


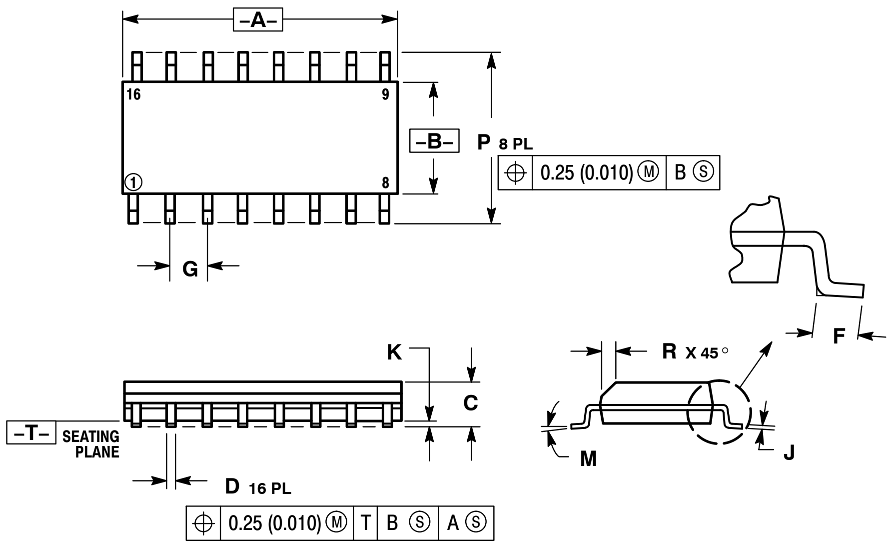
Figure 12. Timing Diagram



SCALE 1:1

SOIC−16
CASE 751B−05
ISSUE K

DATE 29 DEC 2006



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO CONNECTION
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR
15. EMITTER
16. COLLECTOR

STYLE 2:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION
4. CATHODE
5. CATHODE
6. NO CONNECTION
7. ANODE
8. CATHODE
9. CATHODE
10. ANODE
11. NO CONNECTION
12. CATHODE
13. CATHODE
14. NO CONNECTION
15. ANODE
16. CATHODE

STYLE 3:
PIN 1. COLLECTOR, DYE #1
2. BASE, #1
3. EMITTER, #1
4. COLLECTOR, #1
5. COLLECTOR, #2
6. BASE, #2
7. EMITTER, #2
8. COLLECTOR, #2
9. COLLECTOR, #3
10. BASE, #3
11. EMITTER, #3
12. COLLECTOR, #3
13. COLLECTOR, #4
14. BASE, #4
15. EMITTER, #4
16. COLLECTOR, #4

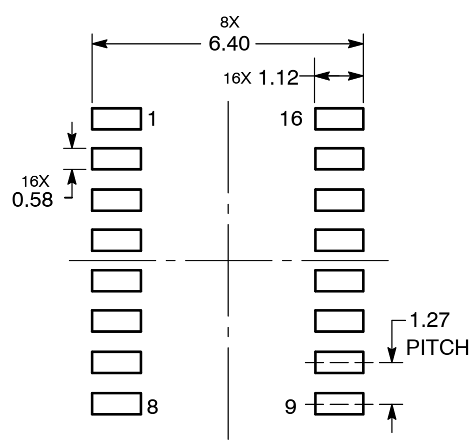
STYLE 4:
PIN 1. COLLECTOR, DYE #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. COLLECTOR, #3
6. COLLECTOR, #3
7. COLLECTOR, #4
8. COLLECTOR, #4
9. BASE, #4
10. EMITTER, #4
11. BASE, #3
12. EMITTER, #3
13. BASE, #2
14. EMITTER, #2
15. BASE, #1
16. EMITTER, #1

STYLE 5:
PIN 1. DRAIN, DYE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. DRAIN, #3
6. DRAIN, #3
7. DRAIN, #4
8. DRAIN, #4
9. GATE, #4
10. SOURCE, #4
11. GATE, #3
12. SOURCE, #3
13. GATE, #2
14. SOURCE, #2
15. GATE, #1
16. SOURCE, #1

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 7:
PIN 1. SOURCE N-CH
2. COMMON DRAIN (OUTPUT)
3. COMMON DRAIN (OUTPUT)
4. GATE P-CH
5. COMMON DRAIN (OUTPUT)
6. COMMON DRAIN (OUTPUT)
7. COMMON DRAIN (OUTPUT)
8. SOURCE P-CH
9. SOURCE P-CH
10. COMMON DRAIN (OUTPUT)
11. COMMON DRAIN (OUTPUT)
12. COMMON DRAIN (OUTPUT)
13. GATE N-CH
14. COMMON DRAIN (OUTPUT)
15. COMMON DRAIN (OUTPUT)
16. SOURCE N-CH

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

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DESCRIPTION:	SOIC−16	PAGE 1 OF 1

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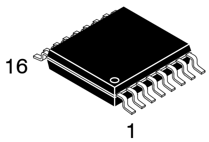

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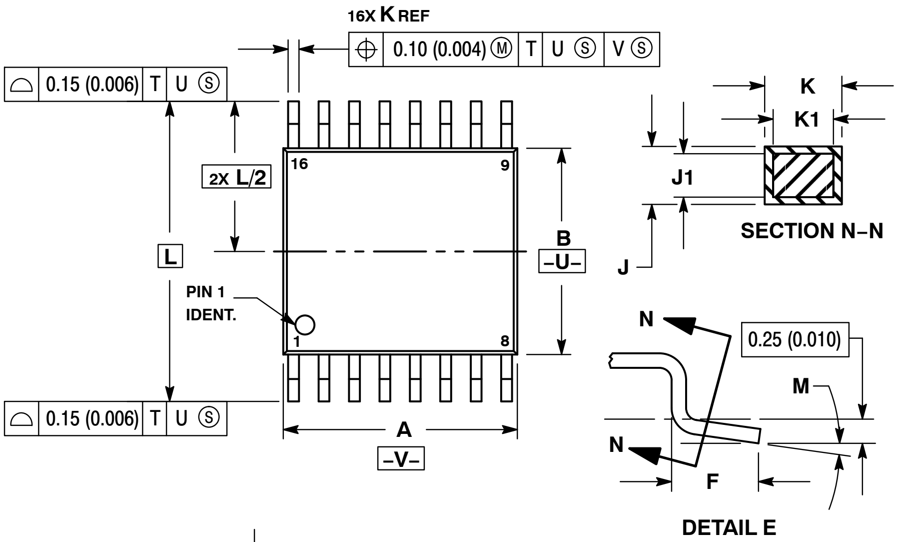
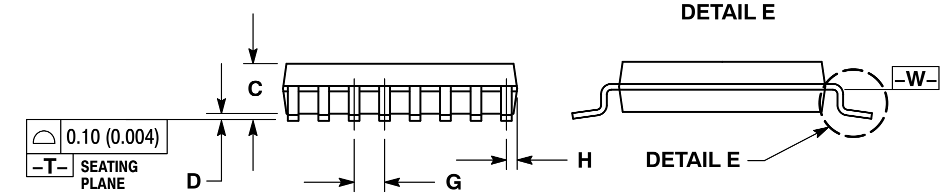
TSSOP−16
CASE 948F−01
ISSUE B

DATE 19 OCT 2006

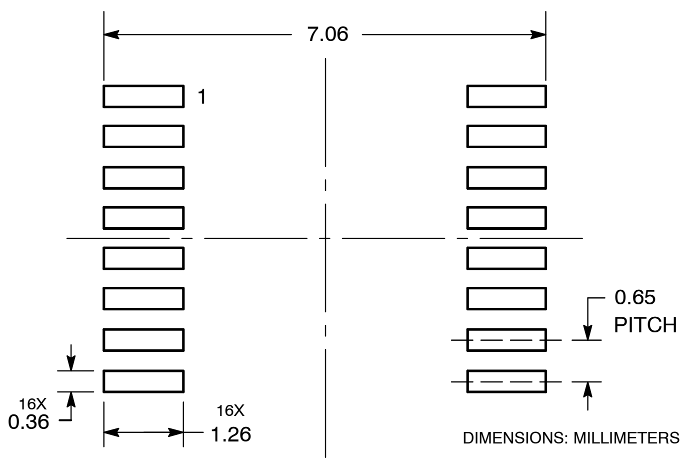




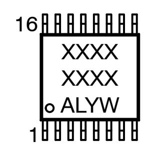
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT



GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
G or ▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

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