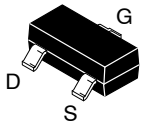
# P-Channel Switch

# MMBFJ270




**SOT−23 (TO−236)**
**CASE 318−08**

### Description

This device is designed for low level analog switching sample and hold circuits and chopper stabilized amplifiers.
Sourced from process 88.

### Features

- These are Pb−Free Devices

### ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25°C unless otherwise noted) (Note 1)

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DG}$ | Drain−Gate Voltage | −30 | V |
| $V_{GS}$ | Gate−Source Voltage | 30 | V |
| $I_{GF}$ | Forward Gate Current | 50 | mA |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | −55 to 150 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

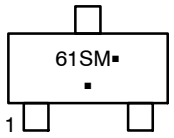
1. These ratings are limiting values above which the serviceability of any semiconductor device may be impaired. These are steady−state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

### THERMAL CHARACTERISTICS ($T_A$ = 25°C unless otherwise noted)

| Symbol | Parameter | Max | Unit |
|---|---|---|---|
| $P_D$ | Total Device Dissipation | 225 | mW |
| | Derate Above 25°C | 1.8 | mW/°C |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (Note 2) | 556 | °C/W |

2. Device mounted on FR−4 PCB, 1 inch x 0.85 inch x 0.062 inch.

### MARKING DIAGRAMS




61S = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Microdot may be in either location)

### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| MMBFJ270 | SOT−23 (TO−236) (Pb−Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted)

| Symbol | Parameter | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** (Note 3) | | | | | |
| $V_{(BR)GSS}$ | Gate−Source Breakdown Voltage | $I_G$ = 1.0 μA, $V_{DS}$ = 0 | 30 | | V |
| $I_{GSS}$ | Gate Reverse Current | $V_{GS}$ = 20 V, $V_{DS}$ = 0 | | 200 | pA |
| $V_{GS(off)}$ | Gate−Source Cut−Off Voltage | $V_{DS}$ = −15 V, $I_D$ = −1.0 nA | 0.5 | 2.0 | V |
| **ON CHARACTERISTICS** (Note 3) | | | | | |
| $I_{DSS}$ | Zero−Gate Voltage Drain Current | $V_{DS}$ = −15 V, $V_{GS}$ = 0 | −2.0 | −15 | mA |
| gfs | Forward Transconductance | $V_{GS}$ = 0 V, $V_{DS}$ = 15 V, f = 1.0 kHz | 6000 | 15000 | μmhos |
| goss | Common−Source Output Conductance | $V_{GS}$ = 0 V, $V_{DS}$ = 15 V, f = 1.0 kHz | | 200 | μmhos |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Short duration test pulse used to minimize self−heating effect.

## TYPICAL CHARACTERISTICS

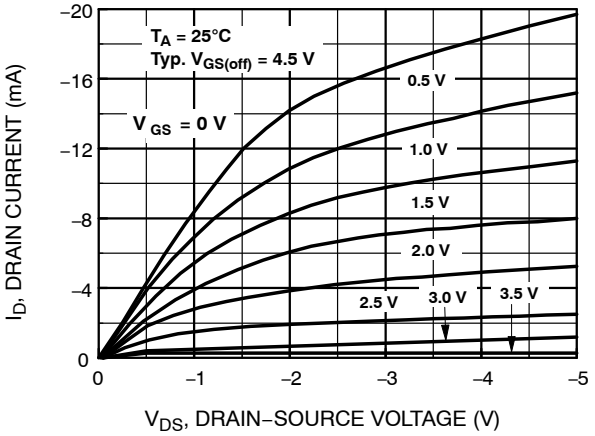



**Figure 1. Common Drain−Source**

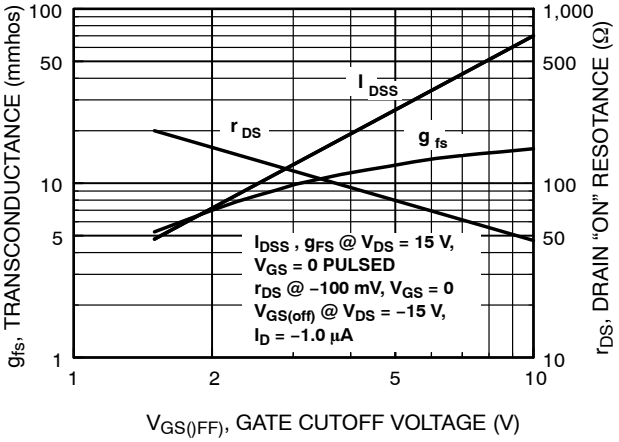



**Figure 2. Parameter Interactions**

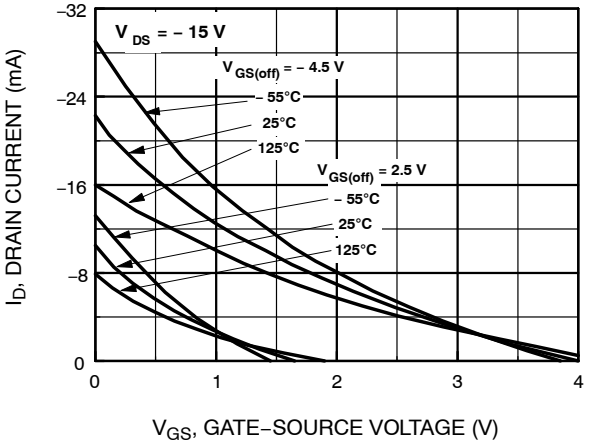



**Figure 3. Transfer Characteristics**

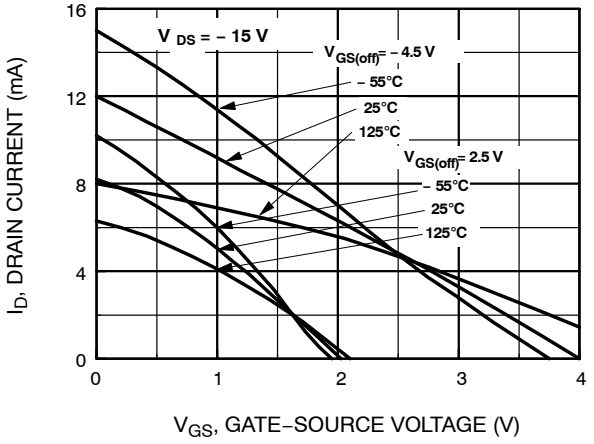



**Figure 4. Transfer Characteristics**

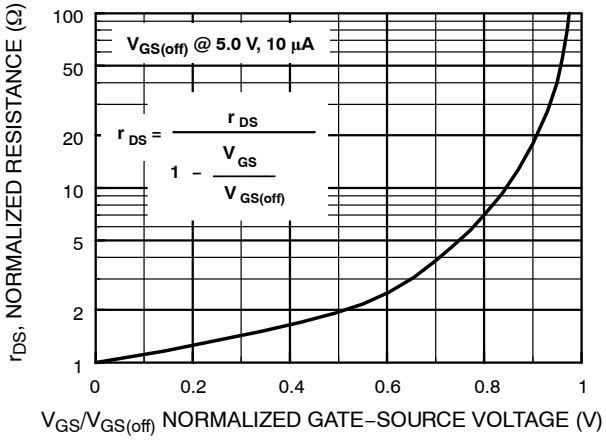



**Figure 5. Normalized Drain Resistance vs. Bias Voltage**

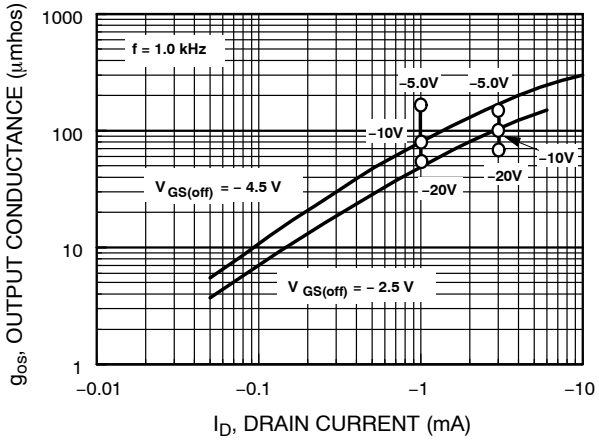



**Figure 6. Output Conductance vs. Drain Current**

## TYPICAL CHARACTERISTICS (Continued)

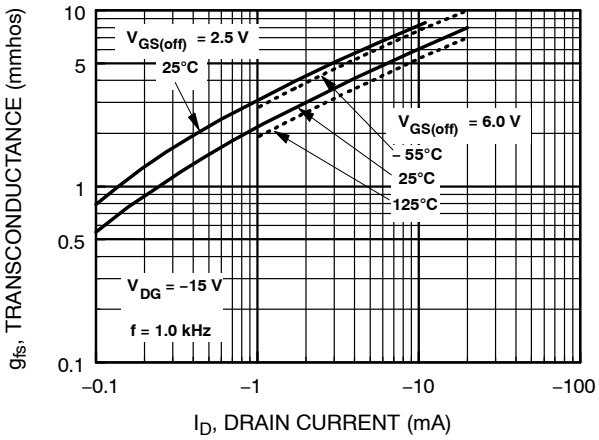



**Figure 7. Transconductance vs. Drain Current**

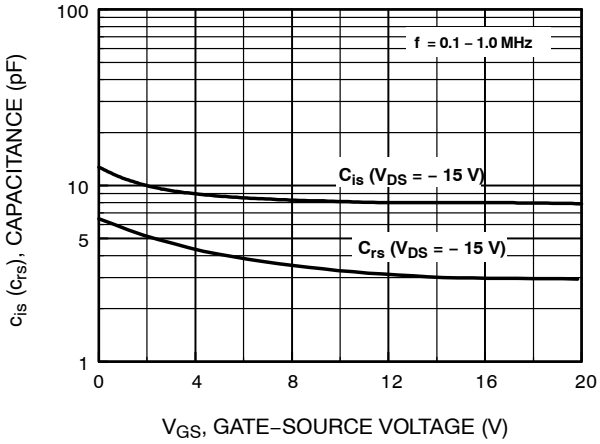



**Figure 8. Capacitance vs. Voltage**

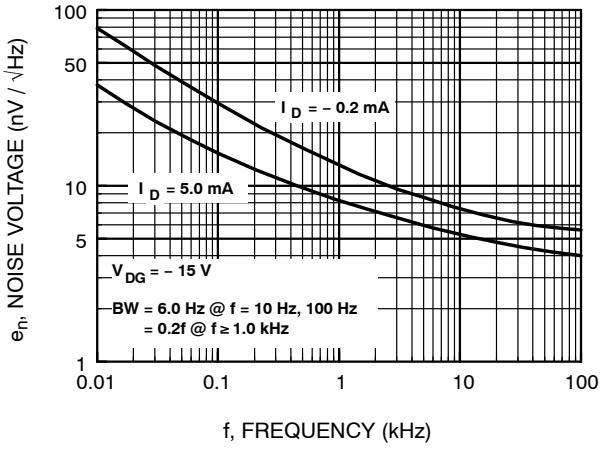



**Figure 9. Noise Voltage vs. Frequency**

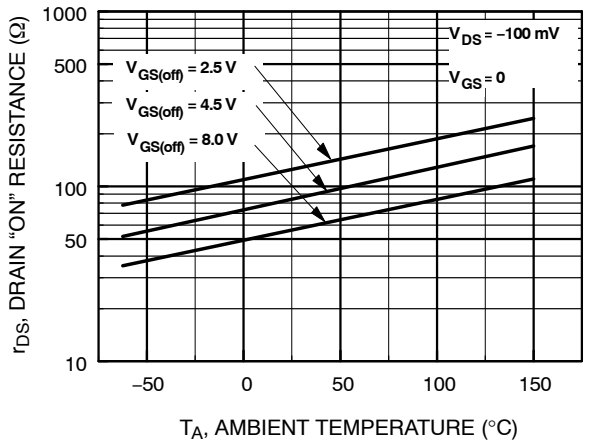



**Figure 10. Channel Resistance vs. Temperature**

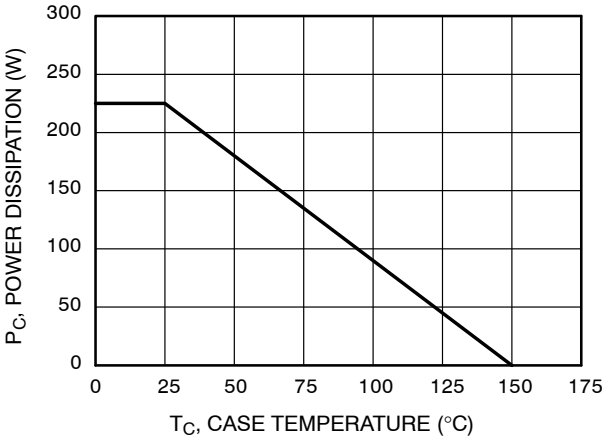
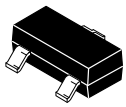



**Figure 11. Power Derating**

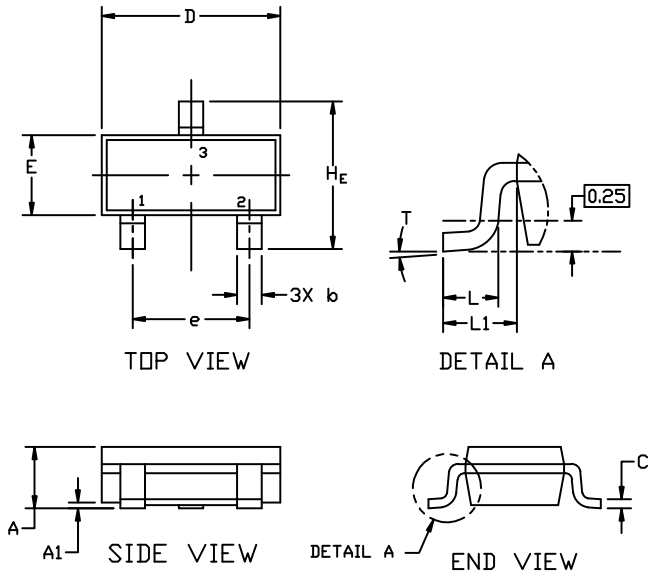
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS



SCALE 4:1

**SOT−23 (TO−236)**
CASE 318
ISSUE AT

DATE 01 MAR 2023

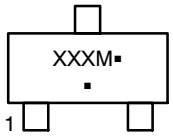



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

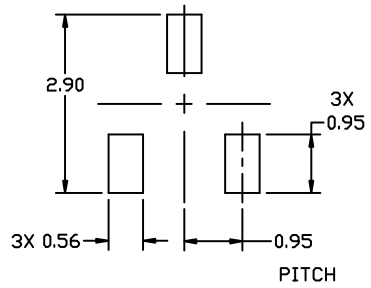
| | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| DIM | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.89 | 1.00 | 1.11 | 0.035 | 0.039 | 0.044 |
| A1 | 0.01 | 0.06 | 0.10 | 0.000 | 0.002 | 0.004 |
| b | 0.37 | 0.44 | 0.50 | 0.015 | 0.017 | 0.020 |
| c | 0.08 | 0.14 | 0.20 | 0.003 | 0.006 | 0.008 |
| D | 2.80 | 2.90 | 3.04 | 0.110 | 0.114 | 0.120 |
| E | 1.20 | 1.30 | 1.40 | 0.047 | 0.051 | 0.055 |
| e | 1.78 | 1.90 | 2.04 | 0.070 | 0.075 | 0.080 |
| L | 0.30 | 0.43 | 0.55 | 0.012 | 0.017 | 0.022 |
| L1 | 0.35 | 0.54 | 0.69 | 0.014 | 0.021 | 0.027 |
| $H_E$ | 2.10 | 2.40 | 2.64 | 0.083 | 0.094 | 0.104 |
| T | 0° | --- | 10° | 0° | --- | 10° |

### GENERIC MARKING DIAGRAM*




XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.




RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**STYLES ON PAGE 2**

| | | | |
|---|---|---|---|
| **DOCUMENT NUMBER:** | **98ASB42226B** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red. | |
| **DESCRIPTION:** | **SOT−23 (TO−236)** | | **PAGE 1 OF 2** |

**SOT−23 (TO−236)**
CASE 318
ISSUE AT

DATE 01 MAR 2023

STYLE 1 THRU 5:
CANCELLED

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 7:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

STYLE 12:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 13:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 15:
PIN 1. GATE
2. CATHODE
3. ANODE

STYLE 16:
PIN 1. ANODE
2. CATHODE
3. CATHODE

STYLE 17:
PIN 1. NO CONNECTION
2. ANODE
3. CATHODE

STYLE 18:
PIN 1. NO CONNECTION
2. CATHODE
3. ANODE

STYLE 19:
PIN 1. CATHODE
2. ANODE
3. CATHODE−ANODE

STYLE 20:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 22:
PIN 1. RETURN
2. OUTPUT
3. INPUT

STYLE 23:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 24:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 25:
PIN 1. ANODE
2. CATHODE
3. GATE

STYLE 26:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION

STYLE 27:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

STYLE 28:
PIN 1. ANODE
2. ANODE
3. ANODE

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