

# Self-Test Appliance Leakage Circuit Interrupter (ALCI) NCS37020

The NCS37020 is an UL943B compliant signal processor for ALCI applications with self-test. The device integrates a 12 V shunt power supply, tiered differential fault detection and self-test per the UL943B standard. Self-test is monitored at start up and every 12 minutes.

## Features

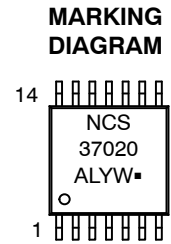
- Meets UL943B Self-test ALCI Requirements
- 12 V Shunt Regulator
- Precision Bandgap
- 3.3 V LDO Linear Regulator
- CT Sense Amplifier  $V_{OS}$  Dynamic Cancellation
- Oscillator Frequency Trimmed to AC Input
- Tiered GF Trip Times
- Built-In Noise Filter
- LED EOL Indicator
- SCR Gate Driver
- Adjustable Sensitivity
- Minimum External Components
- Low Quiescent Current
- 14 Pin TSSOP Package

## Typical Applications

- Personal Care Products
- Non Grounded Neutral Electrical Outlets, Circuit Breakers and Power Cords Requiring Ground Fault Safety Features
- ALCI and RCCB Circuits

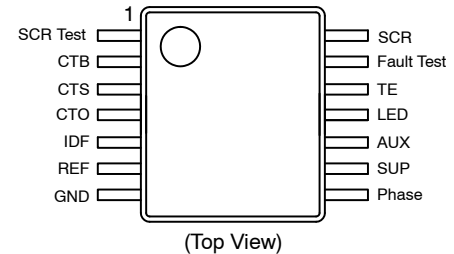


TSSOP-14  
CASE 948G



A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

## PIN CONNECTIONS



## ORDERING INFORMATION

| Device         | Package               | Shipping <sup>†</sup> |
|----------------|-----------------------|-----------------------|
| NCS37020DTBR2G | TSSOP-14<br>(Pb-Free) | 2500 / Tape &<br>Reel |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NCS37020

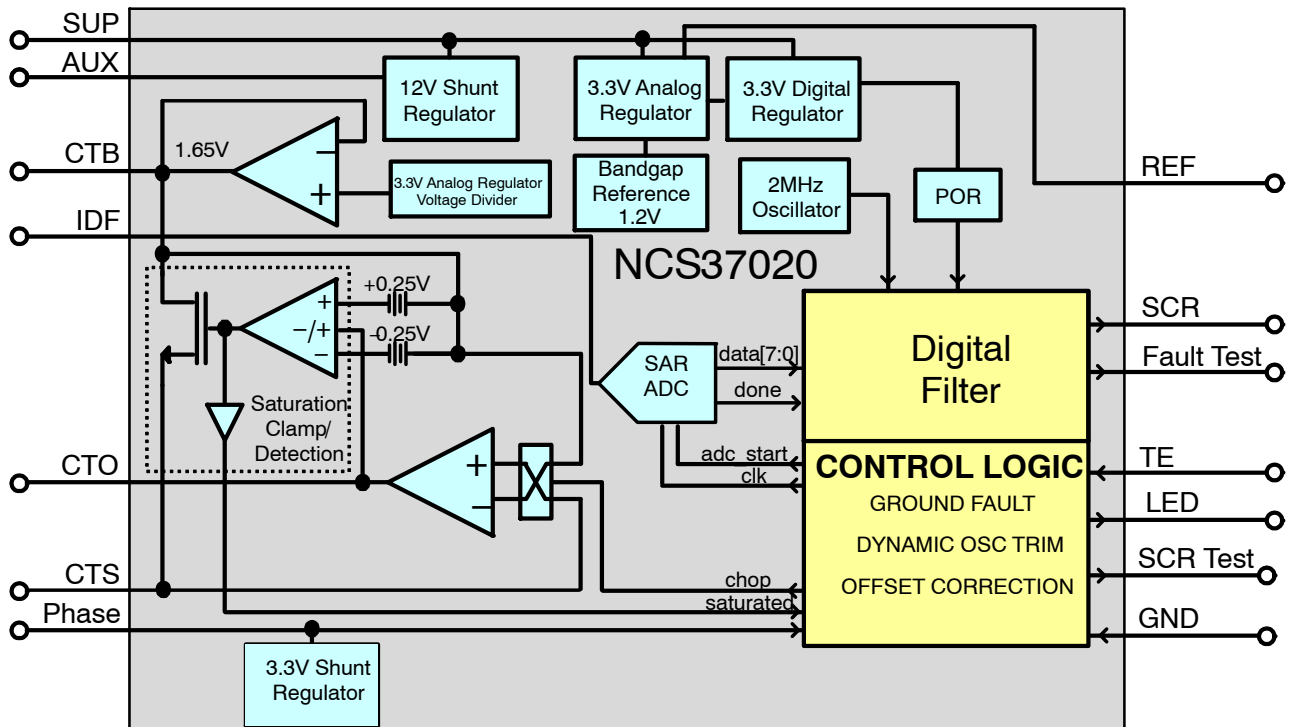


Figure 1. Simplified Block Diagram

Table 1. TSSOP PIN DESCRIPTION

| Pin # | Name       | Pad Description                                |
|-------|------------|------------------------------------------------|
| 1     | SCR Test   | SCR test input for SCR functionality           |
| 2     | CTB        | Differential current transformer bias voltage  |
| 3     | CTS        | Differential current signal input              |
| 4     | CTO        | Differential current to voltage output         |
| 5     | IDF        | Differential low pass filter/ADC input         |
| 6     | REF        | 3.3 V Internal reference voltage               |
| 7     | GND        | Electronics ground                             |
| 8     | Phase      | Zero cross input for V <sub>AC</sub> frequency |
| 9     | SUP        | Power supply input                             |
| 10    | AUX        | Auxiliary power supply input                   |
| 11    | LED        | End of life LED drive                          |
| 12    | TE         | Test enable, Connect to GND                    |
| 13    | Fault Test | Differential self-test output signal           |
| 14    | SCR        | SCR gate drive signal                          |

**Table 2. ABSOLUTE MAXIMUM RATINGS**

| Rating                                                                            | Symbol             | Value                                                      | Unit |
|-----------------------------------------------------------------------------------|--------------------|------------------------------------------------------------|------|
| Supply Voltage Range                                                              | $V_s$              | 13.5                                                       | V    |
| Supply Current                                                                    | $I_s$              | 10                                                         | mA   |
| Input Voltage Range (Note 3)                                                      | $V_{in}$           | -0.3 to 3.6                                                | V    |
| Output Voltage Range                                                              | $V_{out}$          | -0.3 to 3.6 V or ( $V_{in} + 0.3$ ),<br>whichever is lower | V    |
| Maximum Junction Temperature                                                      | $T_{J(max)}$       | 140                                                        | °C   |
| Storage Temperature Range                                                         | $T_{STG}$          | -65 to 150                                                 | °C   |
| ESD Capability, Human Body Model (Note 4)                                         | ESD <sub>HBM</sub> | 2                                                          | kV   |
| ESD Capability, Charge Device Model (Note 4)                                      | ESD <sub>CDM</sub> | 500                                                        | V    |
| Lead Temperature Soldering<br>Reflow (SMD Styles Only), Pb-Free Versions (Note 5) | $T_{SLD}$          | 260                                                        | °C   |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Functional operation above the Recommended Operating Conditions is not implied. Extended
2. Exposure to stresses above the Recommended Operating Conditions may affect device reliability.
3. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
4. This device series incorporates ESD protection and is tested by the following methods:  
 ESD Human Body Model tested per AEC-Q100-002 (JEDEC JS-001-2010)  
 ESD Charge Device Model tested per AEC-Q100-003 (JEDEC JESD22-C101-A)  
 Latchup Current Maximum Rating:  $\leq 100$  mA, 20  $\mu$ s pulse per JEDEC standard: JESD78
5. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERM.D

**Table 3. THERMAL CHARACTERISTICS**

| Rating                                                                           | Symbol          | Value | Unit |
|----------------------------------------------------------------------------------|-----------------|-------|------|
| Thermal Characteristics, TSSOP14<br>Thermal Resistance, Junction-to-Air (Note 6) | $R_{\theta JA}$ | 115   | °C/W |

6. Values based on copper area of 645 mm<sup>2</sup> (or 1 in<sup>2</sup>) of 1 oz copper thickness and FR4 PCB substrate.

**Table 4. OPERATING RANGES** (Unless otherwise noted, ISUP = 3 mA, Phase input = 60 Hz, Refer to Figure 2)

| Parameter                               | Conditions                  | Min  | Typ  | Max  | Units   |
|-----------------------------------------|-----------------------------|------|------|------|---------|
| Operating Temperature                   | Ambient                     | 0    |      | 70   | °C      |
| Shunt Regulator Voltage                 | SUP to GND, ISUP = 1 mA     |      | 12   | 13   | V       |
| Shunt Regulator Current                 | ISUP                        |      |      | 10   | mA      |
| Quiescent Current                       | ISUP, SUP = 10.5 V          |      | 575  | 800  | μA      |
| RMS Trip Threshold Voltage              | IDF to CTB, R5 = 32 kΩ      | 191  | 203  | 215  | mV      |
| SCR Trigger Current                     | ISCR                        |      |      | 4    | mA      |
| SCR Trigger Output Voltage              | SCR to GND, SUP > 4 V       | 3    |      | 3.6  | V       |
| LED Output Voltage                      | LED to GND, SUP > 4 V       | 3    |      | 3.6  | V       |
| CTB Bias Voltage                        | CTB to GND, REF = 3.3 V     |      | 1.65 |      | V       |
| CTS–CTB Absolute Offset Voltage         | CTS–CTB                     | –300 |      | 300  | μV      |
| Ground Fault Response Time              | 6 mA ≤ IDIFF < 15 mA        |      |      | 150  | ms      |
| Ground Fault Response Time              | 15 mA ≤ IDIFF < 30 mA       |      |      | 100  | ms      |
| Ground Fault Response Time              | 30 mA ≤ IDIFF < 100 mA      |      |      | 40   | ms      |
| Ground Fault Response Time              | IDIFF ≥ 100 mA              |      |      | 25   | ms      |
| Internal Oscillator Frequency           | FAC = 60 Hz +/-0.1          | 1.8  | 2    | 2.2  | MHz     |
| Phase Pin Max Clamp Current             | Iphase Max Sink Current     |      |      | 400  | μA      |
| Phase Pin Pull Down Current             | Phase = 1 V                 |      | 1    |      | μA      |
| First ST Timer                          | SUP > 4 V                   | 0.75 | 1    | 1.25 | seconds |
| Periodic ST Timer, Pass                 | Steady State, ST Pass       | 9    | 12   | 15   | minutes |
| Periodic ST Timer, Fail                 | ST Fail                     | 4    | 4.5  | 5    | seconds |
| Consecutive ST Failure Timer            | ST Fail Counter, Enable SCR |      | 16   |      |         |
| LED Blink Frequency                     | ST Failure, EOL             | 3.6  | 4    | 4.4  | Hz      |
| ST Cycle GF Pass Window                 | IDIFF Ground Fault          | 5    |      | 15   | mA      |
| Phase Pin Check Wait Time to Enable EOL | No Phase signal             |      | 32   |      | ms      |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## APPLICATIONS INFORMATION

[www.onsemi.com](http://www.onsemi.com)

# NCS37020

**Table 5. RECOMMENDED EXTERNAL COMPONENTS**

| Component Type      | Instance   | Value                  | Note                                                                             |
|---------------------|------------|------------------------|----------------------------------------------------------------------------------|
| Controller          | U1         | –                      | NCS37020DTBR2G                                                                   |
| SCR                 | Q1A, Q1B   | –                      | 0.8 A, 400 V                                                                     |
| NPN                 | Q2         | –                      | MMBTA42                                                                          |
| Diode Bridge        | D1–D4      | –                      | MB4S                                                                             |
| Diode               | D5         | –                      | 1 A, 300 V                                                                       |
| Diode               | D6, D8, D9 | –                      | 15 mA, 300 V                                                                     |
| LED                 | D7         | –                      | LED for EOL Indicator                                                            |
| Capacitor           | C1         | 2.2 $\mu$ F            | SUP pin holding capacitor, Ceramic 25 V                                          |
| Capacitor           | C2         | 1 $\mu$ F              | REF filter capacitor, 6.3 V                                                      |
| Capacitor           | C3         | 100 nF                 | SCR gate filter capacitor                                                        |
| Capacitor           | C4         | 1 nF                   | Dynamic $V_{OS}$ filter capacitor                                                |
| Capacitor           | C5         | 33 nF                  | CT filter capacitor                                                              |
| Capacitor           | C6         | 2.2 nF                 | CTB bias capacitor                                                               |
| Capacitor           | C7         | 22 to 56 nF            | IDF filter capacitor                                                             |
| Resistor            | R1A        | 49.9k $\Omega$         | Shunt regulator current limit resistor, $\frac{1}{4}$ W                          |
| Resistor            | R1B        | 49.9k $\Omega$         | Shunt regulator current limit resistor, $\frac{1}{4}$ W                          |
| Resistor            | R2         | 1 M $\Omega$           | AC zero cross current limit resistor                                             |
| Resistor            | R4         | 4.7 to 20 k $\Omega$   | IDF filter resistor                                                              |
| Resistor            | R5         | 31.6 k $\Omega$        | Precision resistor (1%), Sets the differential trip level at 5 mA <sub>RMS</sub> |
| Resistor            | R7         | 243 $\Omega$           | Precision resistor (1%), Differential burden/CT low pass filter                  |
| Resistor            | R8         | 10 k $\Omega$          | Sets the self-test GF current                                                    |
| Resistor            | R9         | 3.3 k $\Omega$         | Current limit resistor for LED bias                                              |
| Resistor            | R10        | 4.7 k $\Omega$         | Current limit resistor for Q2 bias                                               |
| Resistor            | R11        | 15 k $\Omega$          | Sets the manual GF test current                                                  |
| Resistor            | R12A       | 4.7 k $\Omega$         | Current limit resistor for Q1A bias                                              |
| Resistor            | R12B       | 3.3 k $\Omega$         | Current limit resistor for Q1B bias                                              |
| Resistor            | R13        | 4.7 k $\Omega$         | SCR gate bleeder resistor                                                        |
| Ferrite Bead        | L1         | 1 k $\Omega$ @ 100 MHz | CIM05U102, CT RF filter                                                          |
| Ferrite Bead        | L2         | 1 k $\Omega$ @ 100 MHz | CIM05U102, CT RF filter                                                          |
| Current Transformer | Sense Coil | 800 turns              | C5029–01C                                                                        |

**Functional Description (refer to application circuit, Figure 2)**

The NCS37020 provides for a single IC controller solution for ground fault protection and self-test auto monitoring per UL standard UL943B.

The key internal blocks include: 12 V shunt regulator, precision bandgap reference, two 3.3 V linear regulators (one for the digital and one for the analog circuit), CT sense amplifier with  $V_{OS}$  dynamic cancellation, 1.65 V reference for the CT, 2 MHz oscillator dynamically trimmed to the AC line frequency, 8 bit SAR ADC, comparators, digital filters and digital control logic.

The internal shunt regulator clamps the SUP pin voltage at 12 volts. This provides the bias voltage for the analog and digital internal circuitry via two 3.3 V linear regulators. The NCS37020 controller can be biased full wave or half wave. Figure 2 shows a half wave bias application. Half wave bias allows for lower wattage bias resistors (R1A and R1B) and less redundant bias diodes. The D1–4 diodes are biased so that only during the positive half cycle the capacitor C1 will be charged to 12 volts. During the negative half cycle, C1 will supply the bias current for the NCS37020. To minimize the NCS37020 bias current during the negative half cycle, the SCR and LED outputs will only be enabled during the positive half cycle. The D1–4 diodes and R1A–R1B resistors include redundant components to pass the UL943B standard.

At POR (power on reset) detection ( $SUP > 4$  V) the logic is reset and the bias circuitry is enabled. The Phase pin continually checks for an input signal. There is a 1  $\mu$ A pull down internal current source connected to this pin so a floating or open pin will be biased low. If there is no 50/60 Hz signal detected on this pin for greater than 32 ms due to an open solenoid or open R2 resistor, a “no clock” End of Life (EOL) fault will occur. After ~150 ms, the LED indicator logic will be enabled and blink at 4 Hz. The SCR will be enabled for one positive half cycle every 4 seconds. The “no clock” EOL logic state will continue until a POR occurs or a 50/60 Hz signal is detected on the Phase pin. When a 50/60 Hz signal is detected, the no clock EOL state will be reset and a ST (self-test) cycle will occur after 75 ms. If this ST cycle passes, the next ST cycle will occur in 12 minutes. If four consecutive no clock ST cycles fail, a ST EOL fault will occur. During a no clock EOL state, the phase information will be detected by the shunt regulator’s bias circuitry. The shunt regulator will detect an AC zero cross by monitoring the Shunt regulator’s clamp current. When the VAC voltage crosses ~80 volts, a zero cross is registered by the shunt regulator’s circuitry.

Note, the “no clock” EOL logic can be used in production testing for generation of an EOL state and enabling the LED indicator. If a DC voltage greater than ~75 volts is applied to the Line Hot input, the NCS37020 will be biased correctly but will not see a zero cross signal and a “no clock” ST EOL failure will occur. The LED will be enabled within 150 ms.

The first self-test (ST) cycle will occur at one second and thereafter every 12 minutes. During the ST cycle, the Fault Test pin will be enabled during the positive half cycle and the CT current (set at 12 mA, R8) will be verified. During the next negative half cycle, the SCR’s anode voltage will be pre-biased by the SCR Test pin to 3.3 volts. The SCR will then be enabled and the SCR’s anode voltage will be monitored by the SCR Test pin. If the anode voltage goes below 2.1 volts, the SCR will be disabled after a 400  $\mu$ s verification check and the ST logic will register a passing ST cycle. Figure 2 shows two SCRs in series. A redundant SCR is required during the SCR anode to cathode short test to prevent the solenoid from burn out damage. The SCR self-test cycle will fail if either SCR Q1A or Q1B are open. If either Q1A or Q1B are shorted (anode to cathode) the ST cycle will pass, however, the GF function will also function correctly. The next ST cycle will occur in 12 minutes. Note that when the SCR is enabled, the blocking diode D5 will prevent the solenoid from being energized and opening the load contacts. If either the GF (ground fault) or SCR self-test cycles fail, these self-test cycles will be repeated for up to three more consecutive cycles. If any consecutive GF and SCR tests pass, the ST logic will register a passing self-test cycle. If all four ST consecutive cycles fail, a ST cycle will be repeated at 2, 3 and 4 seconds for a total of 16 self-test cycles. If all 16 ST cycles fail, a ST EOL fault will occur. The SCR will be enabled for four consecutive positive half cycles, then the LED will blink at 4 Hz. The LED will only be biased during the positive AC half wave cycle. The SCR will be enabled for one positive half cycle every 4.5 seconds. A self-test cycle will occur every second. If a self-test cycle passes, the ST EOL logic will be reset (power on reset state). If a ground fault is detected during a ST EOL state, the EOL logic will be reset. This allows for resetting the ST EOL state by pressing the manual test button when the load contacts are closed.

The above no clock and GF/SCR self-test functions provide for full UL943B (3<sup>rd</sup> Edition) compliance for the auto monitoring requirement. The NCS37020 IC controller tests for the CT, solenoid, clock input, SCR and bias circuitry.

The CT is biased at 1.65 volts. The CT sense amplifier monitors the ground fault current. This current is converted to a voltage level at the CTO pin which is the input to the ADC (IDF pin). The resistor R5 sets the GF threshold per the following equation:

$$I_{diff} = \frac{0.203 \times CT_1 \times (R_{CT1} + R_7 + 2\pi f_{AC} L_{CT1})}{R_5 \times (R_{CT1} + 2\pi f_{AC} L_{CT1})} \quad (\text{eq. 1})$$

$CT_1$  = Turns ratio of differential CT

$R_{CT1}$  = DC winding resistance of differential CT

$f_{AC}$  = AC mains frequency

$L_{CT1}$  = Inductance of differential CT

The ground fault detection circuit has different levels of time delay before the SCR is enabled:

|                 |               |
|-----------------|---------------|
| 6 mA to 15 mA   | $\leq 150$ ms |
| 15 mA to 30 mA  | $\leq 100$ ms |
| 30 mA to 100 mA | $\leq 40$ ms  |
| >100 mA         | $\leq 25$ ms  |

If a very high GF occurs and a greater than 250 mV signal occurs across the CT for greater than 1.4 ms, the saturation fault comparator will enable the SCR during the positive half cycle.

During a self-test, the GF detection circuit is active. However, for the 6 mA to 15 mA GF range, an additional ~100ms trip delay will be added before the SCR is enabled.

Note that the above equation is for an ideal CT. In practice, the GF threshold can be  $\pm 30\%$  different and should be empirically set.

The internal oscillator is trimmed to 2 MHz when the AC frequency is 60 Hz. If the AC frequency is lower, the GF trip threshold response time will be slower.

The CT sense amplifier has an internal dynamic  $V_{OS}$  cancelation circuit which allows for direct coupling to the CT transformer.

The TE pin is used for internal production testing only. This pin should be connected to the GND pin.

Contact **onsemi** for self-test requirement details and noise filtering recommendations.

#### Figure Description

Figure 3 shows the typical SCR enable delay time versus the GF current level. Shown is a typical 85 ms delay time for a 6 mA GF. The typical delay time for a 25 mA GF is 28 ms and 14 ms for a 500  $\Omega$  240 mA GF.

Figure 4 shows a passing self-test ground fault test. This test checks for the CT and bias circuitry. Channel 1 shows the VAC 120  $V_{RMS}$ , 60 Hz Line Voltage. Channel 2 shows the positive and negative phase half wave cycles. Channel 3 shows the Fault Test signal and channel 4 shows the IDF signal (CTO output). The self-test cycle starts in the positive half wave cycle. The Fault Test pin goes high and Q2 (Figure 2) is enabled. Enabling Q2 generates a GF signal via R8. The IDF signal is the CTO amplifier output which is a GF current to voltage signal per the equation on the previous page. When a 5 to 15 mA GF signal is detected, a “passing GF test” is recorded and the Fault Test signal is disabled.

Figure 5 shows a passing self-test SCR test. This test checks for the SCR and bias circuitry. Channel 1 shows the VAC 120  $V_{RMS}$ , 60 Hz Line Voltage. Channel 2 shows the positive and negative phase half wave cycles. Channel 3 shows the SCR signal and channel 4 shows the SCR Test signal. At the end of the positive half cycle, the SCR Test pin is biased high. Approximately 3 ms into the negative half wave cycle, the SCR is enabled high. This causes the SCR Test pin to go low. When it goes below ~2.1 volts, a passing SCR test is recorded and the SCR signal is disabled.

After a passing self-test cycle per Figures 4 and 5, the next ST cycle will occur in 720 seconds.

Figure 6 shows a failing ST cycle for an open CT. Channel 1 shows the NCS37020 supply voltage. Channel 2 shows the phase pin. Channel 3 shows the Fault Test signal and channel 4 shows the LED (End of Life) signal. The first four consecutive ST cycles occur at about 1.1 seconds, then at 2.2, 3.3 and 4.4 seconds. After the 16<sup>th</sup> consecutive cycle failure, the SCR is enabled for four positive half cycles and then the LED is enabled.

Figure 7 also shows a failing ST cycle for an open CT. It is a zoom figure for the first four consecutive ST cycles. It shows the same waveforms as Figure 6 but channel 4 shows the SCR pin. Comparing Figure 7 with Figure 4, it can be observed that the Fault Test pin is enabled for the complete positive half wave cycle because no GF signal is detected by the NCS37020.

Figure 8 shows a failing ST cycle for an open SCR. Channel 1 shows the supply voltage, channel 2 shows the Phase pin, channel 3 shows the SCR pin and channel 4 shows the SCR Test pin. The SCR is enabled inside the negative half wave cycle. The SCR Test pin does not detect the SCR going low so the cycle is recorded as a SCR failure test.

Figure 9 shows a failing “no clock” test. The Phase pin is floating for this test. Channel 1 shows the supply voltage, channel 2 shows the Phase pin and channel 3 shows the LED pin. No signal is present on the Phase pin after POR. At ~114 ms, the LED End of Life signal is enabled during the positive half wave cycle. The LED EOL signal blinks at 4 Hz.

Figure 10 also shows a failing “no clock” test. This figure is the same as Figure 9 except for the time scale and the SCR signal is added (channel 4). The first SCR pulse occurs at ~3.8 seconds.

# NCS37020

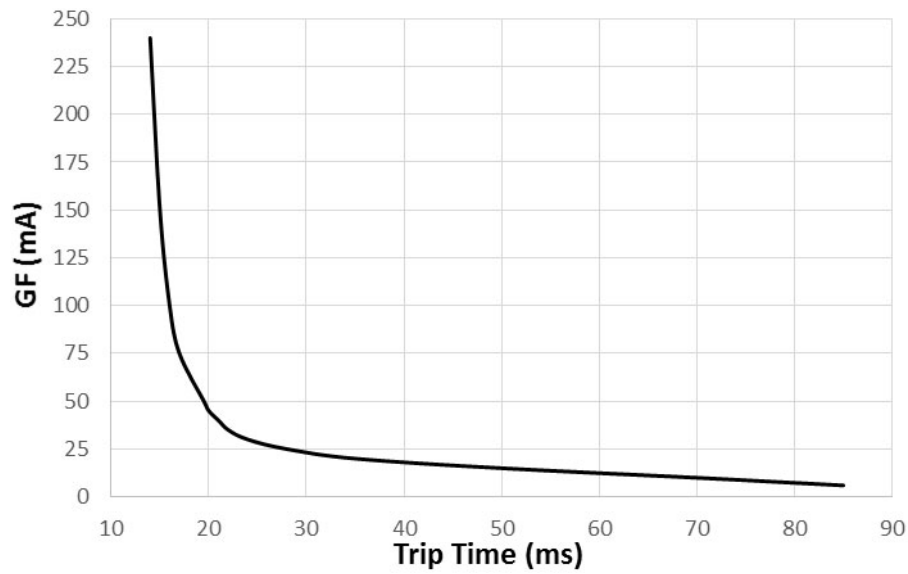


Figure 3. Typical GF Current vs. Trip Time

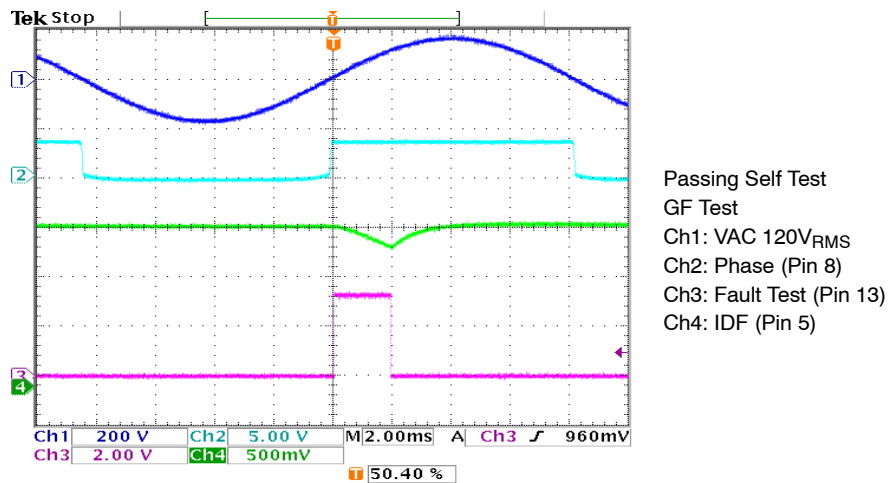


Figure 4. Passing Self Test – GF

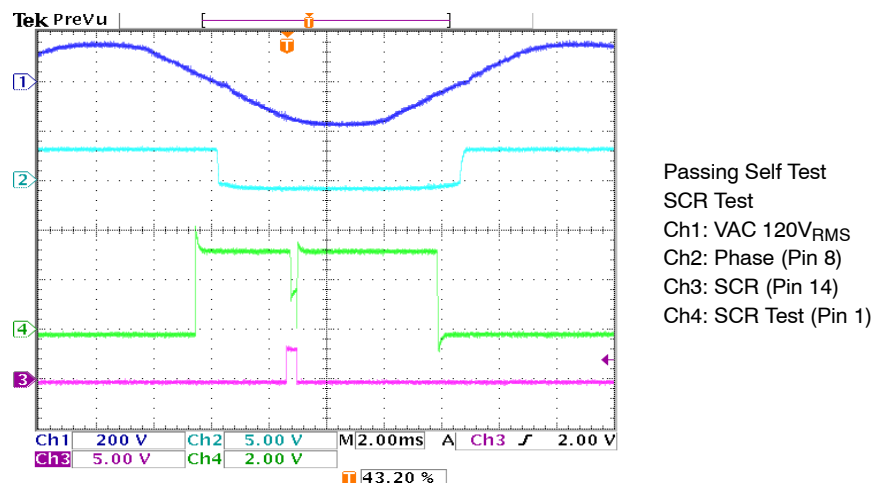


Figure 5. Passing Self Test – SCR

# NCS37020

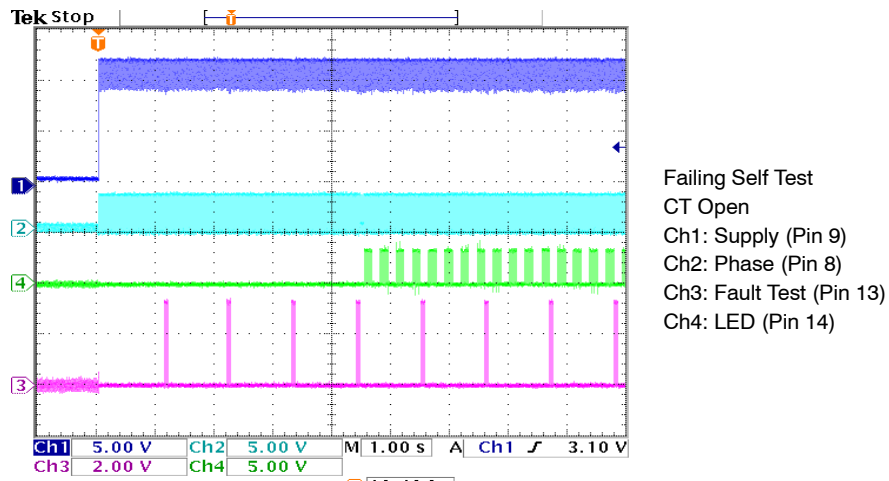


Figure 6. Failing Self Test – CT Open

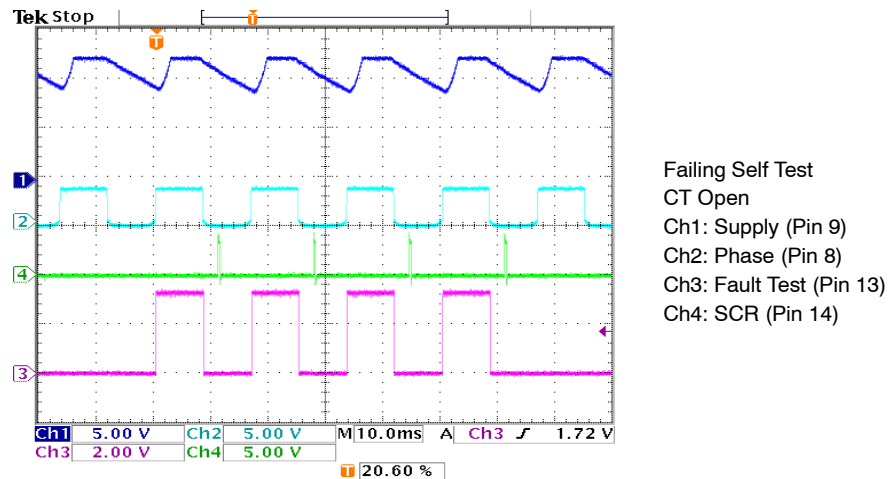


Figure 7. Failing Self Test – CT Open

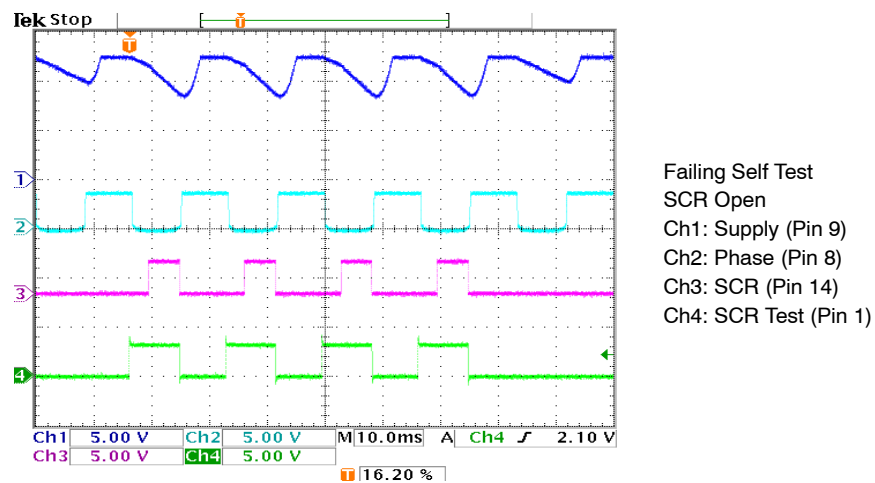


Figure 8. Failing Self Test – SCR Open

# NCS37020

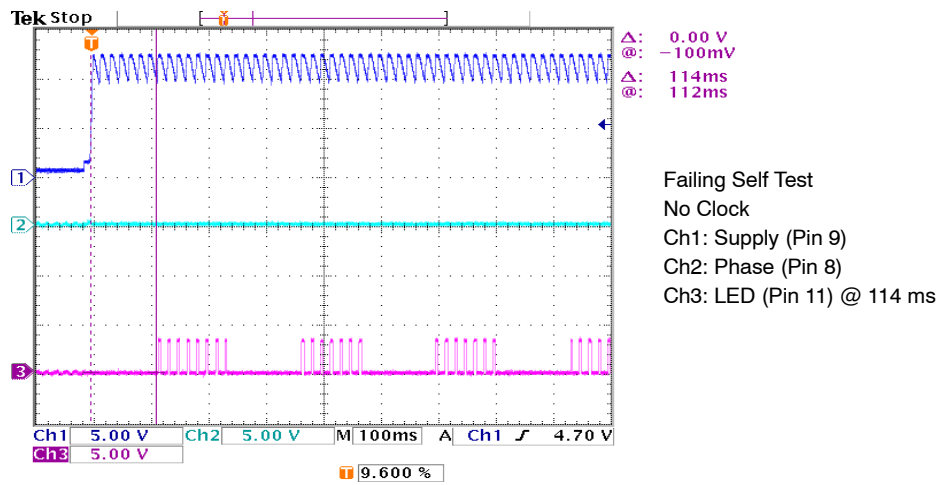


Figure 9. Failing Self Test – No Clock

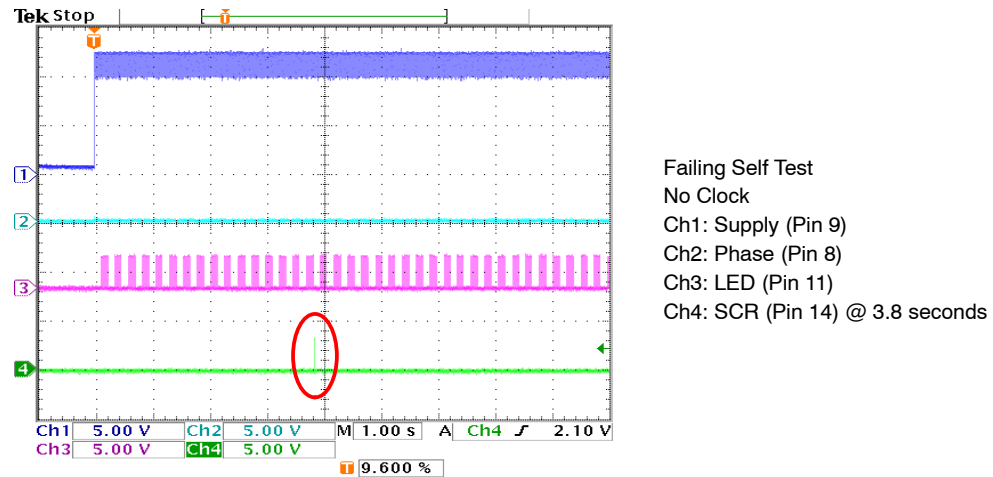
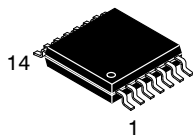


Figure 10. Failing Self Test – No Clock

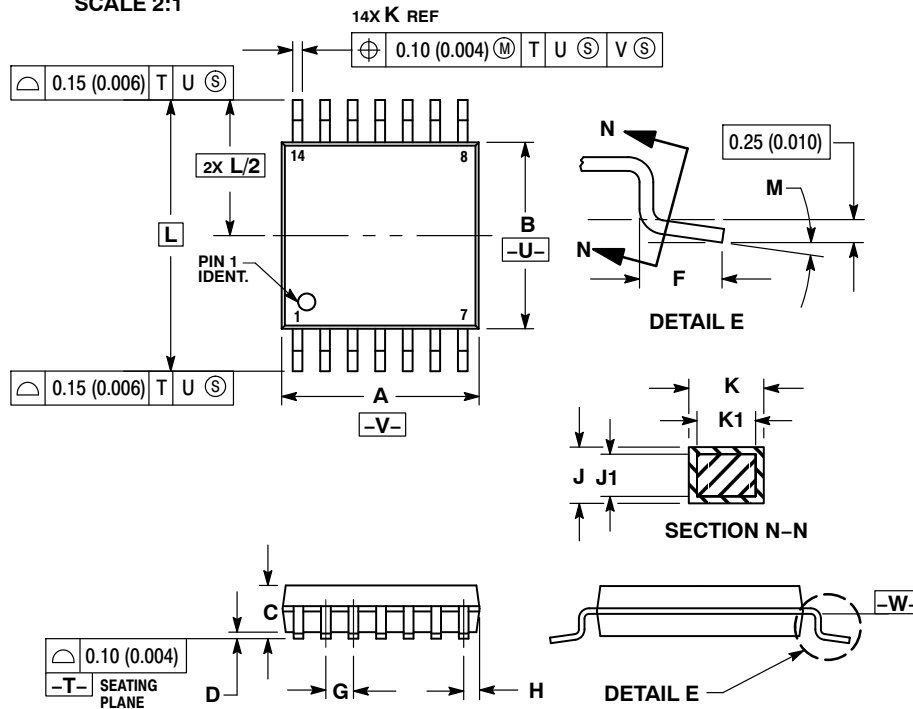
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



**TSSOP-14 WB**  
CASE 948G  
ISSUE C

DATE 17 FEB 2016

SCALE 2:1

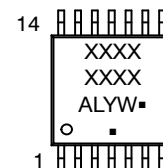


## NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.90        | 5.10 | 0.193     | 0.200 |
| B   | 4.30        | 4.50 | 0.169     | 0.177 |
| C   | ---         | 1.20 | ---       | 0.047 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.50        | 0.75 | 0.020     | 0.030 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| H   | 0.50        | 0.60 | 0.020     | 0.024 |
| J   | 0.09        | 0.20 | 0.004     | 0.008 |
| J1  | 0.09        | 0.16 | 0.004     | 0.006 |
| K   | 0.19        | 0.30 | 0.007     | 0.012 |
| K1  | 0.19        | 0.25 | 0.007     | 0.010 |
| L   | 6.40 BSC    |      | 0.252 BSC |       |
| M   | 0°          | 8°   | 0°        | 8°    |

## GENERIC MARKING DIAGRAM\*

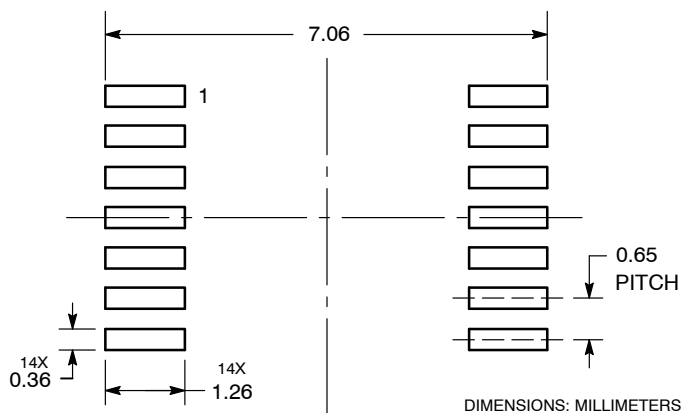


- A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

## SOLDERING FOOTPRINT



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DESCRIPTION: TSSOP-14 WB

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