# Low-Voltage SPDT Analog Switch or 2:1 Multiplexer/ De-multiplexer Bus Switch

# NC7SBU3157, FSAU3157

#### **General Description**

The NC7SBU3157 / FSAU3157 is a high-performance, single-pole / double-throw (SPDT) analog switch or 2:1 multiplexer / de-multiplexer bus switch.

The device is fabricated with advanced sub-micron CMOS technology to achieve high-speed enable and disable times and low on resistance. The break-beforemake select circuitry prevents disruption of signals on the B port due to both switches temporarily being enabled during select pin switching. The device is specified to operate over the 1.65 to 5.5 V V<sub>CC</sub> operating range. The control input tolerates voltages up to 5.5V, independent of the V<sub>CC</sub> operating range.

ON Semiconductor integrated Undershoot Hardened Circuit senses undershoot at the I/Os, and responds by preventing voltage differentials from developing and turning the switch on.

#### Features

- Analog and Digital Applications
- Space-saving, SC70 6-lead, Surface-mount Package
- Low On Resistance: <10  $\Omega$  on typical at 3.3 V V<sub>CC</sub>
- Broad V<sub>CC</sub> Operating Range: 1.65 V to 5.5 V
- Rail-to-rail Signal Handling
- Power-down, High-impedance Control Input
- Over-voltage Tolerance of Control Input to 7.0 V
- Break–before–make Enable Circuitry
- 250 MHz, 3 dB Bandwidth
- This Device is Pb-Free and is RoHS Compliant

#### FUNCTION TABLE

Input (S)	Function
Logic Level Low	B <sub>0</sub> Connected to A
Logic Level High	B <sub>1</sub> Connected to A

#### **PIN DESCRIPTIONS**

Pin Names	Description
A, B <sub>0</sub> , B <sub>1</sub>	Data Ports
S	Control Input



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SC-88 (SC-70 6 Lead), 1.25x2 CASE 419AD

#### **CONNECTION DIAGRAM**



Pin Assignment SC-70

#### MARKING DIAGRAM



NOTE:

Orientation of top mark determines pin one location. Read the top mark left to right and pin one is the lower left pin.

**Pin One Orientation** 

#### **ORDERING INFORMATION**

See detailed ordering and shipping information on page 2 of this data sheet.





Figure 1. Logic Symbol

Figure 2. Analog Symbol

#### **ORDERING INFORMATION**

Part Number	umber Top Mark Operating Temperature Rang		Part Number     Top Mark     Operating Temperature Range     Package		Package	Shipping <sup>†</sup>
NC7SBU3157P6X	U7A	–40 to 85°C	SC70 (Pb-Free)	3000 units / Tape & Reel		
FSAU3157P6X	U7A	–40 to 85°C	SC70 (Pb-Free)	3000 units / Tape & Reel		

+For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

#### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Units
V <sub>CC</sub>	Supply Voltage	-0.5	+7.0	V
VS	DC Switch Voltage (Note 1)	-0.5	V <sub>CC</sub> + 0.5	V
V <sub>IN</sub>	DC Input Voltage (Note 1)	-0.5	+7.0	V
Ι <sub>ΙΚ</sub>	DC Input Diode Current at V <sub>IN</sub> < 0 V		-50	mA
I <sub>OUT</sub>	DC Output Current		128	mA
I <sub>CC</sub> /I <sub>GND</sub>	DC V <sub>CC</sub> or Ground Current		±100	mA
T <sub>STG</sub>	Storage Temperature Range	-65	+150	°C
TJ	Junction Temperature Under Bias		+150	°C
TL	Junction Lead Temperature (Soldering, 10 seconds)		+260	°C
PD	Power Dissipation at +85°C		180	mW

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

#### **RECOMMENDED OPERATING CONDITIONS**

Symbol		Min	Max	Units	
V <sub>CC</sub>	Supply Voltage Operating		1.65	5.50	V
V <sub>IN</sub>	Control Input Voltage (Note 2)		0	V <sub>CC</sub>	V
V <sub>IN</sub>	Switch Input Voltage (Note 2)		0	V <sub>CC</sub>	V
V <sub>OUT</sub>	Output Voltage (Note 2)			V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature			+85	°C
	Input Disc and Fall Time	Control Input $V_{CC} = 2.3 \text{ V} - 3.6 \text{ V}$	0	10	ns/V
۲, ۱f	Input Rise and Fail Time	Control Input $V_{CC} = 4.5 \text{ V} - 5.5 \text{ V}$	0	5	ns/V
θ <sub>JA</sub>	Thermal Resistance			350	°C/W

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

2. Control input must be held HIGH or LOW; it must not float.

#### DC ELECTRICAL CHARACTERISTICS

				T <sub>A</sub> = +25°C		$T_A = -40^{\circ}$	C to +85°C		
Symbol	Parameter	Conditions	V <sub>cc</sub> (V)	Min.	Тур.	Max.	Min.	Max.	Units
Ин	High Level Input Voltage		1.65 to 1.95	$0.75 V_{CC}$			$0.75 V_{CC}$		V
•	riigh zovor input voltage		2.3 to 5.5	$0.7 V_{CC}$			$0.7 V_{CC}$		v
VII	Low Level Input Voltage		1.65 to 1.95			$0.25 \ V_{CC}$		$0.25  V_{CC}$	V
VIL	Low Love input vehage		2.3 to 5.5			$0.3  V_{CC}$		$0.3  V_{CC}$	v
lin	Input Leakage Current	$0 \leq V_{IN} \leq 5.5V$	0 to 5.5		±0.05	±0.1		±1	μΑ
IOFF	Off State Leakage Current	$0 \le A, B \le V_{CC}$	1.65 to 5.5		±0.05	±0.1		±1	μA
Ron	Switch On Resistance	V <sub>IN</sub> =0V, I <sub>O</sub> =30mA	4.5		3.0	15.0		15.0	Ω
	(1010-0)	V <sub>IN</sub> =2.4V, I <sub>O</sub> =-30mA			5.0	15.0		15.0	
		V <sub>IN</sub> =4.5V, I <sub>O</sub> =-30mA			7.0	15.0		15.0	
		V <sub>IN</sub> =0V, I <sub>O</sub> =24mA	3.0		4.0	20.0		20.0	
		V <sub>IN</sub> =3V, I <sub>O</sub> =-24mA			10.0	20.0		20.0	
		V <sub>IN</sub> =0V, I <sub>O</sub> =8mA	2.3		5.0	30.0		30.0	
		V <sub>IN</sub> =2.3V, I <sub>O</sub> =-8mA			13.0	30.0		30.0	
		V <sub>IN</sub> =0V, I <sub>O</sub> =4mA	1.65		6.5	50.0		50.0	
		V <sub>IN</sub> =1.65V, I <sub>O</sub> =–4mA			17.0	50.0		50.0	
lcc	Quiescent Supply Cur- rent; All Channels On or Off	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0	5.5			1		10	μΑ
	Analog Signal Range		Vcc	0		Vcc	0	Vcc	V
RRANGE	On Resistance Over	$I_A$ =-30mA, 0 $\leq$ V <sub>Bn</sub> $\leq$ V <sub>CC</sub>	4.5					25.0	Ω
	(Notes 3, 7)	$I_A$ =-24mA, 0 $\leq$ V <sub>Bn</sub> $\leq$ V <sub>CC</sub>	3.0					50.0	
		$I_A$ =-8mA, $0 \le V_{Bn} \le V_{CC}$	2.3					100	
		$I_A$ =-4mA, $0 \le V_{Bn} \le V_{CC}$	1.65					300	
$\Delta R_{ON}$	On Resistance Match	I <sub>A</sub> =-30mA, V <sub>Bn</sub> =3.15	4.5		0.15				Ω
	(Notes 3, 4, 5)	I <sub>A</sub> =-24mA, V <sub>Bn</sub> 2.1	3.0		0.2				
		I <sub>A</sub> =-8mA, V <sub>Bn</sub> =1.6	2.3		0.5				
		I <sub>A</sub> =–4mA, V <sub>Bn</sub> =1.15	1.65		0.5				
νικυ	Voltage Under- shoot	0.0mA ≤ I <sub>IN</sub> ≤–50, <del>OE</del> 5.5v	5.5					-2	V
Rflat	On Resistance Flatness	$I_{A}\text{=-30mA, 0} \leq V_{Bn} \leq V_{CC}$	5.0		6.0				Ω
	(110185 3, 4, 0)	$I_A = -24 m A, \ 0 \le V_{Bn} \le V_{CC}$	3.3		12.0				1
		$I_{A}\text{=-8mA, 0} \leq V_{Bn} \leq V_{CC}$	2.5		28.0				1
		$I_{A}\text{=}-4mA,0\leq V_{Bn}\leq V_{CC}$	1.8		125				1

Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B Ports).
Parameter is characterized, but not tested in production.
ΔR<sub>ON</sub> = R<sub>ON</sub> max - R<sub>ON</sub> minimum measured at identical V<sub>CC</sub>, temperature, and voltage levels.
Flatness is defined as the difference between the maximum and minimum value of on resistance over the specified range of conditions.
Guaranteed by design.

#### AC ELECTRICAL CHARACTERISTICS

				т	<sub>A</sub> = +25°	°C	T <sub>A</sub> = -40°C	C to +85°C		
Symbol	Parameter	Conditions	Vcc (V)	Min.	Тур.	Max.	Min.	Max.	Units	Figure
tphl, tplh	Propagation Delay	V <sub>I</sub> = OPEN	1.65 to 1.95						ns	Figure 5
	Bus-IO-Bus (Note o)		2.3 to 2.7			1.2		1.2		Figure 6
			3.0 to 3.6			0.8		0.8		
			4.5 to 5.5			0.3		0.3		
tPZL, tPZH	Output Enable Time	$V_1 = 2 \times V_{CC}$ for $t_{PZL}$	1.65 to 1.95	7.0		23.0	7.0	24.0	ns	Figure 5
	$(A \text{ to } B_n)$	$v_1 = 0$ v ioi $t_{PZH}$	2.3 to 2.7	3.5		13.0	3.5	14.0		Figure 6
			3.0 to 3.6	2.5		6.9	2.5	7.6		
			4.5 to 5.5	1.7		5.2	1.7	5.7		
tplz, tphz	Output Disable Time	$V_1 = 2 \times V_{CC}$ for $t_{PLZ}$	1.65 to 1.95	3.0		12.5	3.0	13.0	ns	Figure 5
	(A Port to B Port)	D B Port) $V_1 = 0 V \text{ for } t_{PHZ}$	2.3 to 2.7	2.0		7.0	2.0	7.5		Figure 6
	. ,		3.0 to 3.6	1.5		5.0	1.5	5.3		
			4.5 to 5.5	0.8		3.5	0.8	3.8		
tввм	Break–Before–Make		1.65 to 1.95	0.5			0.5		ns	Figure 7
	Time (Note 9)		2.3 to 2.7	0.5			0.5			
			3.0 to 3.6	0.5			0.5			
			4.5 to 5.5	0.5			0.5			
Q	Charge Injection	$C_L = 0.1 \text{ nF}, V_{GEN} = 0 \text{ V}$	5.0		7.0				рС	Figure 8
	(Note 9)	$R_{GEN} = 0 \Omega$	3.3		3.0					
OIRR	Off Isolation (Note 10)	$R_L = 50 \Omega$ , f = 10 MHz	1.65 to 5.5		-57.0				dB	Figure 9
Xtalk	Crosstalk	$R_L = 50 \Omega$ , f = 10 MHz	1.65 to 5.5		-54.0				dB	Figure 10
BW	–3dB Bandwidth	R <sub>L</sub> = 50 Ω	1.65 to 5.5		250				MHz	Figure 13
THD	Total Harmonic Distor- tion (Note 9)	$R_L$ = 600 Ω, 0.5 V <sub>PP</sub> , f = 20 Hz to 20 KHz	5.0		.011				%	

8. This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).

9. Guaranteed by design.

10. Off Isolation = 20  $\log_{10} [V_A / V_{Bn}]$ .

#### CAPACITANCE (Note 11)

Symbol	Parameter	Conditions	Тур.	Max.	Units	Figure
CIN	Control Pin Input Capacitance	$V_{CC} = 0 V$	2.3		pF	
Сю-в	B Port Off Capacitance	$V_{CC} = 5.0 V$	6.5		pF	Figure 11
CIOA-ON	A Port Capacitance When Switch Is Enabled	$V_{CC} = 5.0 V$	18.5		pF	Figure 12

11.  $T_A = +25^{\circ}C$ , f = 1 MHz, Capacitance is characterized, but not tested in production.

#### UNDERSHOOT CHARACTERISTIC (Note 12)

Symbol	Parameter	Min.	Тур.	Units	Figure
νουτυ	Output Voltage During Undershoot	2.5	V <sub>OH</sub> – 0.3	V	Figure 3

12. This test is intended to characterize the device's protective capabilities by maintaining output signal integrity during an input transient voltage undershoot event.



Figure 3. Output Voltage During Undershoot

#### **DEVICE TEST CONDITIONS**

Parameter Value		Units
V <sub>IN</sub>	see Figure 4	V
$R_1 = R_2$	100	KΩ
V <sub>TRI</sub>	7.0	V
V <sub>CC</sub>	5.5	V



#### Figure 4. Transient Input Voltage Waveform

#### AC Loading and Waveforms



Notes:

Input driven by 50  $\Omega$  source terminated in 50  $\Omega.$  C<sub>L</sub> includes load and stray capacitance, C<sub>L</sub> = 50 pF Input PRR = 1.0 MHz, t<sub>W</sub> = 500 ns

### Figure 5. AC Test Circuit





#### AC Loading and Waveforms (continued)





Figure 13. Bandwidth

#### SC-88 (SC-70 6 Lead), 1.25x2 CASE 419AD ISSUE A

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SIDE VIEW

#### Notes:

(1) All dimensions are in millimeters. Angles in degrees.

(2) Complies with JEDEC MO-203.



END VIEW

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