

NTR4170N

MOSFET – Power, Single, N-Channel, SOT-23

30 V, 3.1 A

Features

- Low $R_{DS(on)}$
- Low Gate Charge
- Low Threshold Voltage
- Halide Free
- This is a Pb-Free Device

Applications

- Power Converters for Portables
- Battery Management
- Load/Power Switch

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V_{DSS}	30	V
Gate-to-Source Voltage		V_{GS}	± 12	V
Continuous Drain Current (Note 1)	Steady State	I_D	2.4	A
	$t \leq 30$ s		3.1	
	$t \leq 10$ s		3.9	
	Steady State	I_D	1.7	
	$t \leq 30$ s		2.3	
	$t \leq 10$ s		2.8	
Power Dissipation (Note 1)	Steady State	P_D	0.48	W
	$t \leq 30$ s		0.82	
	$t \leq 10$ s	P_D	1.25	
Pulsed Drain Current	$t_p = 10$ μ s	I_{DM}	8.0	A
Operating Junction and Storage Temperature		T_J, T_{stg}	-55 to 150	$^\circ\text{C}$
Source Current (Body Diode)		I_S	0.82	A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T_L	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	260	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – $t \leq 30$ s	$R_{\theta JA}$	153	
Junction-to-Ambient – $t < 10$ s (Note 1)	$R_{\theta JA}$	100	

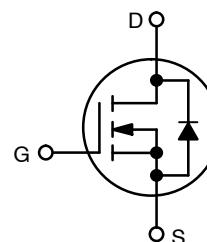


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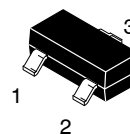
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$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
30 V	55 m Ω @ 10 V	3.1 A
	70 m Ω @ 4.5 V	2.8 A
	110 m Ω @ 2.5 V	2.0 A

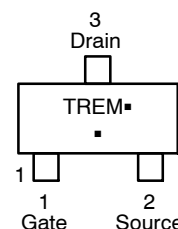
SIMPLIFIED SCHEMATIC – N-CHANNEL



MARKING DIAGRAM/ PIN ASSIGNMENT



SOT-23
CASE 318
STYLE 21



TRE = Specific Device Code
M = Date Code
▪ = Pb-Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTR4170NT1G	SOT-23 (Pb-Free)	3000/Tape & Reel
NTR4170NT3G	SOT-23 (Pb-Free)	10000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NTR4170N

1. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).

NTR4170N

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} / T _J	I _D = 250 μA, Reference to 25°C		26.4		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 24 V, T _J = 25°C V _{GS} = 0 V, V _{DS} = 24 V, T _J = 125°C			1.0 5.0	μA
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 12 V			± 100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250 μA	0.6	1.0	1.4	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} / T _J			3.3		mV/°C
Drain-to-Source On-Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 3.2 A		45	55	mΩ
		V _{GS} = 4.5 V, I _D = 2.8 A		50	70	
		V _{GS} = 2.5 V, I _D = 2.0 A		64	110	
Forward Transconductance	g _{FS}	V _{DS} = 5.0 V, I _D = 3.2 A		8.0		S

CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C _{iss}	V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = 15 V		432		pF
Output Capacitance	C _{oss}			53.6		
Reverse Transfer Capacitance	C _{rss}			37.1		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 4.5 V, V _{DS} = 15 V, I _D = 3.2 A		4.76		nC
Threshold Gate Charge	Q _{G(TH)}			0.3		
Gate-to-Source Charge	Q _{GS}			1.0		
Gate-to-Drain Charge	Q _{GD}			1.4		
Gate Resistance	R _G			3.8		Ω

SWITCHING CHARACTERISTICS, V_{GS} = 4.5 V (Note 4)

Turn-On Delay Time	t _{d(on)}	V _{GS} = 4.5 V, V _{DD} = 15 V, I _D = 3.2 A, R _G = 6.2 Ω		6.4		ns
Rise Time	t _r			9.9		
Turn-Off Delay Time	t _{d(off)}			15.1		
Fall Time	t _f			3.5		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 1.0 A, T _J = 25°C		0.75	1.0	V
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, I _S = 1.0 A, dI _{SD} /dt = 100 A/μs		8.0		ns
Charge Time	t _a			5.1		
Discharge Time	t _b			2.9		
Reverse Recovery Charge	Q _{RR}			2.9		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Surface-mounted on FR4 board using 1 in sq pad size (CU area = 1.127 in sq [2 oz] including traces).

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

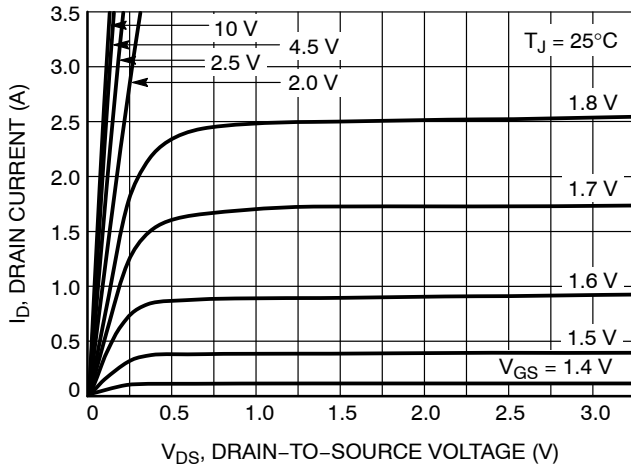


Figure 1. On-Region Characteristics

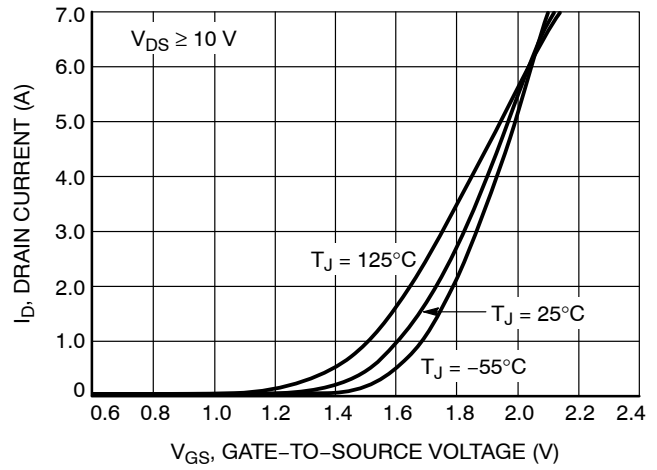


Figure 2. Transfer Characteristics

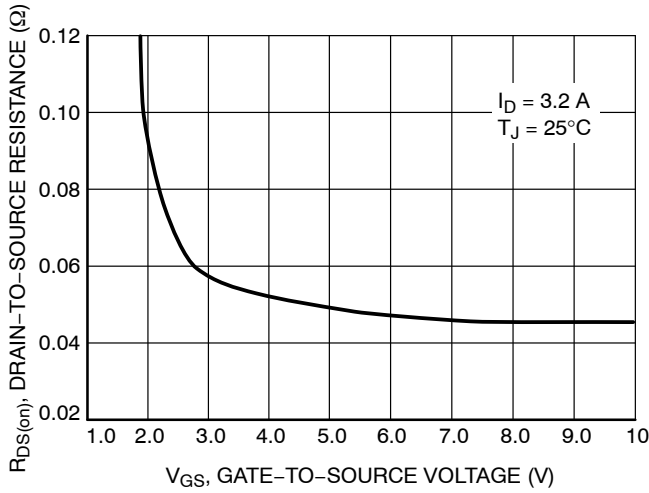


Figure 3. On-Resistance vs. Gate Voltage

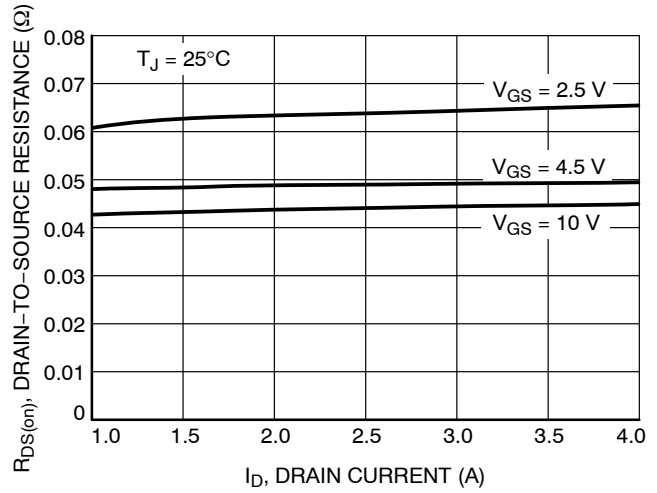


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

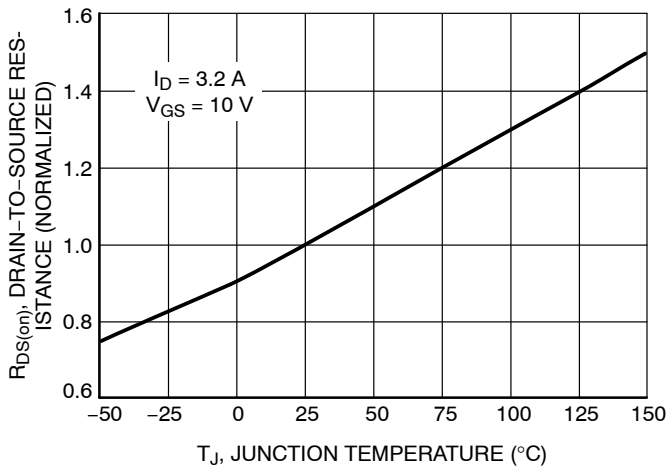


Figure 5. On-Resistance Variation with Temperature

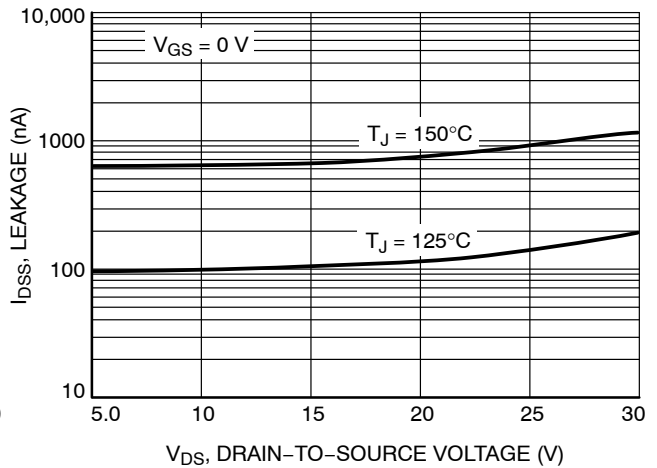


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

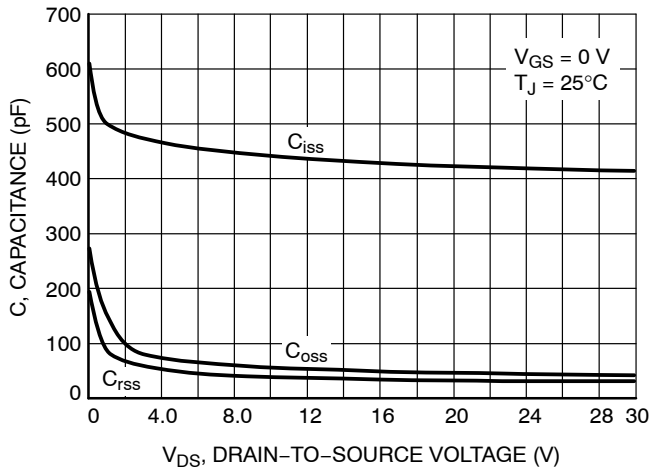


Figure 7. Capacitance Variation

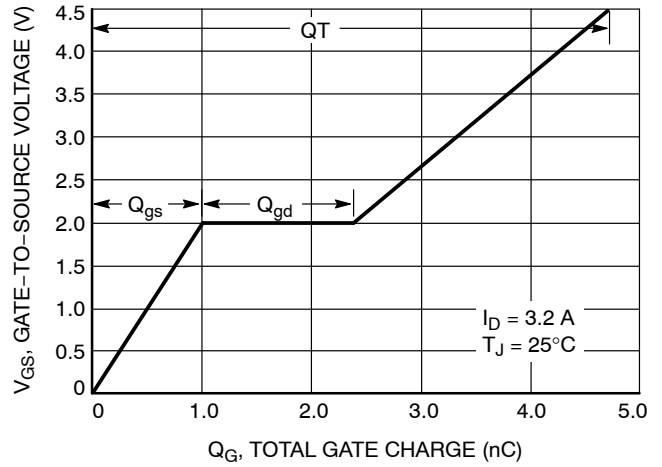


Figure 8. Gate-to-Source Voltage vs. Total Charge

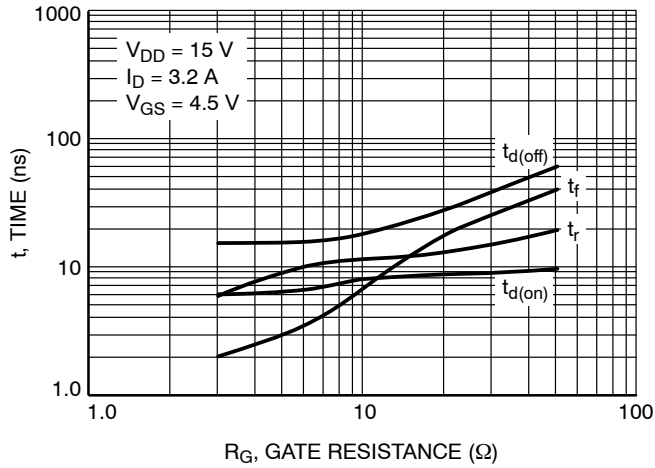


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

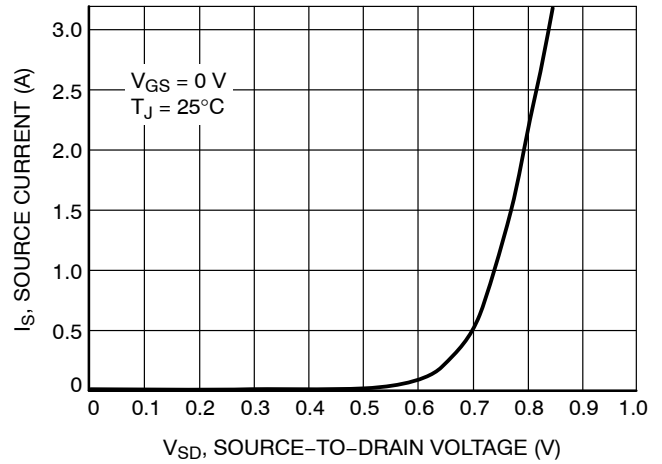
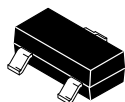


Figure 10. Diode Forward Voltage vs. Current

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 4:1

SOT-23 (TO-236)
CASE 318
ISSUE AT

DATE 01 MAR 2023

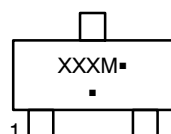


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

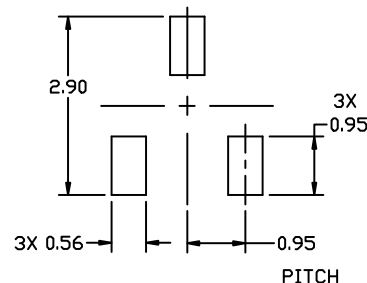
DIM	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
c	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
H _E	2.10	2.40	2.64	0.083	0.094	0.104
T	0°	---	10°	0°	---	10°

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS



SOT-23 (TO-236) CASE 318 ISSUE AT

DATE 01 MAR 2023

STYLE 1 THRU 5: CANCELLED	STYLE 6: PIN 1. BASE 2. EMITTER 3. COLLECTOR	STYLE 7: PIN 1. EMITTER 2. BASE 3. COLLECTOR	STYLE 8: PIN 1. ANODE 2. NO CONNECTION 3. CATHODE		
STYLE 9: PIN 1. ANODE 2. ANODE 3. CATHODE	STYLE 10: PIN 1. DRAIN 2. SOURCE 3. GATE	STYLE 11: PIN 1. ANODE 2. CATHODE 3. CATHODE-ANODE	STYLE 12: PIN 1. CATHODE 2. CATHODE 3. ANODE	STYLE 13: PIN 1. SOURCE 2. DRAIN 3. GATE	STYLE 14: PIN 1. CATHODE 2. GATE 3. ANODE
STYLE 15: PIN 1. GATE 2. CATHODE 3. ANODE	STYLE 16: PIN 1. ANODE 2. CATHODE 3. CATHODE	STYLE 17: PIN 1. NO CONNECTION 2. ANODE 3. CATHODE	STYLE 18: PIN 1. NO CONNECTION 2. CATHODE 3. ANODE	STYLE 19: PIN 1. CATHODE 2. ANODE 3. CATHODE-ANODE	STYLE 20: PIN 1. CATHODE 2. ANODE 3. GATE
STYLE 21: PIN 1. GATE 2. SOURCE 3. DRAIN	STYLE 22: PIN 1. RETURN 2. OUTPUT 3. INPUT	STYLE 23: PIN 1. ANODE 2. ANODE 3. CATHODE	STYLE 24: PIN 1. GATE 2. DRAIN 3. SOURCE	STYLE 25: PIN 1. ANODE 2. CATHODE 3. GATE	STYLE 26: PIN 1. CATHODE 2. ANODE 3. NO CONNECTION
STYLE 27: PIN 1. CATHODE 2. CATHODE 3. CATHODE	STYLE 28: PIN 1. ANODE 2. ANODE 3. ANODE				

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