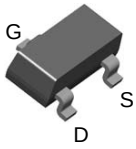
N-Channel RF Amplifier

J211, MMBFJ211

1. Drain
2. Source
3. Gate

Bent Lead
Tape & Reel
Ammo Packing

TO−92 3
CASE 135AR



NOTE: Source & Drain are interchangeable

SOT−23
CASE 318−08

Description

This device is designed for HF/VHF mixer/amplifier and applications where process 50 is not adequate. Sufficient gain and low−noise for sensitive receivers. Sourced from process 90.

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted) (Notes 1, 2)

Symbol	Parameter	Value	Unit
V_{DG}	Drain−Gate Voltage	25	V
V_{GS}	Gate−Source Voltage	−25	V
I_{GF}	Forward Gate Current	10	mA
T_J, T_{STG}	Operating and Storage Junction Temperature Range	−55 to 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

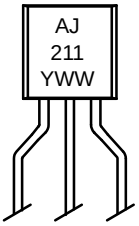
1. These ratings are based on a maximum junction temperature of 150°C.
2. These are steady−state limits. **onsemi** should be consulted on applications involving pulsed or low− duty−cycle operations.

THERMAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

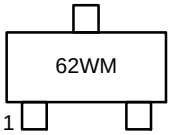
Symbol	Parameter	Max		Unit
		J211 (Note 3)	**MMBFJ211** (Note 3)	
P_D	Total Device Dissipation	350	225	mW
	Derate Above 25°C	2.8	1.8	mW/°C
$R_{\theta JC}$	Thermal Resistance, Junction−to−Case	125	−	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient	357	556	°C/W

3. Device mounted on FR−4 PCB 36 mm x 18 mm x 1.5 mm; mounting pad for the collector lead minimum 6 cm^2.

MARKING DIAGRAM



J211−D74Z



MMBFJ211

J211, 62W = Device Code
A = Assembly Site
WW = Work Week Number
Y = Year of Production
M = Date Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Max	Unit
OFF CHARACTERISTICS					
$V_{(BR)GSS}$	Gate−Source Breakdown Voltage	I_G = 1.0 μA, V_{DS} = 0	−25	−	V
I_{GSS}	Gate Reverse Current	V_{GS} = 15 V, V_{DS} = 0	−	−100	pA
V_{GS}(off)	Gate−Source Cut−Off Voltage	V_{DS} = 15 V, I_D = 1.0 nA	−2.5	−4.5	V
ON CHARACTERISTICS					
I_{DSS}	Zero−Gate Voltage Drain Current (Note 4)	V_{DS} = 15 V, V_{GS} = 0	7.0	20	mA
SMALL SIGNAL CHARACTERISTICS					
g_{fs}	Common Source Forward Transconductance	V_{DS} = 15 V, V_{GS} = 0, f = 1.0 kHz	7000	12000	μmhos
g_{oss}	Common Source Output Conductance	V_{DS} = 15 V, V_{GS} = 0, f = 1.0 kHz	−	200	μmhos

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse test: pulse width ≤ 300 μs

TYPICAL PERFORMANCE CHARACTERISTICS

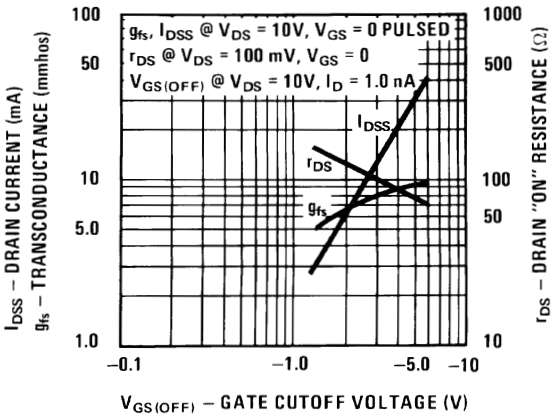


Figure 1. Parameter Interactions

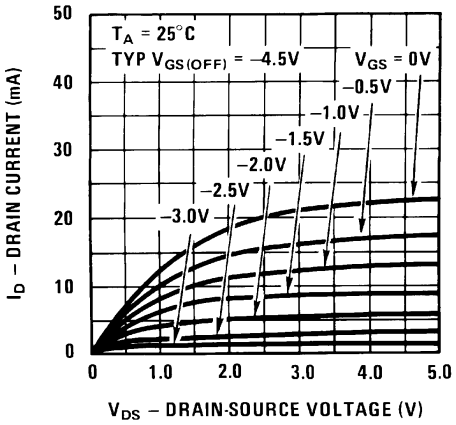


Figure 2. Common Drain−Source

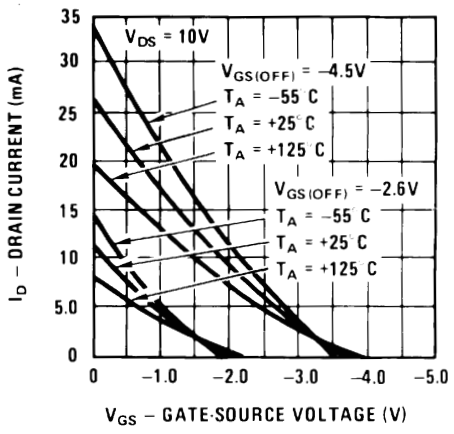


Figure 3. Transfer Characteristics

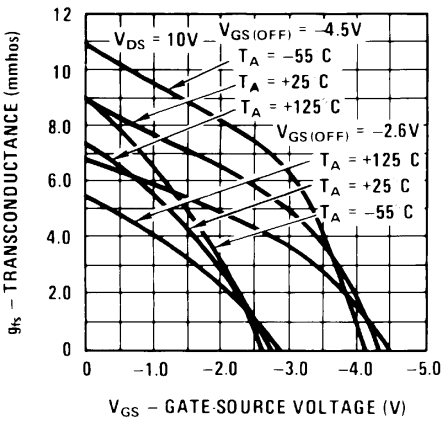


Figure 4. Transfer Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

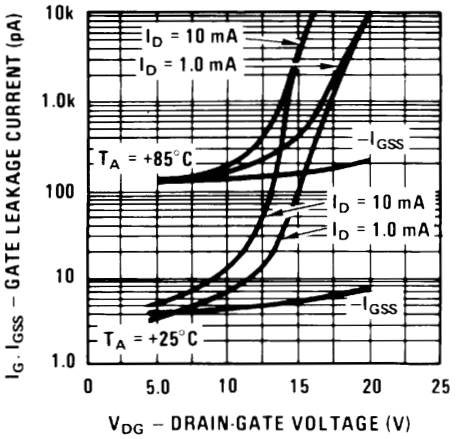


Figure 5. Leakage Current vs. Voltage

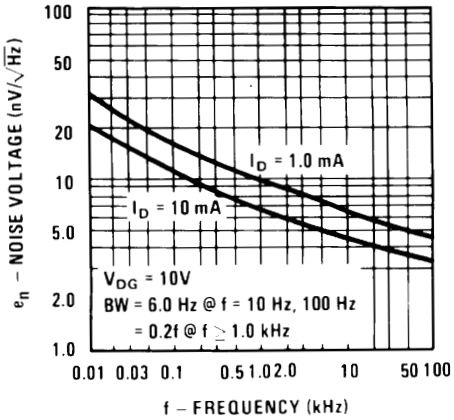


Figure 6. Noise Voltage vs. Frequency

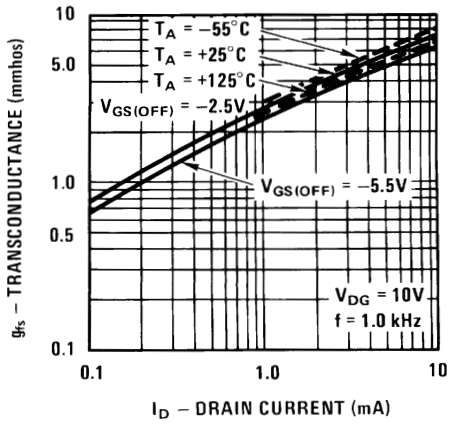


Figure 7. Transconductance vs. Drain Current

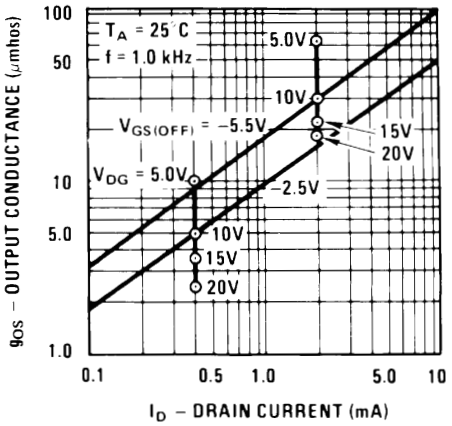


Figure 8. Output Conductance vs. Drain Current

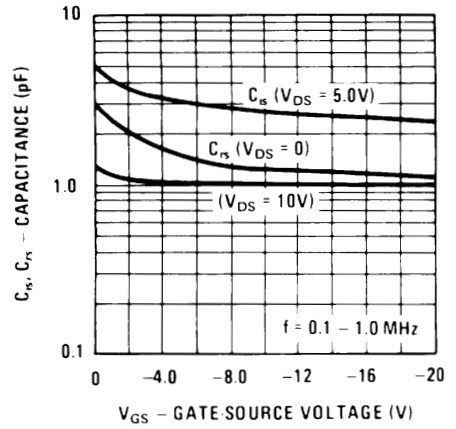


Figure 9. Capacitance vs. Voltage

COMMON SOURCE CHARACTERISTICS

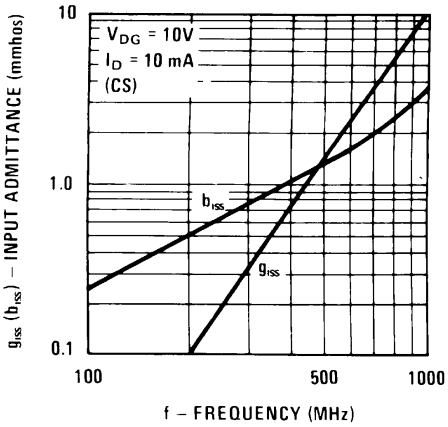


Figure 10. Input Admittance

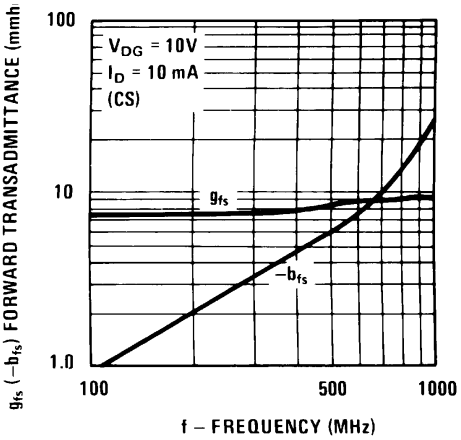


Figure 11. Forward Transadmittance

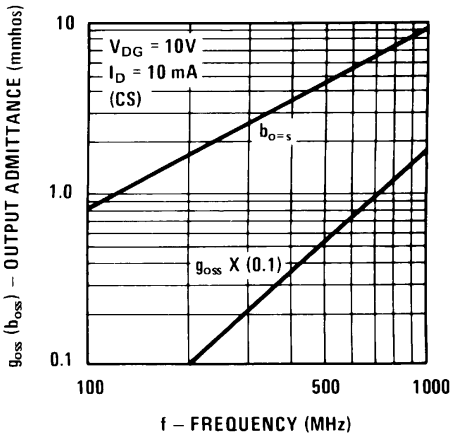


Figure 12. Output Admittance

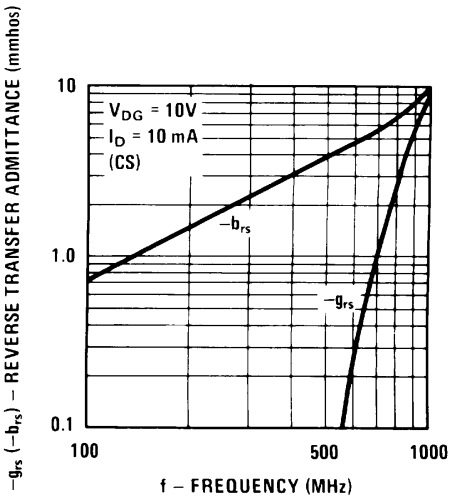


Figure 13. Reverse Transadmittance

COMMON GATE CHARACTERISTICS

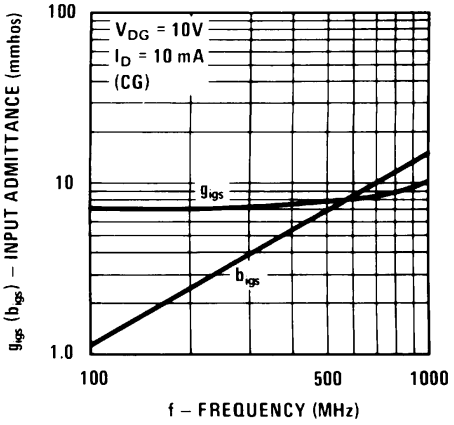


Figure 14. Input Admittance

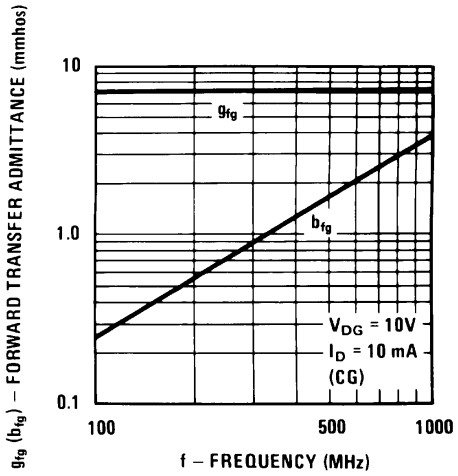


Figure 15. Forward Transadmittance

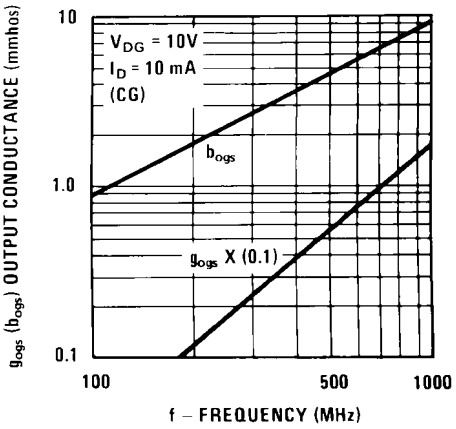


Figure 16. Output Admittance

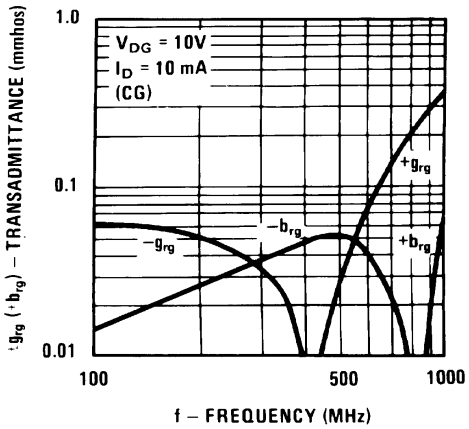


Figure 17. Reverse Transadmittance

ORDERING INFORMATION

Part Number	Top Mark	Package	Packing Method†
J211−D74Z	J211	TO−92 3L (Pb−Free)	Ammo
MMBFJ211	62W	SOT−23 3L (Pb−Free)	Tape and Reel

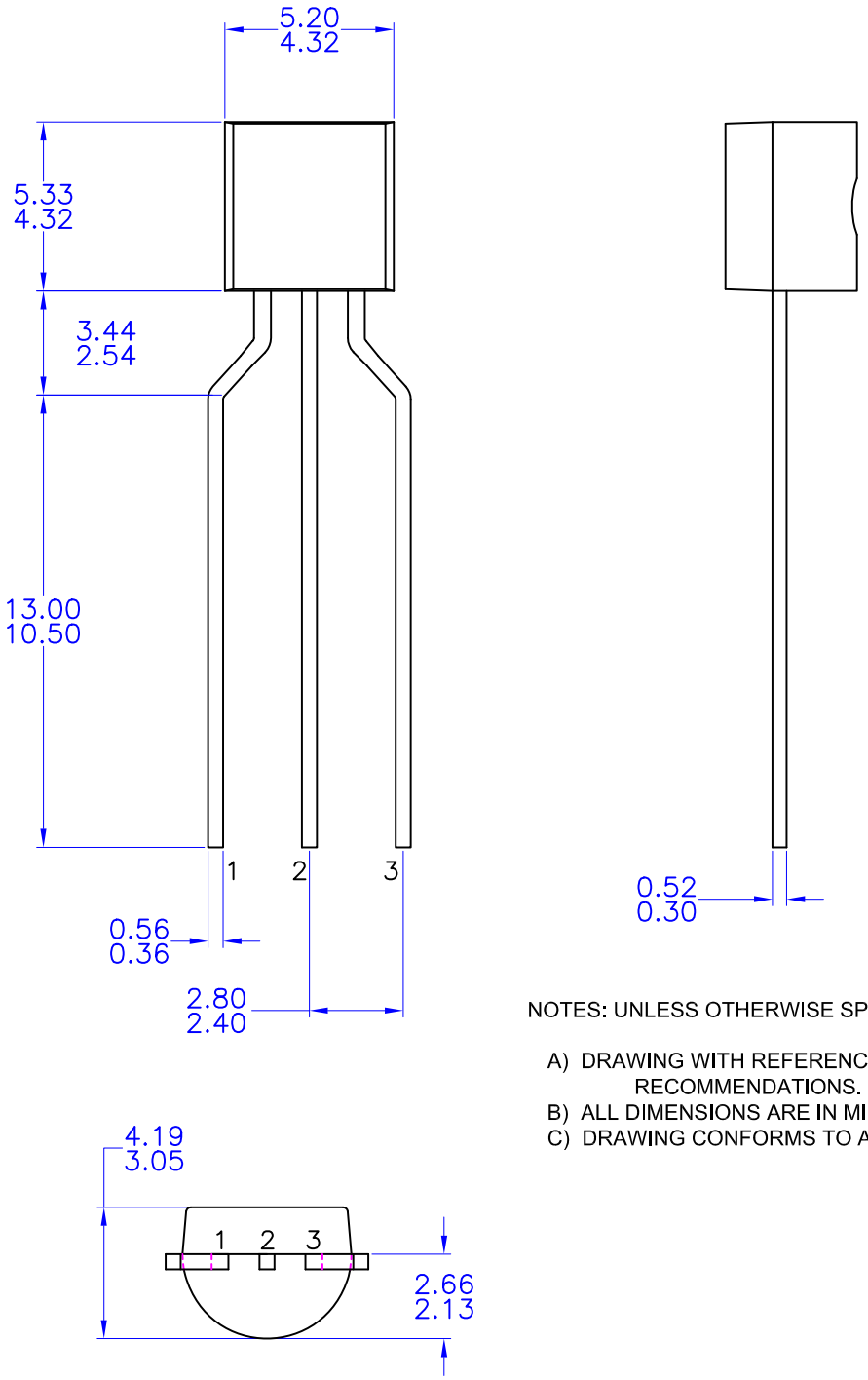
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

TO−92 3 4.83x4.76 LEADFORMED
CASE 135AR
ISSUE O

DATE 30 SEP 2016

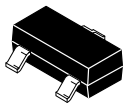


NOTES: UNLESS OTHERWISE SPECIFIED

A) DRAWING WITH REFERENCE TO JEDEC TO-92 RECOMMENDATIONS.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DRAWING CONFORMS TO ASME Y14.5M-1994

DOCUMENT NUMBER:	**98AON13879G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**TO−92 3 4.83X4.76 LEADFORMED**		**PAGE 1 OF 1**

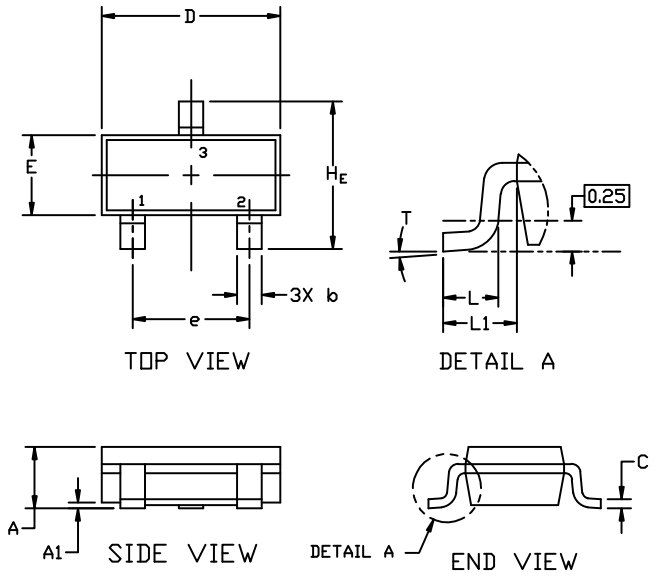
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



SCALE 4:1

SOT−23 (TO−236)
CASE 318
ISSUE AT

DATE 01 MAR 2023

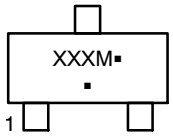


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

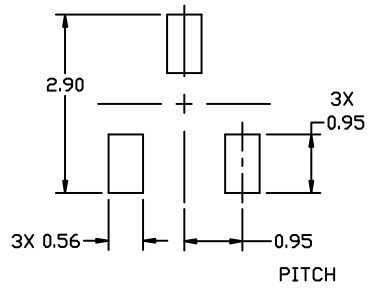
	MILLIMETERS			INCHES		
DIM	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
c	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
H_E	2.10	2.40	2.64	0.083	0.094	0.104
T	0°	---	10°	0°	---	10°

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42226B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**SOT−23 (TO−236)**		**PAGE 1 OF 2**

SOT−23 (TO−236)
CASE 318
ISSUE AT

DATE 01 MAR 2023

STYLE 1 THRU 5:
CANCELLED

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 7:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

STYLE 12:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 13:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 15:
PIN 1. GATE
2. CATHODE
3. ANODE

STYLE 16:
PIN 1. ANODE
2. CATHODE
3. CATHODE

STYLE 17:
PIN 1. NO CONNECTION
2. ANODE
3. CATHODE

STYLE 18:
PIN 1. NO CONNECTION
2. CATHODE
3. ANODE

STYLE 19:
PIN 1. CATHODE
2. ANODE
3. CATHODE−ANODE

STYLE 20:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 22:
PIN 1. RETURN
2. OUTPUT
3. INPUT

STYLE 23:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 24:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 25:
PIN 1. ANODE
2. CATHODE
3. GATE

STYLE 26:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION

STYLE 27:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

STYLE 28:
PIN 1. ANODE
2. ANODE
3. ANODE

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

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