

PNP General-Purpose Amplifier

PZTA56, MMBTA56

General Description

This device is designed for general-purpose amplifier applications at collector currents to 300 mA. Sourced from process 73.

Features

- These are Pb-Free Devices

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted) (Note 1, Note 2)

Symbol	Parameter	Value	Unit
V_{CES}	Collector-Emitter Voltage	-80	V
V_{CBO}	Collector-Base Voltage	-80	V
V_{EBO}	Emitter-Base Voltage	-4.0	V
I_C	Collector Current - Continuous	-500	mA
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to + 150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

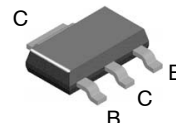
1. These ratings are based on a maximum junction temperature of 150°C .
2. These are steady-state limits. ON Semiconductor should be consulted on applications involving pulsed or low-duty-cycle operations.



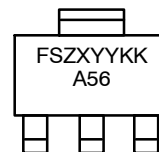
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MARKING DIAGRAM

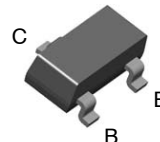


SOT-223-4
CASE 318H

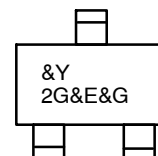


FS = On Semiconductor Logo
Z = Assembly Plant Code
X = Single Digit Numeric Year Code
Last Digit of the Calendar Year
YY = Two Digit Weekly Numeric Code
KK = Two Alphanumeric Character Lot Code
A56 = Device Code

MARKING DIAGRAM



SOT-23-3
CASE 318BM



&Y = ON Semiconductor Logo
2G = Specific Device Code
&E = Designated Space
&G = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping†
PZTA56	SOT-223-4	4000 Tape & Reel
MMBTA56	SO-23-3	3000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

PZTA56, MMBTA56

THERMAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Max		Unit
		PZTA56 (Note 3)	MMBTA56 (Note 4)	
P _D	Total Device Dissipation	1000	350	mW
	Derate Above 25°C	8.0	2.8	mW/°C
R _{θJA}	Thermal Resistance, Junction-to-Ambient	125	357	°C/W

3. PCB size: FR-4, 76 mm x 114 mm x 1.57 mm (3.0 inch x 4.5 inch x 0.062 inch) with minimum land pattern size.

4. Device mounted on FR-4 PCB 36 mm x 18 mm x 1.5 mm; mounting pad for the collector lead minimum 6cm².

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Max	Unit
V _{(BR)CEO}	Collector-Emitter Breakdown Voltage (Note 5)	I _C = -1.0 mA, I _B = 0	-80		V
V _{(BR)CBO}	Collector-Base Breakdown Voltage	I _C = -100 μA, I _E = 0	-60		V
V _{(BR)EBO}	Emitter-Base Breakdown Voltage	I _E = -100 μA, I _C = 0	-4.0		V
I _{CES}	Collector Cut-Off Current	V _{CE} = -60 V, I _B = 0		-0.1	μA
I _{CBO}	Collector Cut-Off Current	V _{CB} = -80 V, I _E = 0		-0.1	μA
h _{FE}	DC Current Gain	I _C = -10 mA, V _{CE} = -1.0 V	100		
		I _C = -100 mA, V _{CE} = -1.0 V	100		
V _{CE(sat)}	Collector-Emitter Saturation Voltage	I _C = -100 mA, I _B = -10 mA		-0.25	V
V _{BE(on)}	Base-Emitter On Voltage	I _C = -100 mA, V _{CE} = -1.0 V		-1.2	V
f _T	Current Gain – Bandwidth Product	I _C = -100 mA, V _{CE} = -1.0 V, f = 100 MHz	50		MHz

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse test: pulse width ≤ 300 μs, duty cycle ≤ 2.0%.

TYPICAL PERFORMANCE CHARACTERISTICS

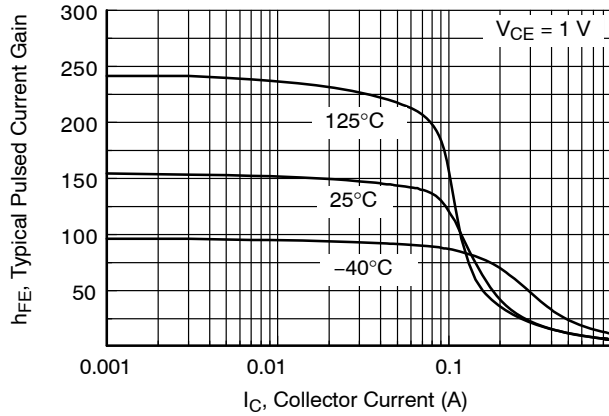


Figure 1. Typical Pulsed Current Gain vs. Collector Current

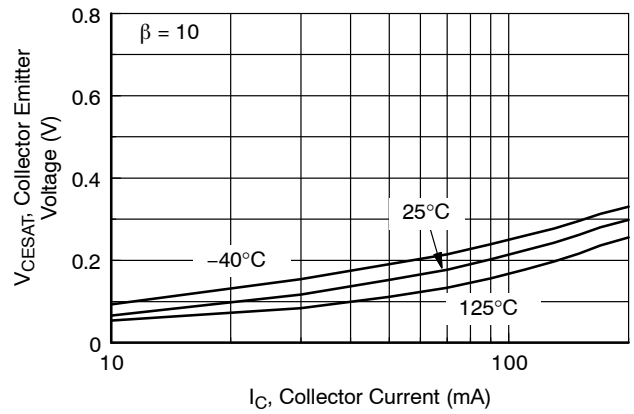


Figure 2. Collector-Emitter Saturation Voltage vs. Collector Current

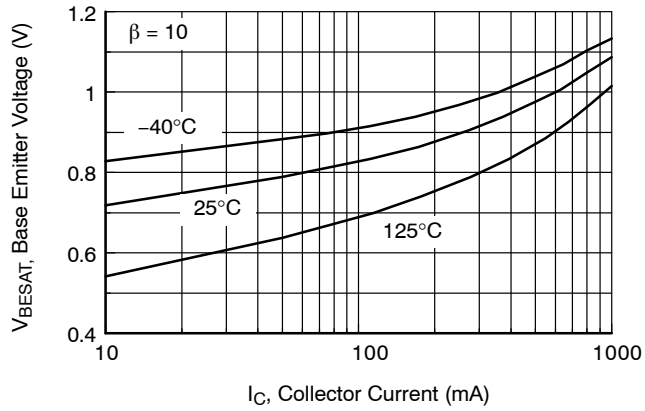


Figure 3. Base-Emitter Saturation Voltage vs. Collector Current

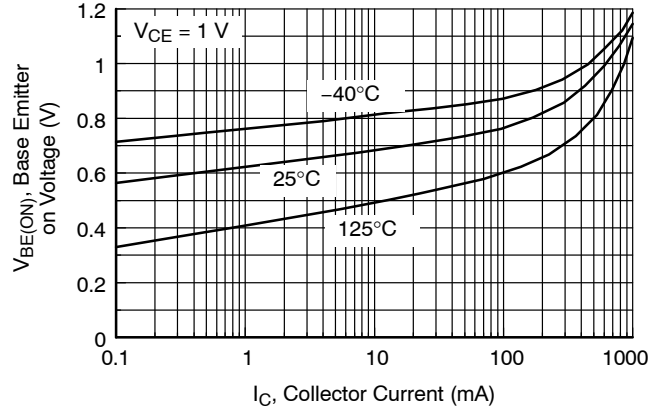


Figure 4. Base-Emitter On Voltage vs. Collector Current

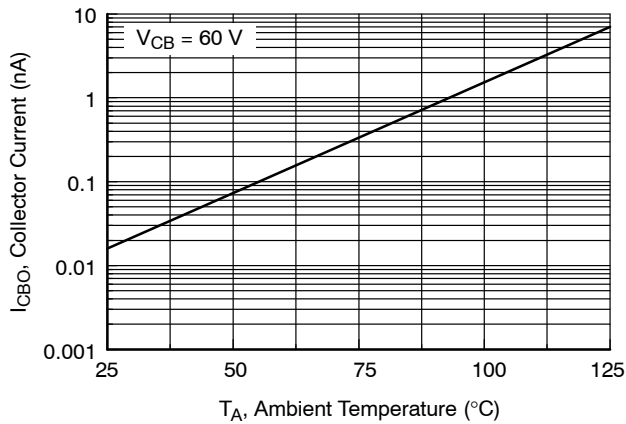


Figure 5. Collector Cut-Off Current vs. Ambient Temperature

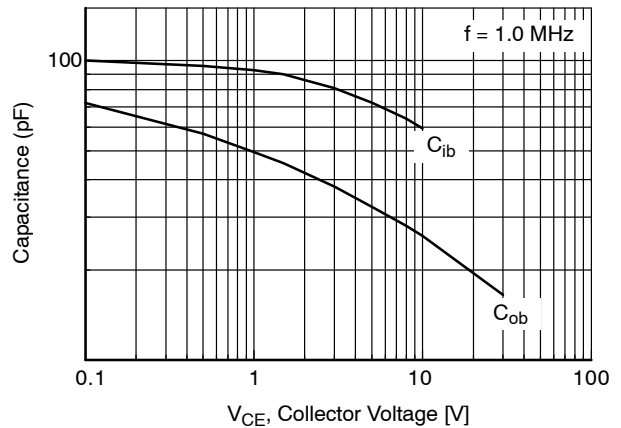


Figure 6. Input and Output Capacitance vs. Reverse Voltage

PZTA56, MMBTA56

TYPICAL CHARACTERISTICS (continued)

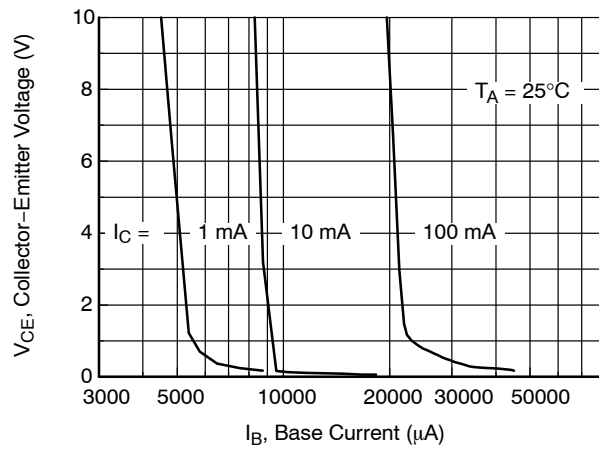


Figure 7. Collector Saturation Region

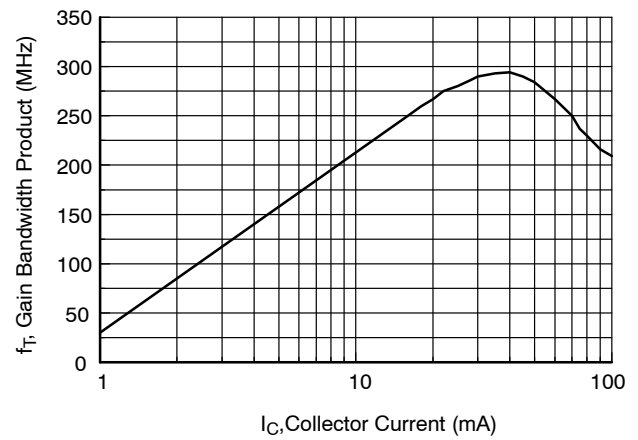


Figure 8. Gain Bandwidth Product vs. Collector Current

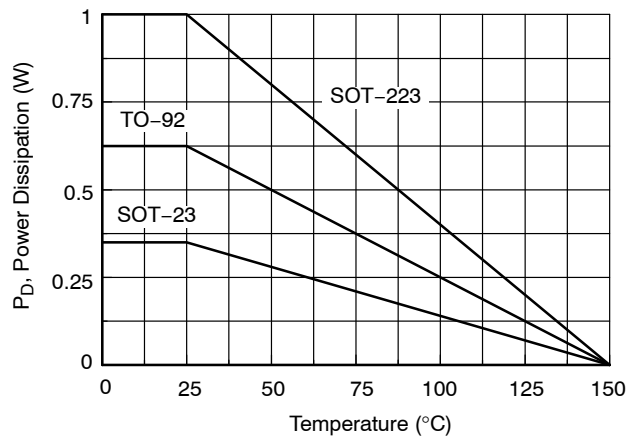


Figure 9. Maximum Safe Operating Area

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

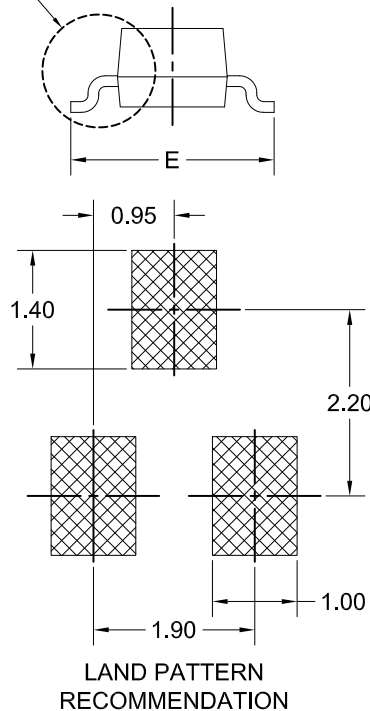
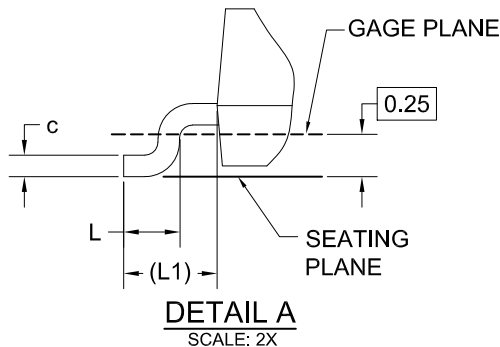
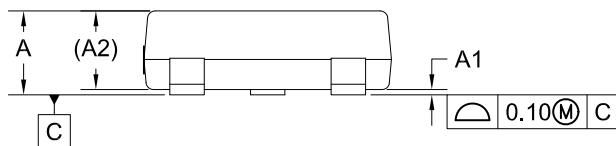
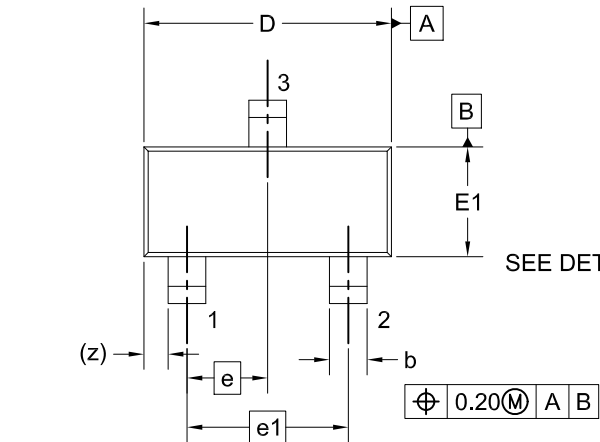


SOT-23 CASE 318BM ISSUE A

DATE 01 SEP 2021

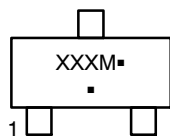
NOTES: UNLESS OTHERWISE SPECIFIED

- A) REFERENCE JEDEC REGISTRATION TO-236, VARIATION AB, ISSUE H.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS ARE INCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 2009.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.20
A1	0.00	0.05	0.10
A2	0.93 REF		
b	0.37	0.44	0.60
c	0.08	0.15	0.23
D	2.72	2.92	3.12
E	2.10	2.40	2.70
E1	1.15	1.30	1.50
e	0.95 BSC		
e1	1.90 BSC		
L	0.20	---	---
L1	0.55 REF		
z	0.29 REF		

GENERIC MARKING DIAGRAM*



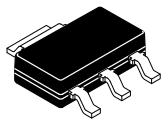
XXX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

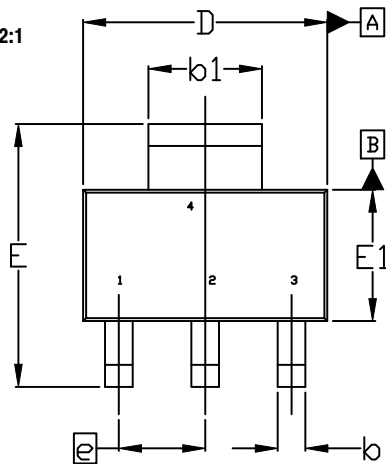
*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

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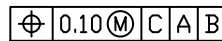
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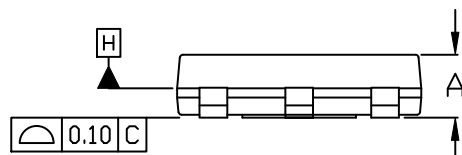
SCALE 2:1



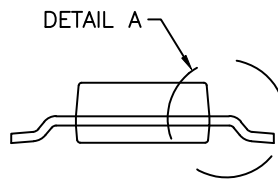
TOP VIEW



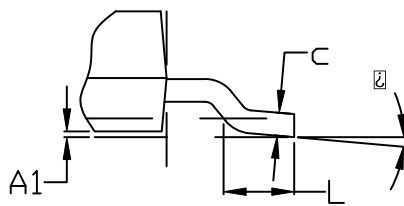
NOTE 7



SIDE VIEW

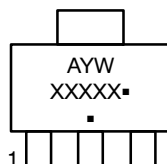


END VIEW



DETAIL A

GENERIC MARKING DIAGRAM*



A = Assembly Location
Y = Year
W = Work Week
XXXXX = Specific Device Code
▪ = Pb-Free Package

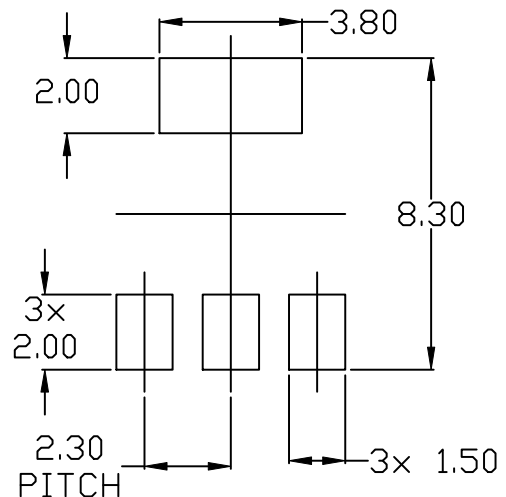
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E1 ARE DETERMINED AT DATUM H. DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. SHALL NOT EXCEED 0.23mm PER SIDE.
4. LEAD DIMENSIONS b AND b1 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS 0.08mm PER SIDE.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.80
A1	0.02	0.06	0.11
b	0.60	0.74	0.88
b1	2.90	3.00	3.10
c	0.24	---	0.35
D	6.30	6.50	6.70
E	6.70	7.00	7.30
E1	3.30	3.50	3.70
e	2.30 BSC		
L	0.25	---	---
⌀	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

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