MOSFET - Power, Single N-Channel, Source-Down TDFN9

60 V, 1.3 mΩ, 243 A

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
60 V	1.3 mΩ @ 10 V	243 A
	2.0 mΩ @ 4.5 V	

NTMFSS1D3N06CL

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- These Devices are Pb−Free, Halogen−Free / BFR Free and are RoHS Compliant

Typical Applications

- DC−DC Converters
- Power Load Switch
- Notebook Battery Management
- Synchronous Rectifier

D (5, 6, 7, 8)

G (9)

S (1, 2, 3, 4)

N−CHANNEL MOSFET

TDFN9 5x6
CASE 520AE

MARKING DIAGRAM
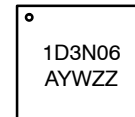
1D3N06
AYWZZ

XXXX = Specific Device Code
A   = Assembly Location
Y   = Year
W   = Work Week
ZZ   = Wafer Lot

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

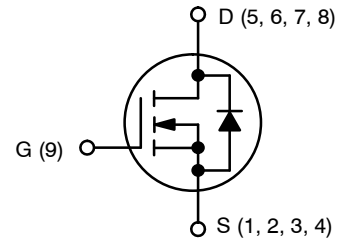| Parameter		Symbol	Value	Unit
Drain−to−Source Voltage		V_{DSS}	60	V
Gate−to−Source Voltage		V_{GS}	±20	V
Continuous Drain Current $R_{\theta JC}$	Steady State $T_C = 25°C$	I_D	243	A
	Steady State $T_C = 100°C$		153	
Power Dissipation $R_{\theta JC}$	Steady State $T_C = 25°C$	P_D	153	W
	Steady State $T_C = 100°C$		61	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	Steady State $T_A = 25°C$	I_D	31	A
	$T_C = 100°C$		19	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)	Steady State $T_A = 25°C$	P_D	2.5	W
	$T_C = 100°C$		1	
Pulsed Drain Current	$T_A = 25°C$, $t_p = 10$ μs	I_{DM}	1758	A
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to +150	°C
Single Pulse Drain−to−Source Avalanche Energy ($I_{L(pk)} = 79$ A)		E_{AS}	234	mJ
Lead Temperature Soldering Reflow for Soldering Purposes (1/8″ from case for 10 s)		T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
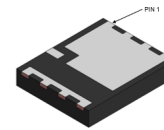
THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Case – Steady State	$R_{\theta JC}$	0.81	°C/W
Junction−to−Ambient – Steady State (Note 2)	$R_{\theta JA}$	50	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface−mounted on FR4 board using a 1 in^2 pad size, 2 oz. Cu pad.

ORDERING INFORMATION

Device	Package	Shipping[†]
NTMFSS1D3N06CL	TDFN9 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NTMFSS1D3N06CL

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		60			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = 250 μA, ref to 25°C			24		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 60 V	T_J = 25°C			10	μA
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 20 V				100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		1.2		2.0	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	I_D = 250 μA, ref to 25°C			−5.9		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 50 A			1.0	1.3	mΩ
		V_{GS} = 4.5 V, I_D = 50 A			1.3	2.0	
Forward Transconductance	g_{FS}	V_{DS} = 15 V, I_D = 50 A			180		S
Gate Resistance	R_G	T_A = 25°C			0.6		Ω
CHARGES & CAPACITANCES							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 30 V			8190		pF
Output Capacitance	C_{OSS}				3950		
Reverse Capacitance	C_{RSS}				25		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 30 V, I_D = 50 A			117		nC
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 30 V, I_D = 50 A			53		
Gate−to−Drain Charge	Q_{GD}				10		
Gate−to−Source Charge	Q_{GS}				22.4		
Plateau Voltage	V_{GP}				2.8		V
SWITCHING CHARACTERISTICS (Note 3)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 4.5 V, V_{DD} = 30 V, I_D = 50 A, R_G = 2.5 Ω			19.6		ns
Rise Time	t_r				9.2		
Turn−Off Delay Time	$t_{d(OFF)}$				55		
Fall Time	t_f				14		
SOURCE−TO−DRAIN DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 50 A	T_J = 25°C		0.79	1.2	V
			T_J = 125°C		0.65		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI/dt = 100 A/μs, I_S = 50 A			84		ns
Charge Time	t_a				43		
Discharge Time	t_b				41		
Reverse Recovery Charge	Q_{RR}				153		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
3. Switching characteristics are independent of operating junction temperatures.

NTMFSS1D3N06CL

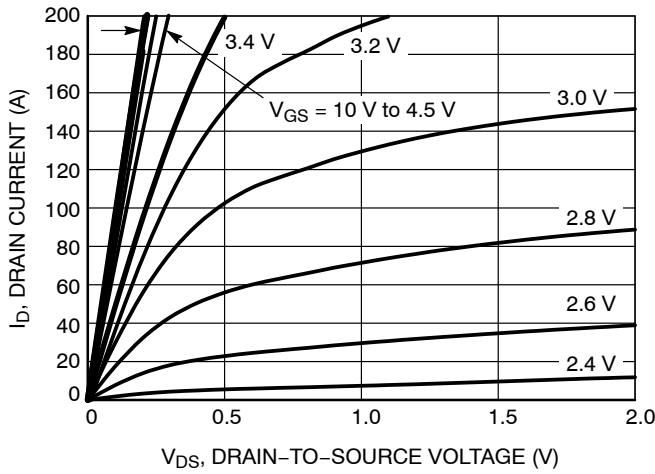## TYPICAL CHARACTERISTICS

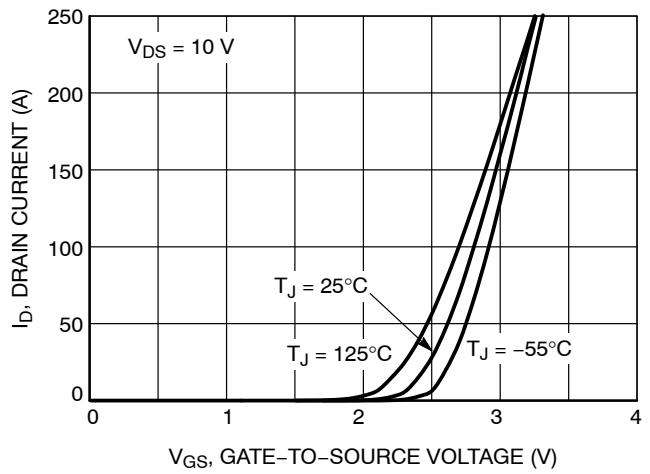Figure 1. On−Region Characteristics
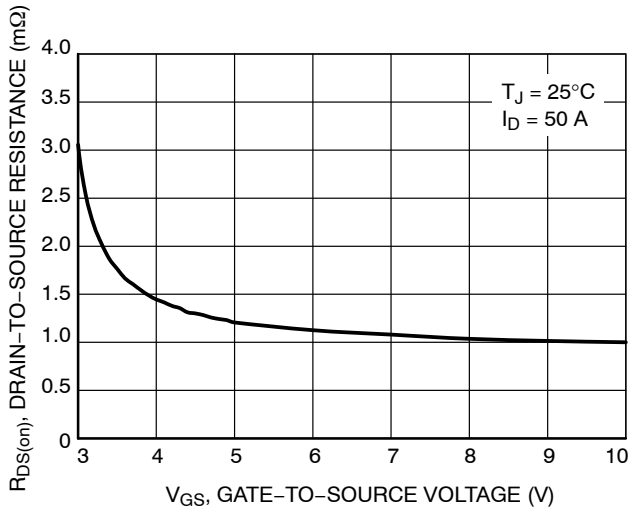

Figure 2. Transfer Characteristics

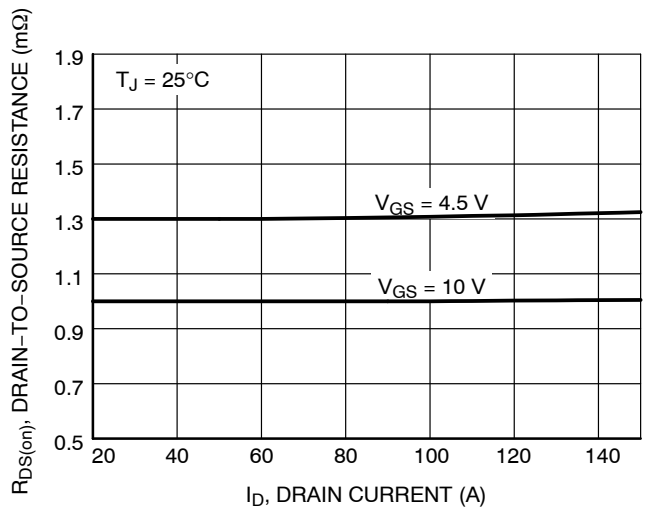Figure 3. On−Resistance vs. Gate−to−Source Voltage

Figure 4. On−Resistance vs. Drain Current and Gate Voltage
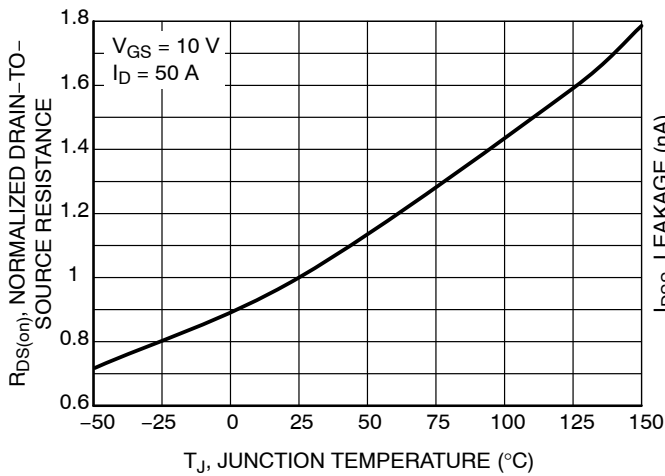

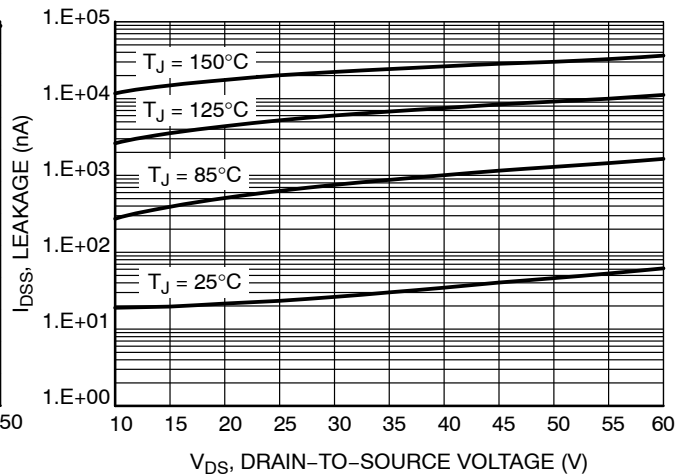Figure 5. On−Resistance Variation with Temperature

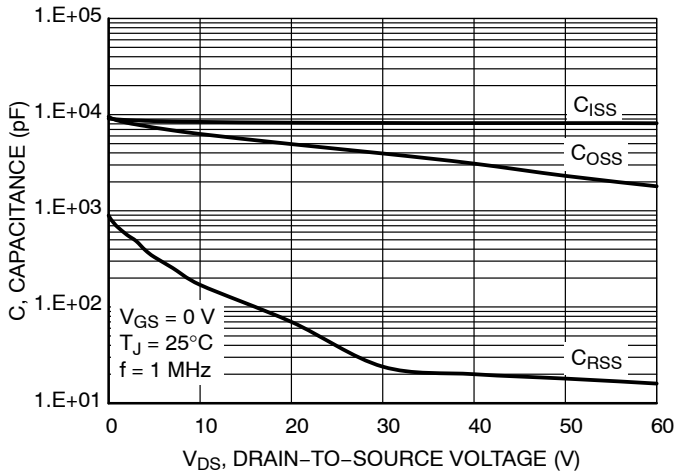Figure 6. Drain−to−Source Leakage Current vs. Voltage

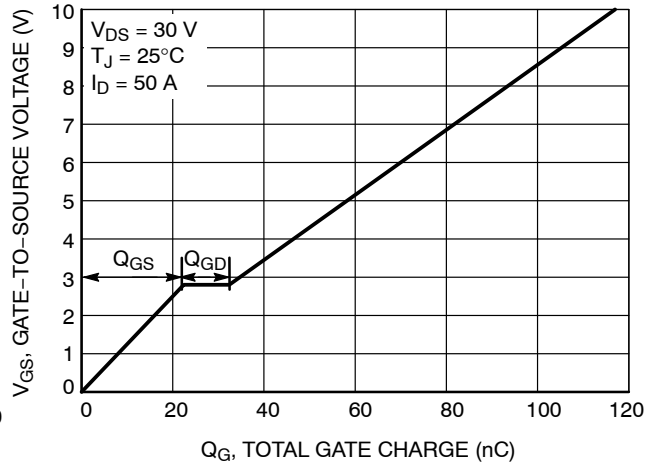## TYPICAL CHARACTERISTICS

Figure 7. Capacitance Variation
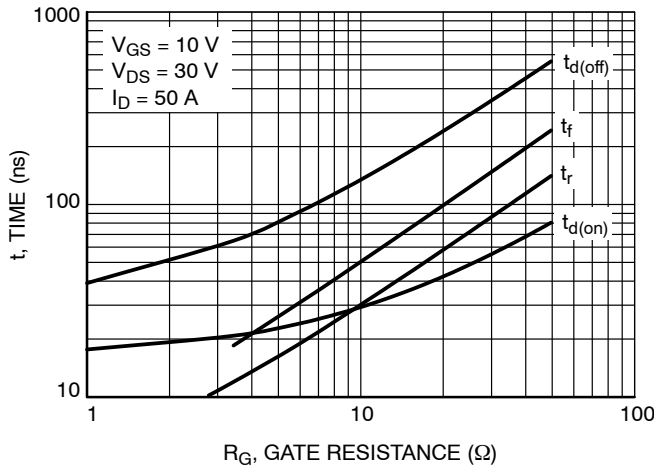

Figure 8. Gate−to−Source vs. Total Charge

Figure 9. Resistive Switching Time Variation vs. Gate Resistance
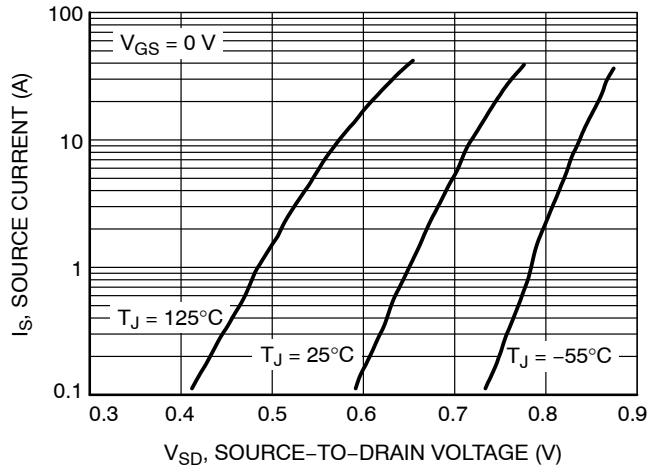
Figure 10. Diode Forward Voltage vs. Current
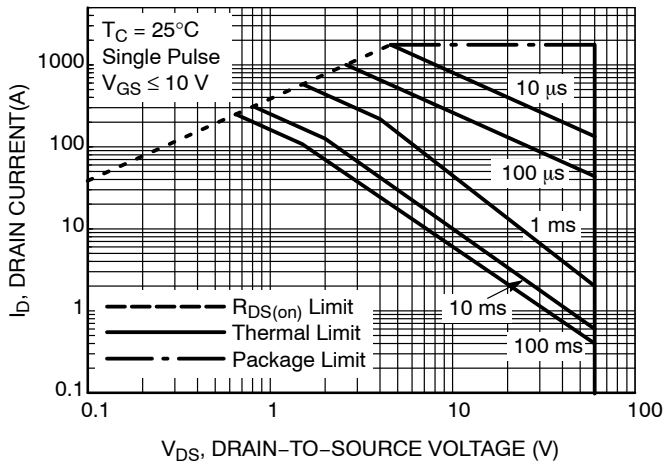
Figure 11. Safe Operating Area
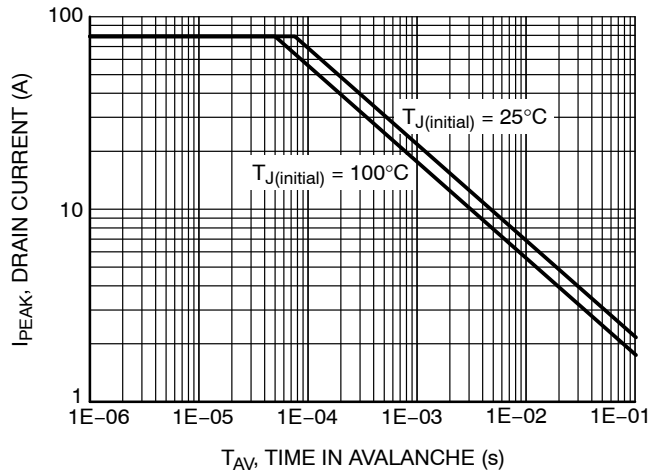
Figure 12. I$_{PEAK}$ vs. Time in Avalanche

NTMFSS1D3N06CL

TYPICAL CHARACTERISTICS
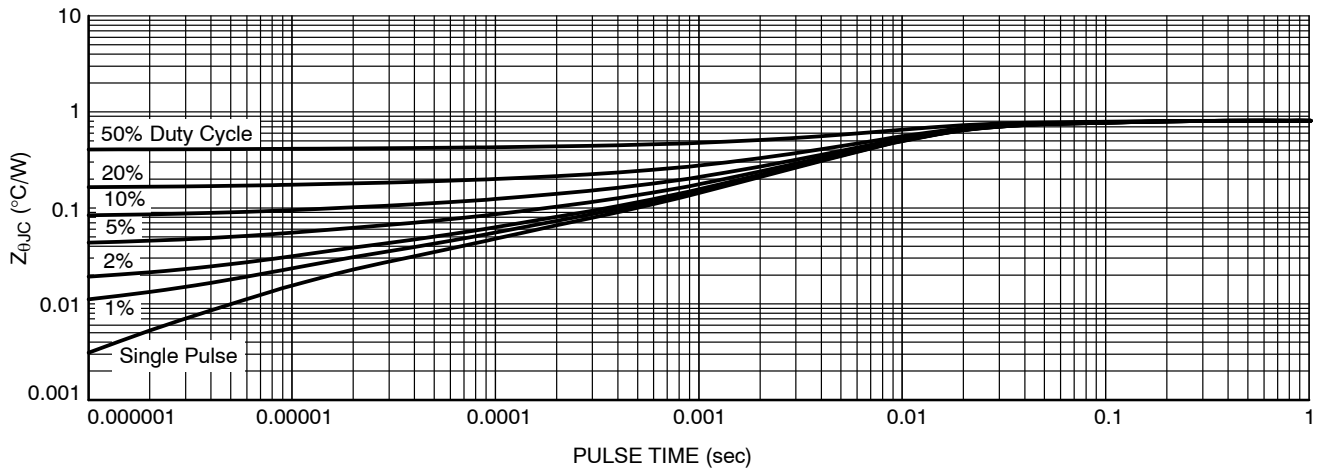
Figure 13. Thermal Characteristics
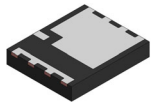
TDFN9 5x6, 1.27P
CASE 520AE
ISSUE B

DATE 24 NOV 2022

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1, D2, E1 AND E2 DO NOT INCLUDE MOLD FLASH.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

TOP VIEW

FRONT VIEW

SEE DETAIL A

DETAIL A
SCALE: 3:1

BOTTOM VIEW

KEEP OUT AREA
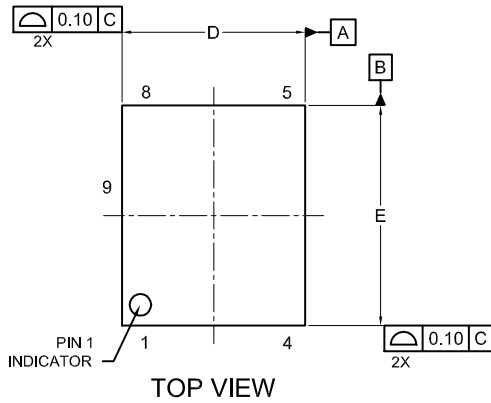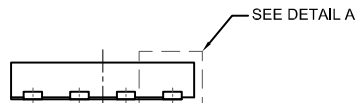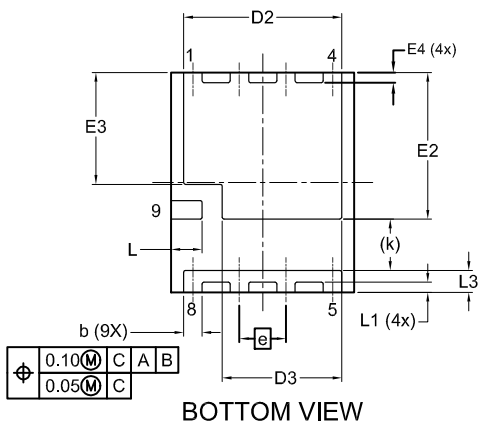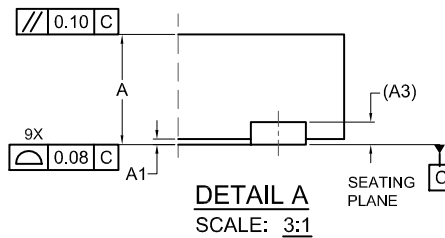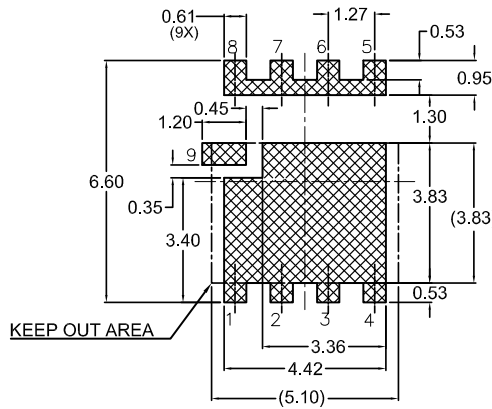
LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.95	1.00	1.05
A1	0.00	0.02	0.05
A3	0.20 REF		
b	0.45	0.50	0.55
D	4.90	5.00	5.10
D2	4.10	4.30	4.50
D3	3.16	3.26	3.36
E	5.90	6.00	6.10
E2	3.90	4.00	4.10
E3	2.95	3.05	3.15
E4	0.18	0.28	0.38
e	1.27 BSC		
k	1.40 REF		
L	0.75	0.85	0.95
L1	0.18	0.28	0.38
L3	0.50	0.60	0.70

GENERIC MARKING DIAGRAM*

XXXXXX
XXXXXX
AWLYWW
°

XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year Code
WW = Work Week Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98AON99041G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	TDFN9 5x6, 1.27P		PAGE 1 OF 1

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT
North American Technical Support:
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

◊