# NTGS3447P

# Power MOSFET

## −12 V, −5.3 A, Single P−Channel, TSOP−6

### Features

- Low $R_{DS(on)}$ in TSOP−6 Package
- 1.8 V Gate Rating
- This is a Pb−Free Device

### Applications

- Battery Switch and Load Management Applications in Portable Equipment
- High Side Load Switch
- PA Switch

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise stated)

| Parameter | | | Symbol | Value | Unit |
|---|---|---|---|---|---|
| Drain−to−Source Voltage | | | $V_{DSS}$ | −12 | V |
| Gate−to−Source Voltage | | | $V_{GS}$ | ±8 | V |
| Continuous Drain Current (Note 1) | Steady State | $T_A$ = 25°C | $I_D$ | −4.7 | A |
| | | $T_A$ = 85°C | | −3.4 | |
| | t ≤ 5 s | $T_A$ = 25°C | | −5.3 | |
| Power Dissipation (Note 1) | Steady State | $T_A$ = 25°C | $P_D$ | 1.25 | W |
| | t ≤ 5 s | | | 1.6 | |
| Continuous Drain Current (Note 2) | Steady State | $T_A$ = 25°C | $I_D$ | −3.4 | A |
| | | $T_A$ = 85°C | | −2.5 | |
| Power Dissipation (Note 2) | | $T_A$ = 25°C | $P_D$ | 0.7 | W |
| Pulsed Drain Current | $t_p$ = 10 μs | | $I_{DM}$ | −19 | A |
| Operating Junction and Storage Temperature | | | $T_J$, $T_{STG}$ | −55 to 150 | °C |
| Lead Temperature for Soldering Purposes (1/8″ from case for 10 s) | | | $T_L$ | 260 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface−mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces)
2. Surface−mounted on FR4 board using the minimum recommended pad size.

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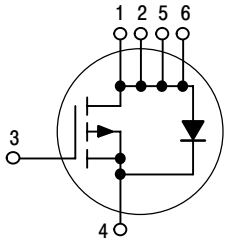
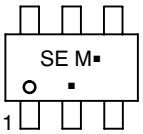
| $V_{(BR)DSS}$ | $R_{DS(on)}$ MAX | $I_D$ MAX |
|---|---|---|
| −12 V | 40 mΩ @ −4.5 V | −4.7 A |
| | 53 mΩ @ −2.5 V | −4.1 A |
| | 72 mΩ @ −1.8 V | −2.0 A |

**P−Channel**



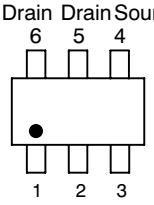

**MARKING DIAGRAM**


**TSOP−6**
**CASE 318G**
**STYLE 1**




SE = Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| NTGS3447PT1G | TSOP−6 (Pb−Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## THERMAL RESISTANCE MAXIMUM RATINGS

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Junction−to−Ambient − Steady State (Note 3) | $R_{\theta JA}$ | 100 | °C/W |
| Junction−to−Ambient − t ≤ 5 s (Note 3) | $R_{\theta JA}$ | 78 | |
| Junction−to−Ambient − Minimum Pad (Note 4) | $R_{\theta JA}$ | 188 | |

3. Surface−mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces)
4. Surface−mounted on FR4 board using the minimum recommended pad size (Cu area = 0.0775 in sq).

## ELECTRICAL CHARACTERISTICS ($T_J$ = 25°C unless otherwise specified)

| Parameter | Symbol | Test Condition | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | | |
| Drain−to−Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS}$ = 0 V, $I_D$ = −250 μA | | −12 | | | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{GS}$ = 0 V, $V_{DS}$ = −12 V | $T_J$ = 25°C | | | −1.0 | μA |
| | | | $T_J$ = 85°C | | | −5.0 | |
| Gate−to−Source Leakage Current | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = ±8 V | | | | ±0.1 | μA |
| **ON CHARACTERISTICS** (Note 5) | | | | | | | |
| Gate Threshold Voltage | $V_{GS(TH)}$ | $V_{GS}$ = $V_{DS}$, $I_D$ = −250 μA | | −0.45 | | −1.0 | V |
| Drain−to−Source On Resistance | $R_{DS(on)}$ | $V_{GS}$ = −4.5 V, $I_D$ = −4.7 A | | | 30 | 40 | mΩ |
| | | $V_{GS}$ = −2.5 V, $I_D$ = −4.1 A | | | 40 | 53 | |
| | | $V_{GS}$ = −1.8 V, $I_D$ = −2.0 A | | | 53 | 72 | |
| Forward Transconductance | $g_{FS}$ | $V_{DS}$ = −5 V, $I_D$ = −4.7 A | | | 12 | | S |
| **CHARGES, CAPACITANCES AND GATE RESISTANCE** | | | | | | | |
| Input Capacitance | $C_{ISS}$ | $V_{GS}$ = 0 V, f = 1 MHz, $V_{DS}$ = −6 V | | | 1053 | | pF |
| Output Capacitance | $C_{OSS}$ | | | | 254 | | |
| Reverse Transfer Capacitance | $C_{RSS}$ | | | | 129 | | |
| Total Gate Charge | $Q_{G(TOT)}$ | $V_{GS}$ = −4.5 V, $V_{DS}$ = −6 V; $I_D$ = −4.7 A | | | 10.4 | 15 | nC |
| Threshold Gate Charge | $Q_{G(TH)}$ | | | | 1.0 | | |
| Gate−to−Source Charge | $Q_{GS}$ | | | | 1.7 | | |
| Gate−to−Drain Charge | $Q_{GD}$ | | | | 0.4 | | |
| **SWITCHING CHARACTERISTICS**, $V_{GS}$ = 4.5 V (Note 6) | | | | | | | |
| Turn−On Delay Time | $t_{d(ON)}$ | $V_{GS}$ = −4.5 V, $V_{DS}$ = −6 V, $I_D$ = −1.0 A, $R_G$ = 6.0 Ω | | | 7 | 11 | ns |
| Rise Time | $t_r$ | | | | 14 | 22 | |
| Turn−Off Delay Time | $t_{d(OFF)}$ | | | | 78 | 117 | |
| Fall Time | $t_f$ | | | | 47 | 71 | |
| **DRAIN−SOURCE DIODE CHARACTERISTICS** | | | | | | | |
| Forward Diode Voltage | $V_{SD}$ | $V_{GS}$ = 0 V, $I_S$ = −1.7 A | $T_J$ = 25°C | | −0.7 | −1.2 | V |
| Reverse Recovery Time | $t_{RR}$ | $V_{GS}$ = 0 V, $dI_{SD}/d_t$ = 100 A/μs, $I_S$ = −1.7 A | | | 33 | 66 | ns |

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%
6. Switching characteristics are independent of operating junction temperatures

## TYPICAL PERFORMANCE CURVES ($T_J$ = 25°C unless otherwise noted)

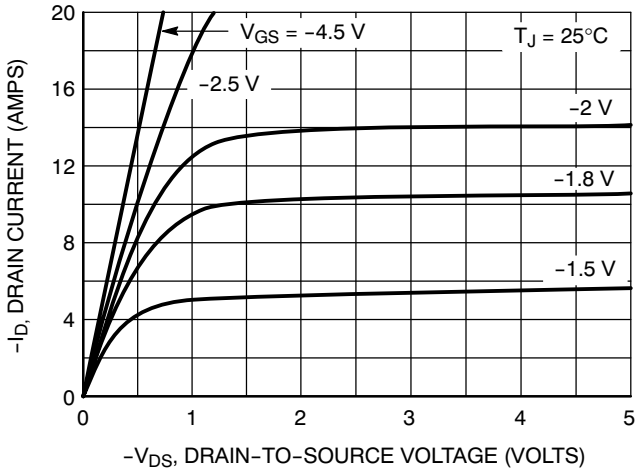



**Figure 1. On−Region Characteristics**

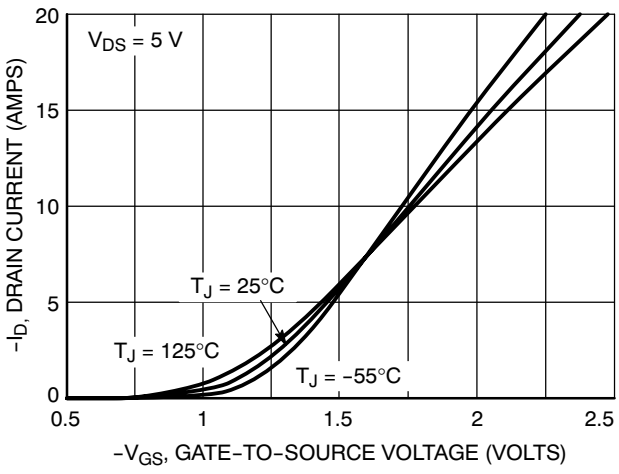



**Figure 2. Transfer Characteristics**

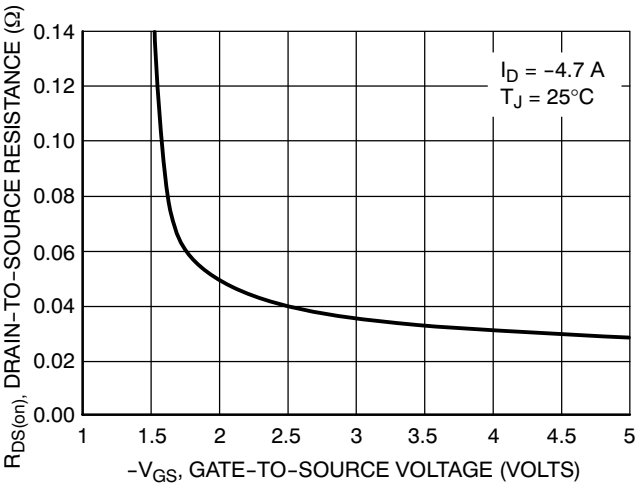



**Figure 3. On−Resistance vs. Gate−to−Source Voltage**

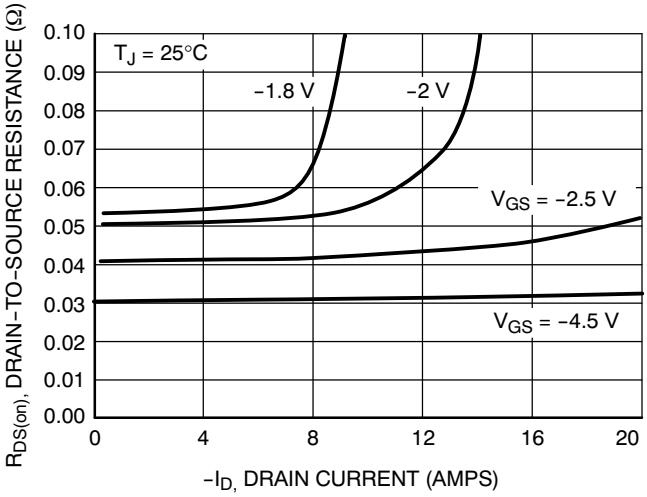



**Figure 4. On−Resistance vs. Drain Current and Gate Voltage**

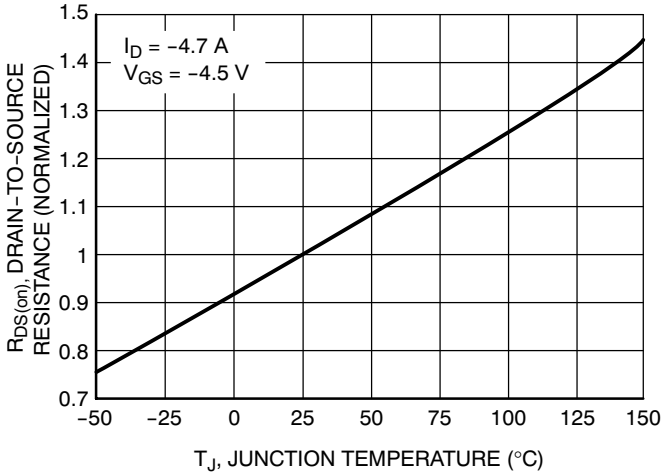



**Figure 5. On−Resistance Variation with Temperature**

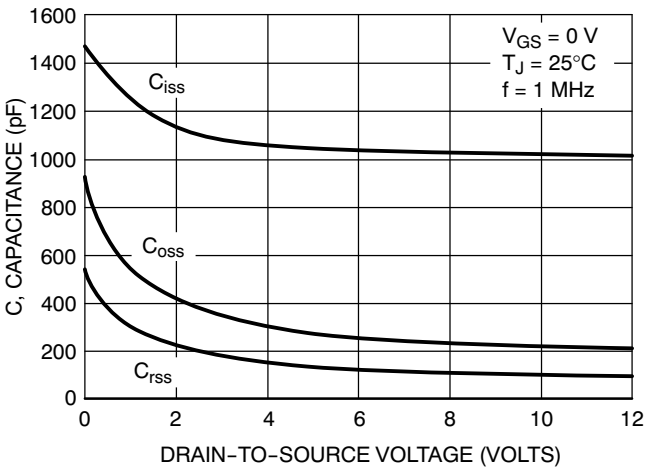



**Figure 6. Capacitance Variation**

## TYPICAL PERFORMANCE CURVES ($T_J$ = 25°C unless otherwise noted)

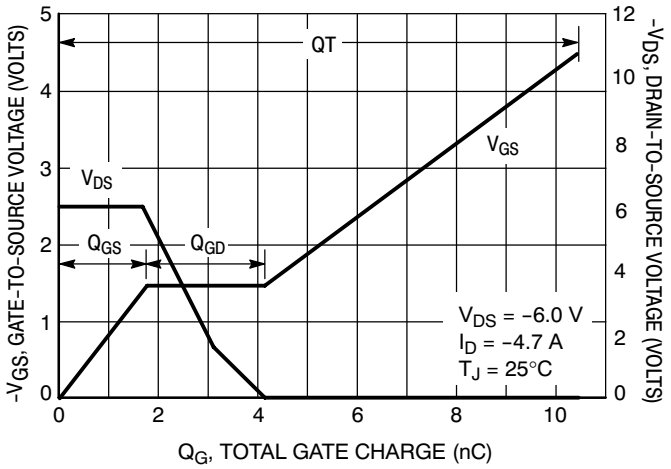



**Figure 7. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge**

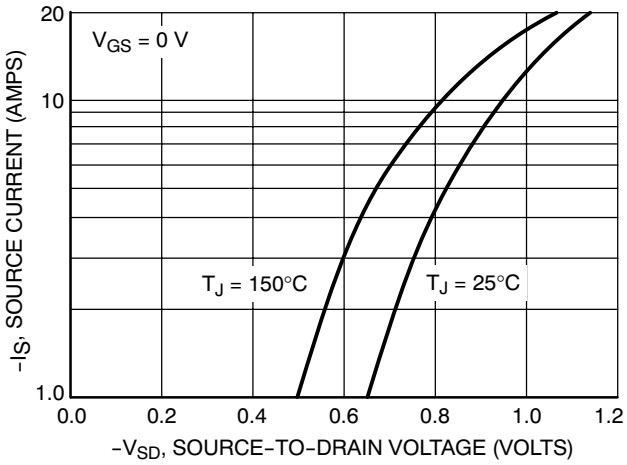



**Figure 8. Diode Forward Voltage vs. Current**

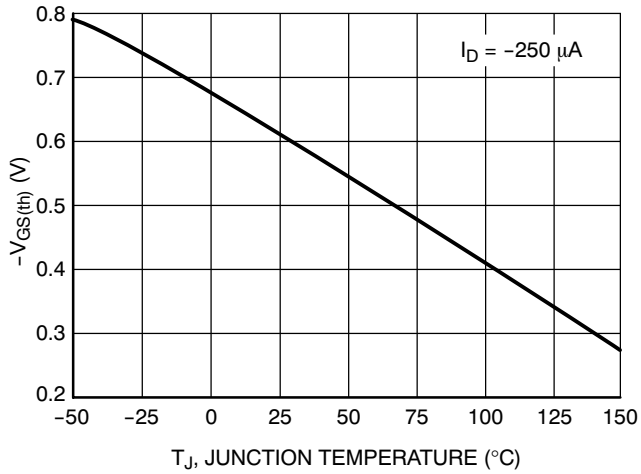



**Figure 9. Threshold Voltage**

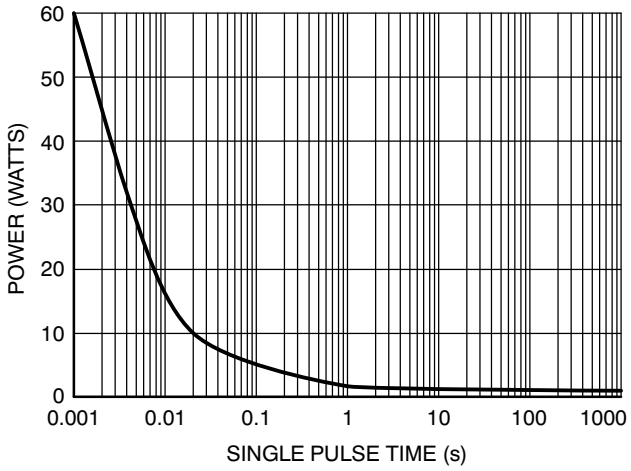



**Figure 10. Single Pulse Maximum Power Dissipation**

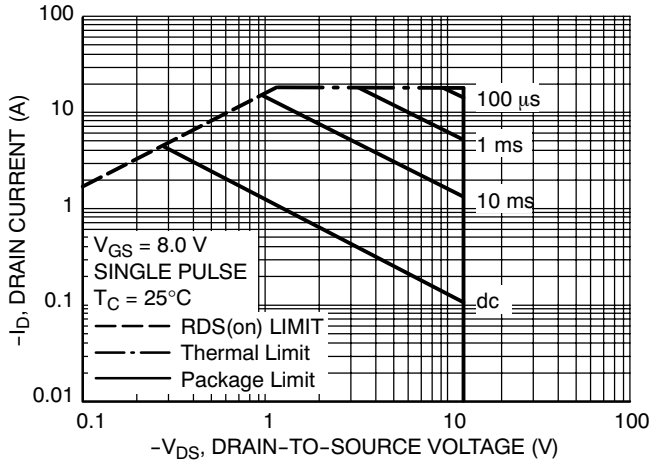



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

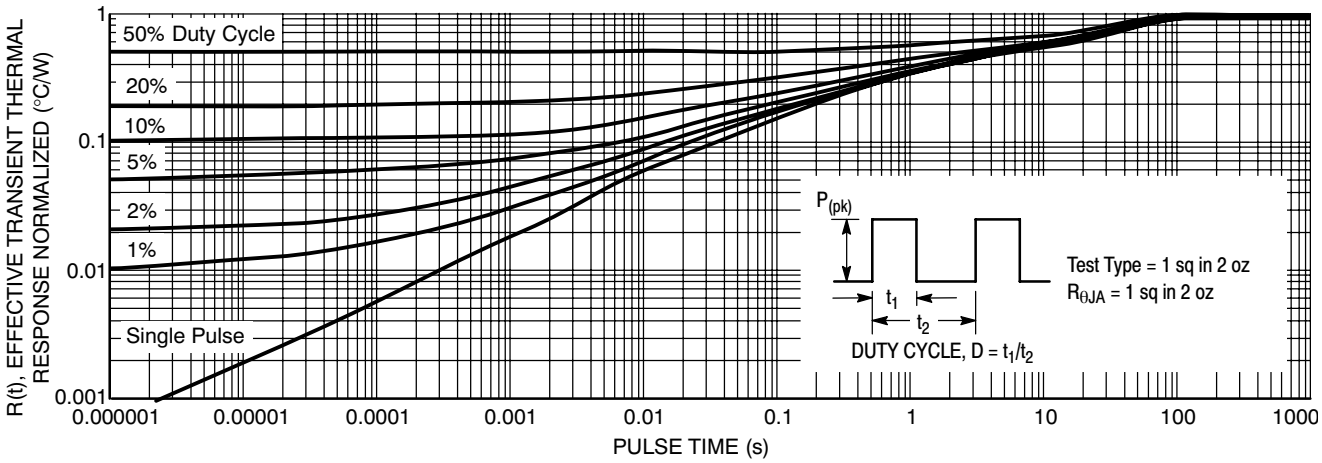



**Figure 12. FET Thermal Response**

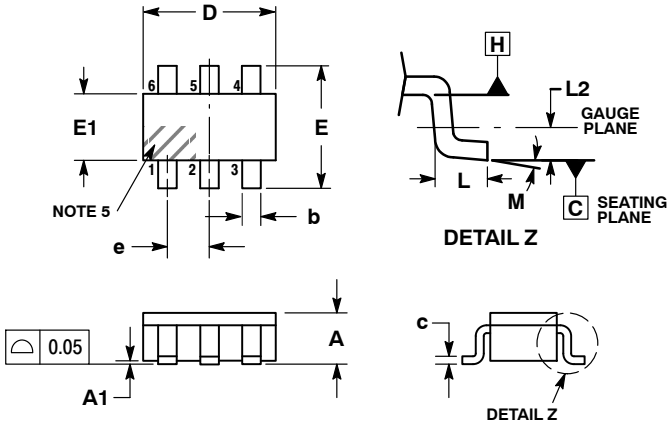
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

1

**SCALE 2:1**

**TSOP−6**
CASE 318G−02
ISSUE V

DATE 12 JUN 2012




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

| | MILLIMETERS | | |
|---|---|---|---|
| **DIM** | **MIN** | **NOM** | **MAX** |
| **A** | 0.90 | 1.00 | 1.10 |
| **A1** | 0.01 | 0.06 | 0.10 |
| **b** | 0.25 | 0.38 | 0.50 |
| **c** | 0.10 | 0.18 | 0.26 |
| **D** | 2.90 | 3.00 | 3.10 |
| **E** | 2.50 | 2.75 | 3.00 |
| **E1** | 1.30 | 1.50 | 1.70 |
| **e** | 0.85 | 0.95 | 1.05 |
| **L** | 0.20 | 0.40 | 0.60 |
| **L2** | 0.25 BSC | | |
| **M** | 0° | – | 10° |

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 2:
PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. BASE 2
6. COLLECTOR 2

STYLE 3:
PIN 1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out

STYLE 4:
PIN 1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD

STYLE 5:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 6:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 7:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. N/C
5. COLLECTOR
6. EMITTER

STYLE 8:
PIN 1. Vbus
2. D(in)
3. D(in)+
4. D(out)+
5. D(out)
6. GND

STYLE 9:
PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE

STYLE 10:
PIN 1. D(OUT)+
2. GND
3. D(OUT)−
4. D(IN)−
5. VBUS
6. D(IN)+

STYLE 11:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1/GATE 2

STYLE 12:
PIN 1. I/O
2. GROUND
3. I/O
4. I/O
5. VCC
6. I/O

STYLE 13:
PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1

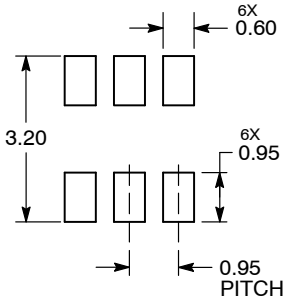
STYLE 14:
PIN 1. ANODE
2. SOURCE
3. GATE
4. CATHODE/DRAIN
5. CATHODE/DRAIN
6. CATHODE/DRAIN

STYLE 15:
PIN 1. ANODE
2. SOURCE
3. GATE
4. DRAIN
5. N/C
6. CATHODE

STYLE 16:
PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE

STYLE 17:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR

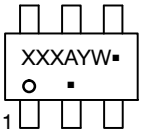
### RECOMMENDED SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

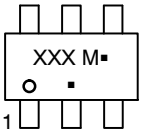
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM*




**IC**

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package




**STANDARD**

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

| | | |
|---|---|---|
| **DOCUMENT NUMBER:** | **98ASB14888C** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red. |
| **DESCRIPTION:** | **TSOP−6** | **PAGE 1 OF 1** |

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For additional information, please contact your local Sales Representative

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