

# Silicon Carbide (SiC) MOSFET – EliteSiC, 40 mohm, 1200 V, M3S, D2PAK-7L

## NTBG040N120M3S

### Features

- Typ.  $R_{DS(on)}$  = 40 m $\Omega$  @  $V_{GS}$  = 18 V
- Ultra Low Gate Charge ( $Q_{G(TOT)}$  = 75 nC)
- High Speed Switching with Low Capacitance ( $C_{OSS}$  = 80 pF)
- 100% Avalanche Tested
- This Device is Halide Free and RoHS Compliant with Exemption 7a, Pb-Free 2LI (on Second Level Interconnection)

### Typical Applications

- Solar Inverters
- Electric Vehicle Charging Stations
- Uninterruptible Power Supplies (UPS)
- Energy Storage Systems
- Switch Mode Power Supplies (SMPS)

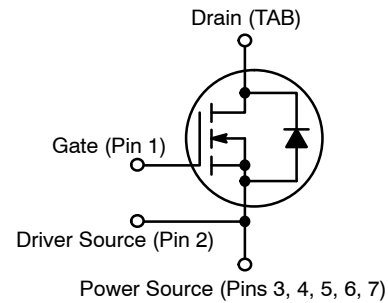
### MAXIMUM RATINGS ( $T_J$ = 25°C unless otherwise noted)

Parameter	Symbol	Value	Unit		
Drain-to-Source Voltage	$V_{DSS}$	1200	V		
Gate-to-Source Voltage	$V_{GS}$	-10/+22	V		
Recommended Operation Values of Gate-to-Source Voltage	$T_C < 175^\circ\text{C}$	$V_{GSop}$	-3/+18 V		
Continuous Drain Current (Notes 2, 3)	Steady State	$T_C = 25^\circ\text{C}$	$I_D$	57	A
			$P_D$	263	W
Power Dissipation (Note 2)	Steady State	$T_C = 100^\circ\text{C}$	$I_D$	40	A
			$P_D$	131	W
Pulsed Drain Current (Note 4)	$T_C = 25^\circ\text{C}$	$I_{DM}$	149	A	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +175	°C		
Source Current (Body Diode) $T_C = 25^\circ\text{C}, V_{GS} = -3\text{ V}$ (Note 2)	$I_S$	50	A		
Single Pulse Drain-to-Source Avalanche Energy ( $I_{L(pk)} = 16.9\text{ A}, L = 1\text{ mH}$ ) (Note 5)	$E_{AS}$	143	mJ		
Maximum Temperature for Soldering (10 s)	$T_L$	270	°C		

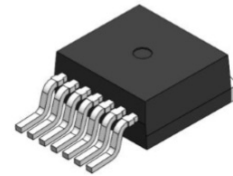
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface mounted on a FR-4 board using 1 in<sup>2</sup> pad of 2 oz copper.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
3. The maximum current rating is based on typical  $R_{DS(on)}$  performance.
4. Repetitive rating, limited by max junction temperature.
5.  $E_{AS}$  of 143 mJ is based on starting  $T_J = 25^\circ\text{C}$ ;  $L = 1\text{ mH}$ ,  $I_{AS} = 16.9\text{ A}$ ,  $V_{DD} = 100\text{ V}$ ,  $V_{GS} = 18\text{ V}$ .

$V_{(BR)DSS}$	$R_{DS(ON)}\text{ MAX}$	$I_D\text{ MAX}$
1200 V	54 m $\Omega$ @ 18 V	57 A

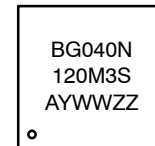


N-CHANNEL MOSFET



D2PAK-7L  
CASE 418BJ

### MARKING DIAGRAM



BG040N120M3S = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
ZZ = Lot Traceability

### ORDERING INFORMATION

Device	Package	Shipping
NTBG040N120M3S	D2PAK-7L	800 / Tape & Reel

# NTBG040N120M3S

## THERMAL CHARACTERISTICS

Parameter	Symbol	Max	Unit
Junction-to-Case – Steady State (Note 2)	$R_{\theta JC}$	0.57	°C/W
Junction-to-Ambient – Steady State (Notes 1, 2)	$R_{\theta JA}$	40	

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF-STATE CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	1200	–	–	V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 1\text{ mA}$ , referenced to $25^\circ\text{C}$ (Note 7)	–	0.3	–	V/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 1200\text{ V}$	–	–	100	$\mu\text{A}$
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{GS} = +22/-10\text{ V}, V_{DS} = 0\text{ V}$	–	–	$\pm 1$	$\mu\text{A}$

### ON-STATE CHARACTERISTICS

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 10\text{ mA}$	2.04	2.9	4.4	V
Recommended Gate Voltage	$V_{GOP}$		–3	–	+18	V
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 18\text{ V}, I_D = 20\text{ A}, T_J = 25^\circ\text{C}$	–	40	54	$\text{m}\Omega$
		$V_{GS} = 18\text{ V}, I_D = 20\text{ A}, T_J = 175^\circ\text{C}$ (Note 7)	–	80	–	
Forward Transconductance	$g_{FS}$	$V_{DS} = 10\text{ V}, I_D = 20\text{ A}$ (Note 7)	–	16	–	S

### CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 800\text{ V}$	–	1700	–	$\text{pF}$
Output Capacitance	$C_{OSS}$		–	80	–	
Reverse Transfer Capacitance	$C_{RSS}$		–	7	–	
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -3/18\text{ V}, V_{DS} = 800\text{ V}, I_D = 20\text{ A}$	–	75	–	$\text{nC}$
Threshold Gate Charge	$Q_{G(TH)}$		–	4.4	–	
Gate-to-Source Charge	$Q_{GS}$		–	14	–	
Gate-to-Drain Charge	$Q_{GD}$		–	22	–	
Gate-Resistance	$R_G$		$f = 1\text{ MHz}$	–	3.8	

### SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = -3/18\text{ V}, V_{DS} = 800\text{ V}, I_D = 20\text{ A}, R_G = 4.7\ \Omega$ Inductive Load (Notes 6, 7)	–	13	–	ns
Rise Time	$t_r$		–	16	–	
Turn-Off Delay Time	$t_{d(OFF)}$		–	38	–	
Fall Time	$t_f$		–	10	–	
Turn-On Switching Loss	$E_{ON}$		–	193	–	$\mu\text{J}$
Turn-Off Switching Loss	$E_{OFF}$		–	66	–	
Total Switching Loss	$E_{tot}$		–	259	–	

### SOURCE-DRAIN DIODE CHARACTERISTICS

Continuous Source-Drain Diode Forward Current (Note 2)	$I_{SD}$	$V_{GS} = -3\text{ V}, T_C = 25^\circ\text{C}$ (Note 7)	–	–	50	A
Pulsed Source-Drain Diode Forward Current (Note 4)	$I_{SDM}$		–	–	149	
Forward Diode Voltage	$V_{SD}$	$V_{GS} = -3\text{ V}, I_{SD} = 20\text{ A}, T_J = 25^\circ\text{C}$	–	4.5	–	V

# NTBG040N120M3S

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified) (continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>SOURCE-DRAIN DIODE CHARACTERISTICS</b>						
Reverse Recovery Time	$t_{RR}$	$V_{GS} = -3/18\text{ V}$ , $I_{SD} = 20\text{ A}$ , $di_S/dt = 1000\text{ A}/\mu\text{s}$ , $V_{DS} = 800\text{ V}$ (Note 7)	-	16.8	-	ns
Reverse Recovery Charge	$Q_{RR}$		-	82	-	nC
Reverse Recovery Energy	$E_{REC}$		-	7.9	-	$\mu\text{J}$
Peak Reverse Recovery Current	$I_{RRM}$		-	9.8	-	A
Charge time	$t_A$		-	9.6	-	ns
Discharge time	$t_B$		-	7.2	-	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6.  $E_{ON}/E_{OFF}$  result is with body diode

7. Defined by design, not subject to production test.

# NTBG040N120M3S

## TYPICAL CHARACTERISTICS

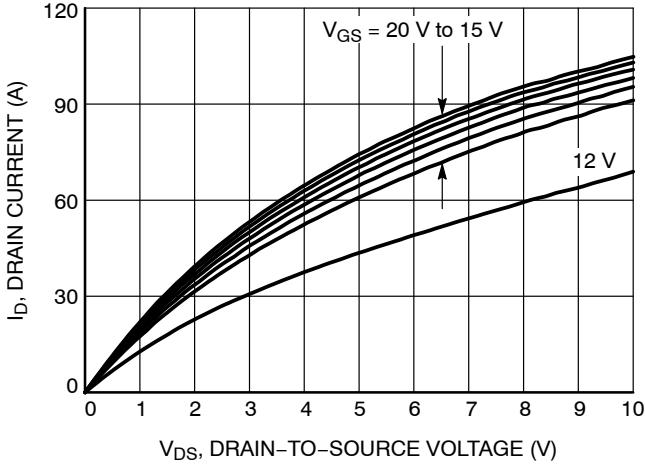


Figure 1. On-Region Characteristics

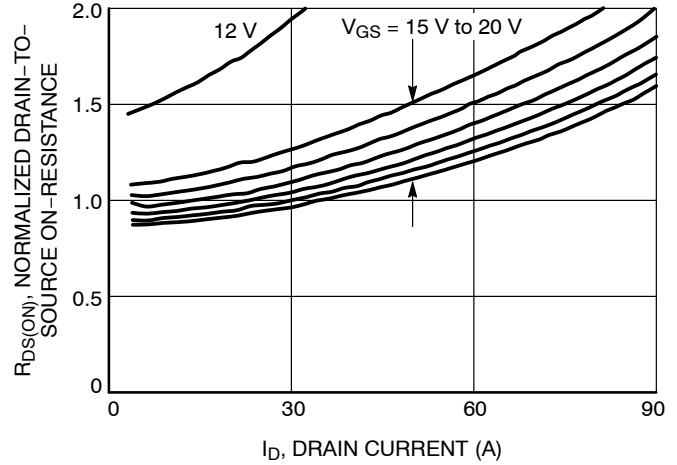


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

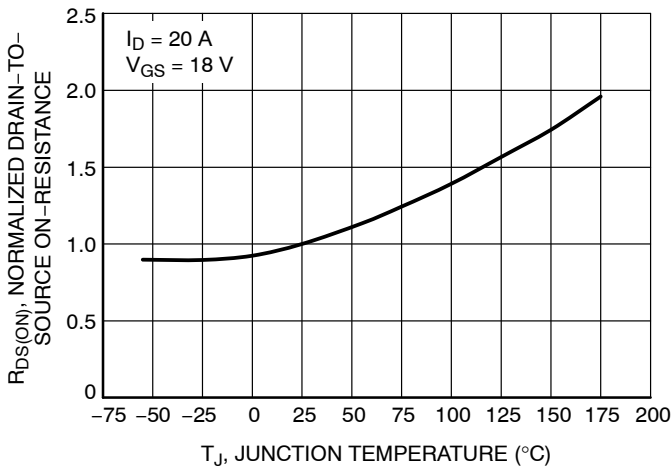


Figure 3. On-Resistance Variation with Temperature

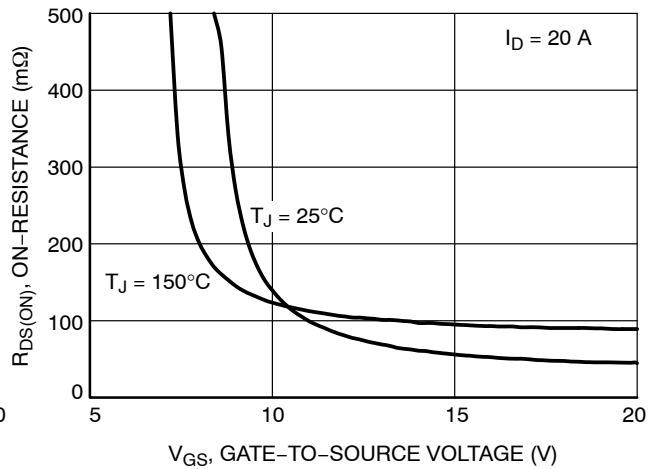


Figure 4. On-Resistance vs. Gate-to-Source Voltage

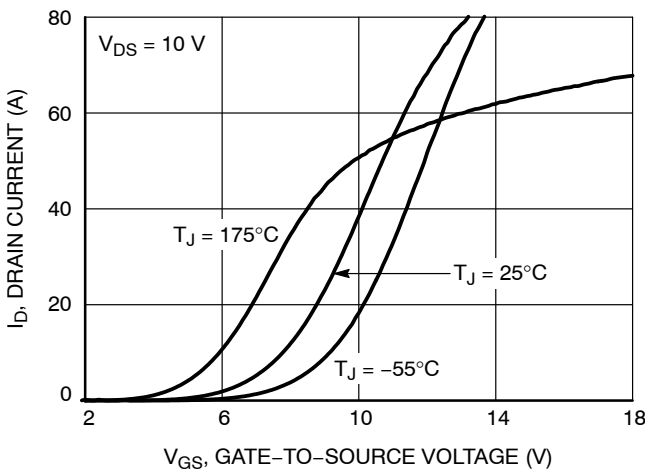


Figure 5. Transfer Characteristics

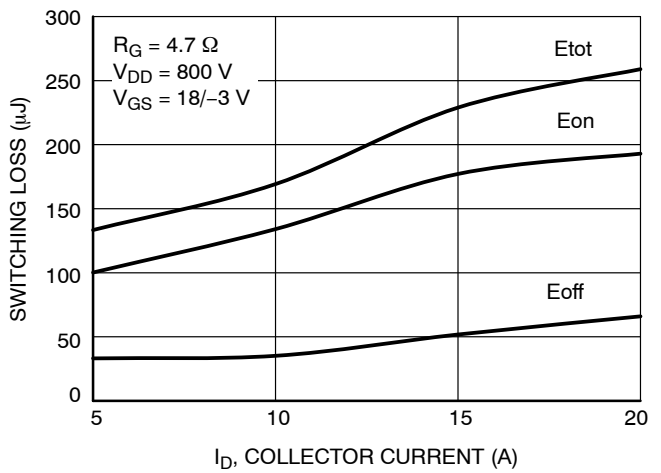


Figure 6. Switching Loss vs. Collector Current

# NTBG040N120M3S

## TYPICAL CHARACTERISTICS

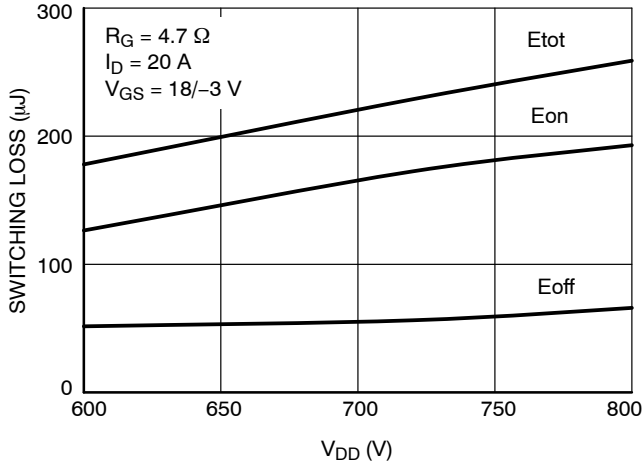


Figure 7. Switching Loss vs. Gate Resistance

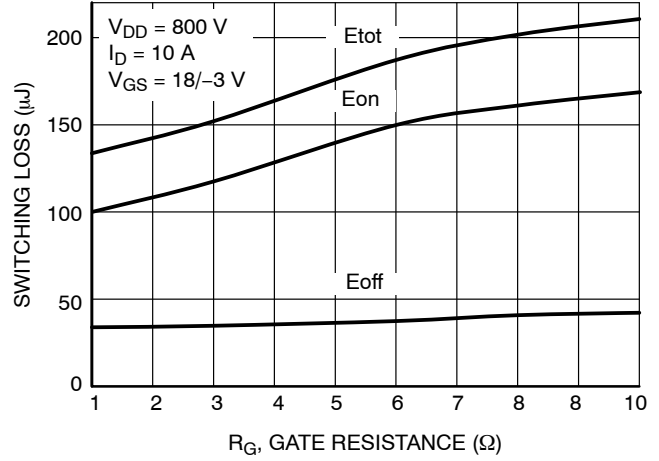


Figure 8. Switching Loss vs. Gate Resistance

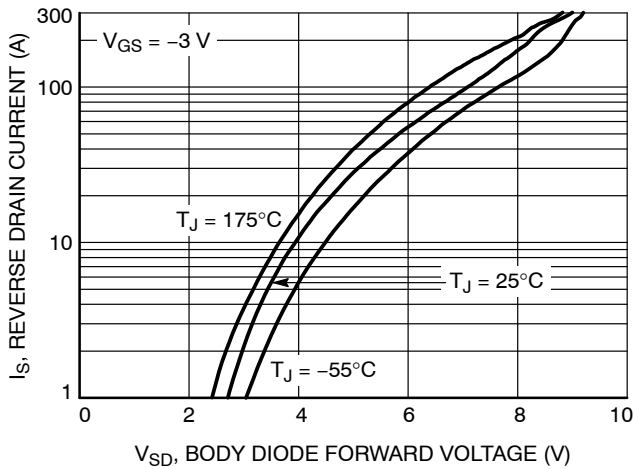


Figure 9. Reverse Drain Current vs. Body Diode Forward Voltage

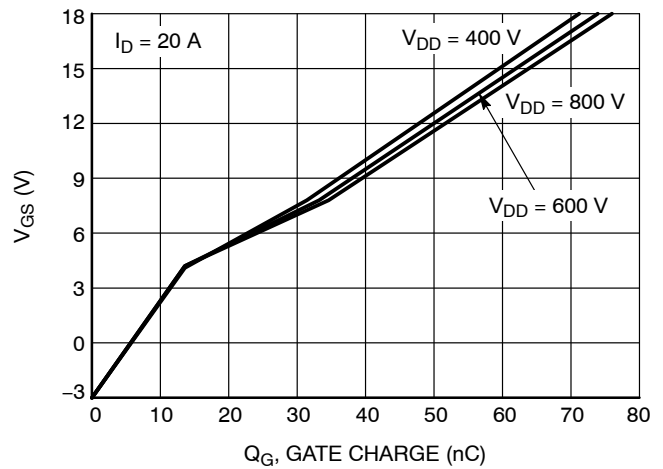


Figure 10. Gate-to-Source Voltage vs. Total Charge

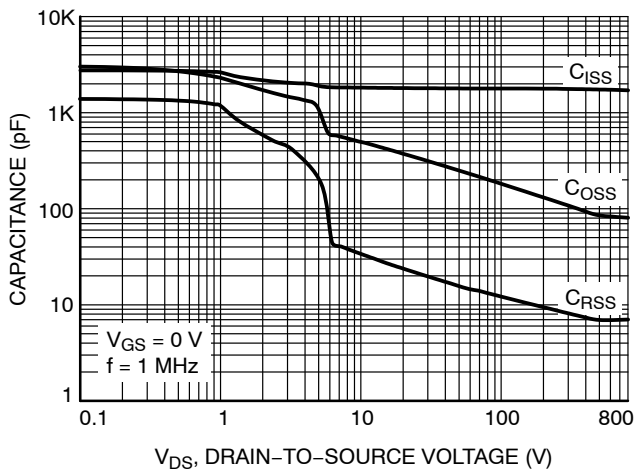


Figure 11. Capacitance vs. Drain-to-Source Voltage

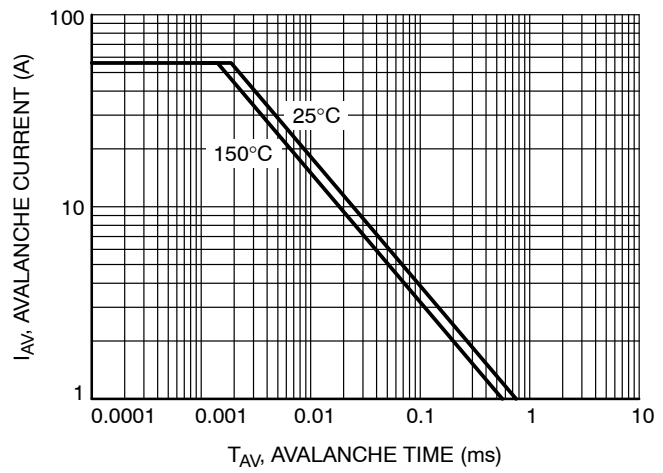
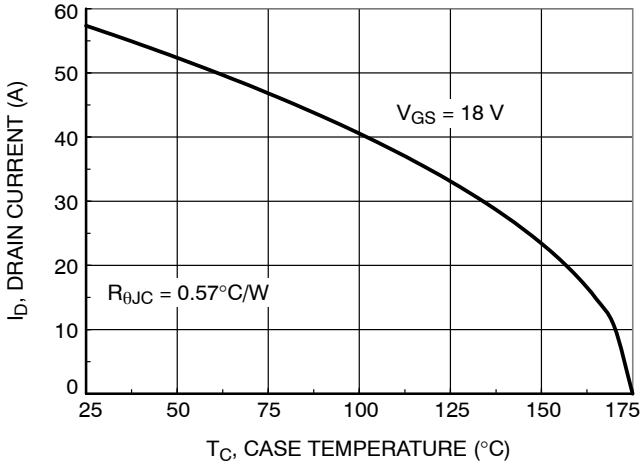


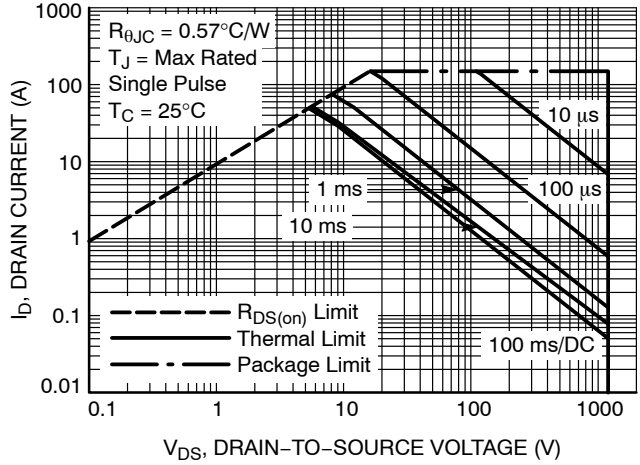
Figure 12. Unclamped Inductive Switching Capability

# NTBG040N120M3S

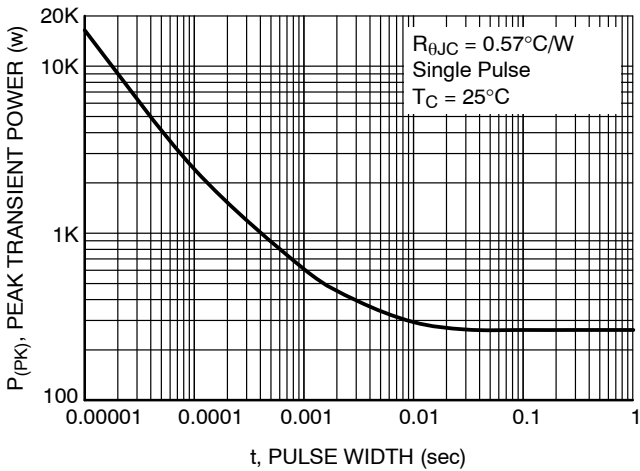
## TYPICAL CHARACTERISTICS



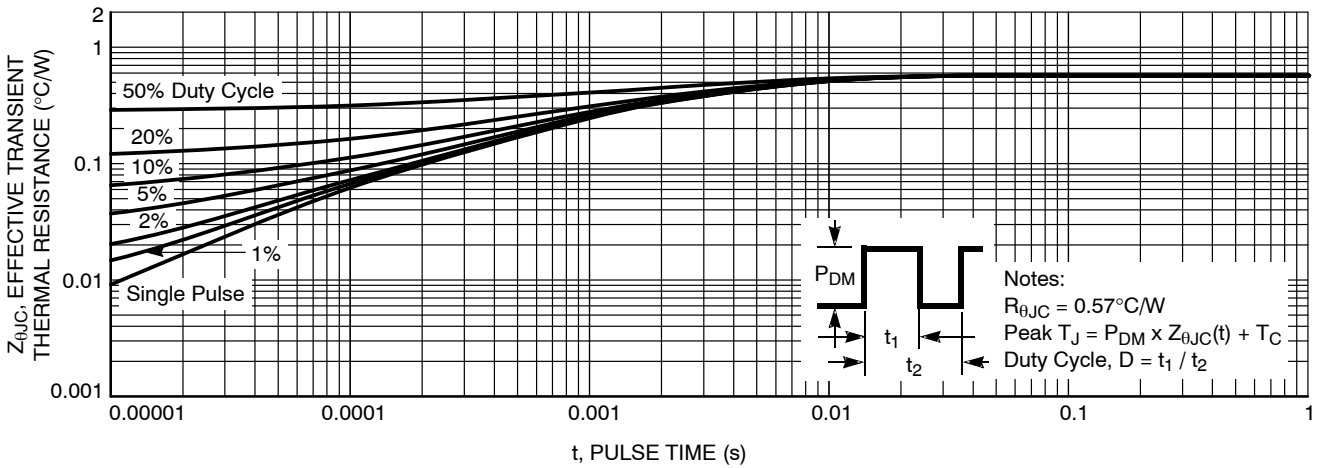
**Figure 13. Maximum Continuous Drain Current vs. Case Temperature**



**Figure 14. Safe Operating Area**



**Figure 15. Single Pulse Maximum Power Dissipation**



**Figure 16. Junction-to-Case Transient Thermal Response**

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



### D<sup>2</sup>PAK7 (TO-263-7L HV) CASE 418BJ ISSUE B

DATE 16 AUG 2019



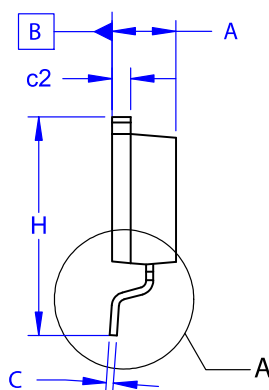
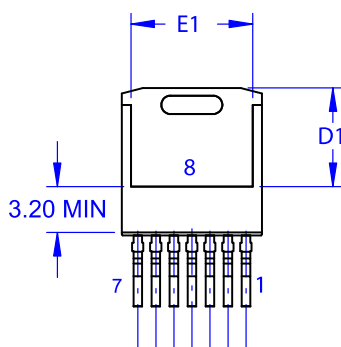
NOTES:

A. PACKAGE CONFORMS TO JEDEC TO-263 VARIATION CB EXCEPT WHERE NOTED.  
B. ALL DIMENSIONS ARE IN MILLIMETERS.

C. OUT OF JEDEC STANDARD VALUE.  
D. DIMENSION AND TOLERANCE AS PER ASME Y14.5-2009.

E. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	0.00	0.10	0.20
b2	0.60	0.70	0.80
b	0.51	0.60	0.70
c	0.40	0.50	0.60
c2	1.20	1.30	1.40
D	9.00	9.20	9.40
D1	6.15	6.80	7.15
E	9.70	9.90	10.20
E1	7.15	7.65	8.15
e	~	1.27	~
H	15.10	15.40	15.70
L	2.44	2.64	2.84
L1	1.00	1.20	1.40
L3	~	0.25	~
aaa	~	~	0.25

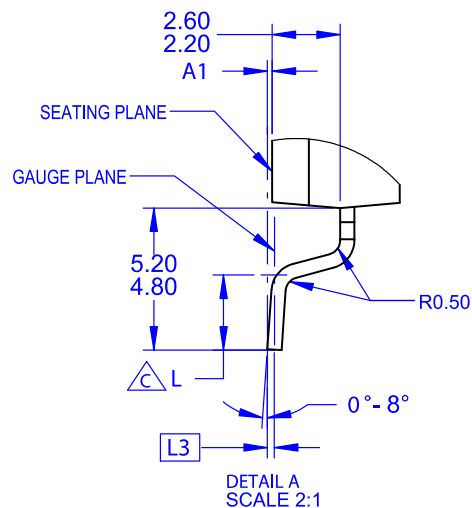


#### GENERIC MARKING DIAGRAM\*



XXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.



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