

# MOSFET – N-Channel, POWERTRENCH®

30 V, 15 A, 5.7 mΩ

## FDMC8854

### General Description

This N-Channel MOSFET is a rugged gate version of onsemi's advanced Power Trench process. It has been optimized for power management applications.

### Features

- Max  $r_{DS(on)}$  = 5.7 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 15\text{ A}$
- Max  $r_{DS(on)}$  = 7.6 mΩ at  $V_{GS} = 4.5\text{ V}$ ,  $I_D = 13\text{ A}$
- Low Profile – 1 mm Max in Power 33
- This Device is Pb-Free, Halide Free and is RoHS Compliant

### Applications

- DC-DC Conversion

### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted.)

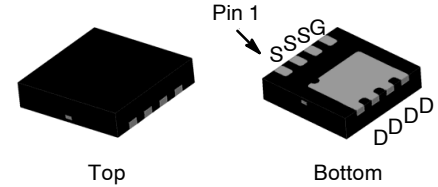
Symbol	Parameter	Value	Unit
$V_{DS}$	Drain to Source Voltage	30	V
$V_{GS}$	Gate to Source Voltage	±20	V
$I_D$	Drain Current		A
	– Continuous $T_C = 25^\circ\text{C}$	15	
	– Continuous (Note 1a) $T_A = 25^\circ\text{C}$	15	
	– Pulsed	100	
$P_D$	Power Dissipation $T_C = 25^\circ\text{C}$	41	W
	Power Dissipation (Note 1a) $T_A = 25^\circ\text{C}$	2.0	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	–55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise noted.)

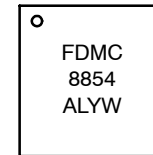
Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	60	°C/W

$V_{DS}$	$R_{DS(on)}$ MAX	$I_D$ MAX
30 V	5.7 mΩ @ 10 V	15 A
	7.6 mΩ @ 4.5 V	



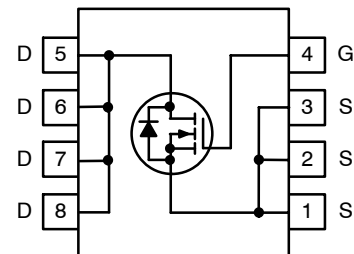
WDFN8 3.3x3.3, 0.65P  
CASE 511DH

### MARKING DIAGRAM



FDMC8854 = Device Code  
A = Assembly Site  
L = Wafer Lot Number  
YW = Assembly Start Week

### PIN ASSIGNMENT



N-Channel MOSFET

### ORDERING INFORMATION

Device	Package	Shipping†
FDMC8854	WDFN8 (Pb-Free, Halide Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

# FDMC8854

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0 V	30	–	–	V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, referenced to 25°C	–	21	–	mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 24 V, V <sub>GS</sub> = 0 V	–	–	1	μA
I <sub>GSS</sub>	Gate to Source Leakage Current	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V	–	–	±100	nA

### ON CHARACTERISTICS (Note 2)

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	1	1.9	3	V
ΔV <sub>GS(th)</sub> / ΔT <sub>J</sub>	Gate to Source Threshold Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, referenced to 25°C	–	–6	–	mV/°C
r <sub>DS(on)</sub>	Static Drain to Source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 15 A	–	4.4	5.7	mΩ
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 13 A	–	5.6	7.6	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 15 A, T <sub>J</sub> = 125°C	–	6.6	9.0	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 15 A	–	60	–	S

### DYNAMIC CHARACTERISTICS

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0 V, f = 1 MHz	–	2560	3405	pF
C <sub>oss</sub>	Output Capacitance		–	515	685	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		–	290	435	pF
R <sub>g</sub>	Gate Resistance	f = 1 MHz	–	1.3	–	Ω

### SWITCHING CHARACTERISTICS

t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 10 V, I <sub>D</sub> = 15 A, V <sub>GS</sub> = 10 V, R <sub>GEN</sub> = 6 Ω	–	13	23	ns
t <sub>r</sub>	Rise Time		–	5	10	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		–	31	50	ns
t <sub>f</sub>	Fall Time		–	5	10	ns
Q <sub>g(TOT)</sub>	Total Gate Charge	V <sub>DD</sub> = 10 V, I <sub>D</sub> = 15 A, V <sub>GS</sub> = 10 V	–	41	57	nC
Q <sub>gs</sub>	Gate to Source Gate Charge		–	7	–	nC
Q <sub>gd</sub>	Gate to Drain "Miller" Charge		–	7	–	nC

### DRAIN-SOURCE DIODE CHARACTERISTICS

V <sub>SD</sub>	Source to Drain Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 15 A (Note 2)	–	0.8	1.3	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = 15 A, di/dt = 100 A/μs	–	33	50	ns
Q <sub>rr</sub>	Reverse Recovery Charge		–	28	42	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

#### NOTES:

- R<sub>θJA</sub> is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR-4 material. R<sub>θJC</sub> is guaranteed by design while R<sub>θCA</sub> is determined by the user's board design.



- 60°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



- 135°C/W when mounted on a minimum pad of 2 oz copper.

- Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

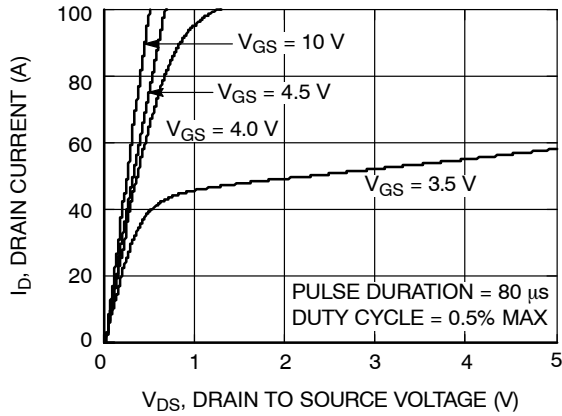


Figure 1. On Region Characteristics

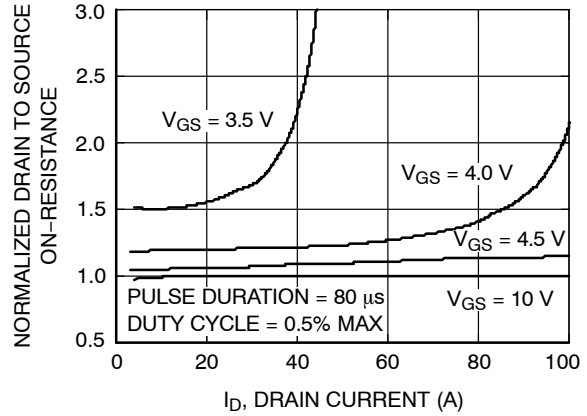


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

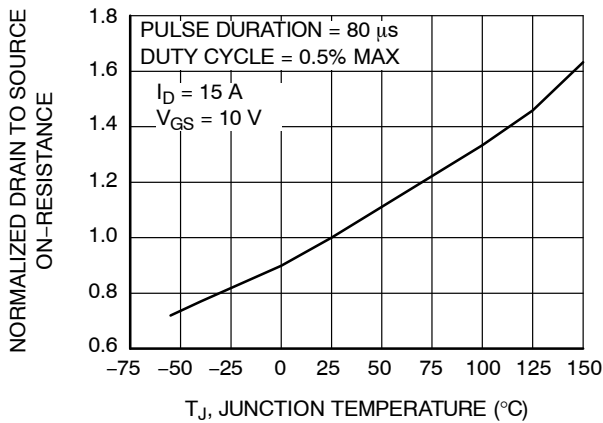


Figure 3. Normalized On Resistance vs. Junction Temperature

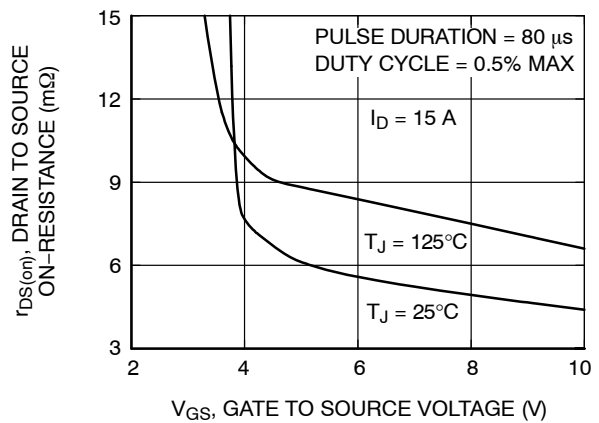


Figure 4. On-Resistance vs. Gate to Source Voltage

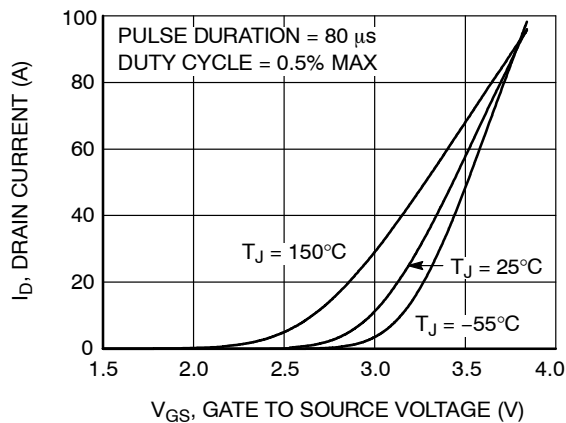


Figure 5. Transfer Characteristics

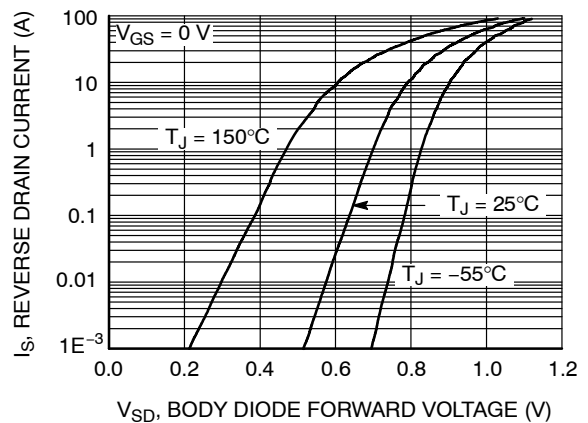


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$  unless otherwise noted) (continued)

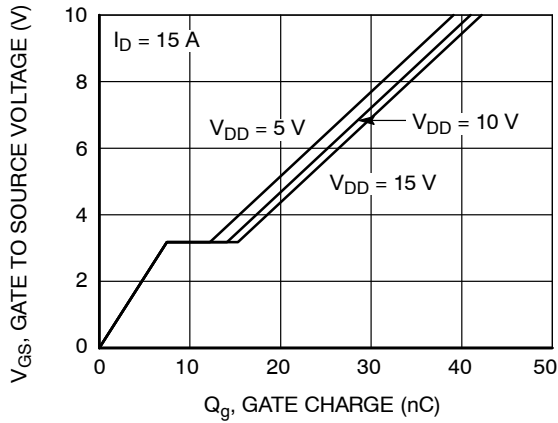


Figure 7. Gate Charge Characteristics

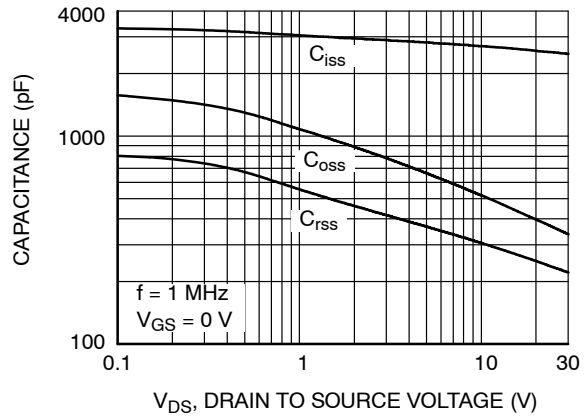


Figure 8. Capacitance vs. Drain to Source Voltage

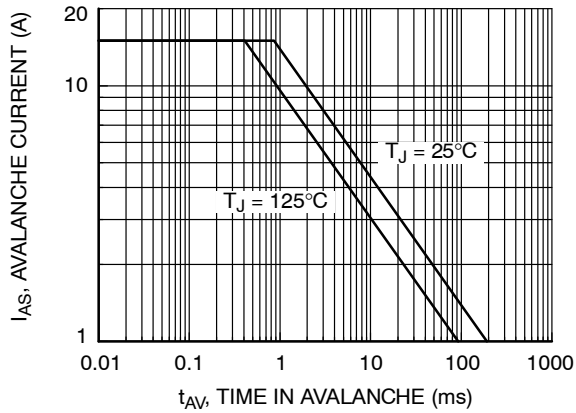


Figure 9. Unclamped Inductive Switching Capability

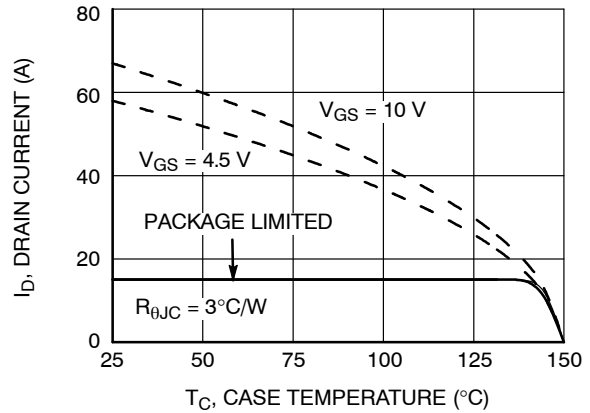


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

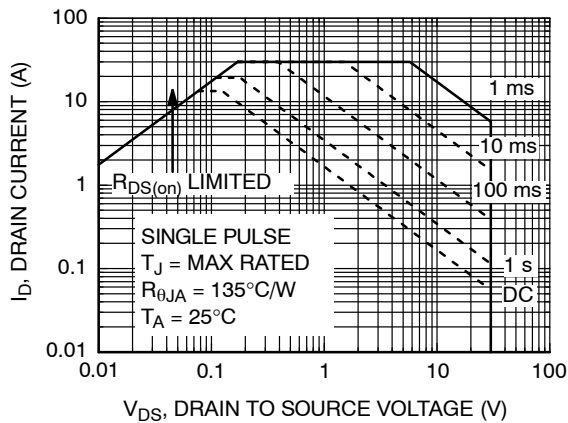


Figure 11. Forward Bias Safe Operating Area

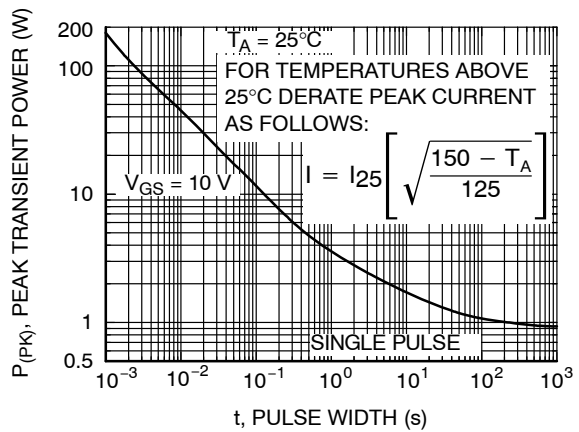


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$  unless otherwise noted) (continued)

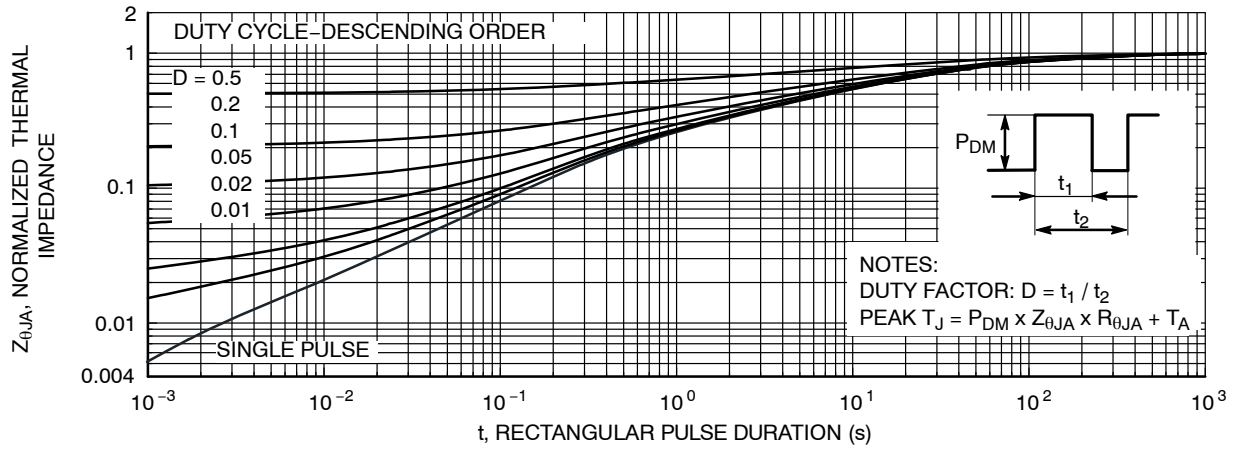


Figure 13. Transient Thermal Response Curve

# MECHANICAL CASE OUTLINE

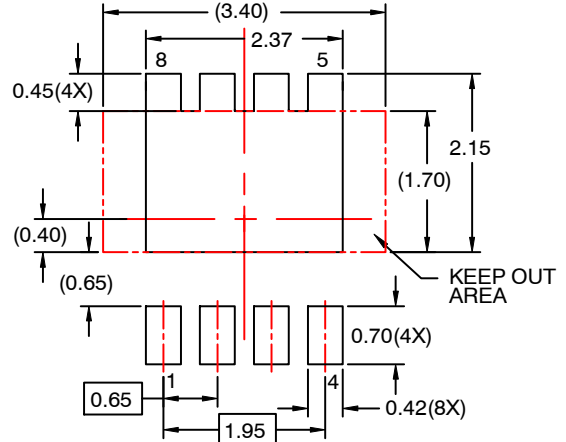
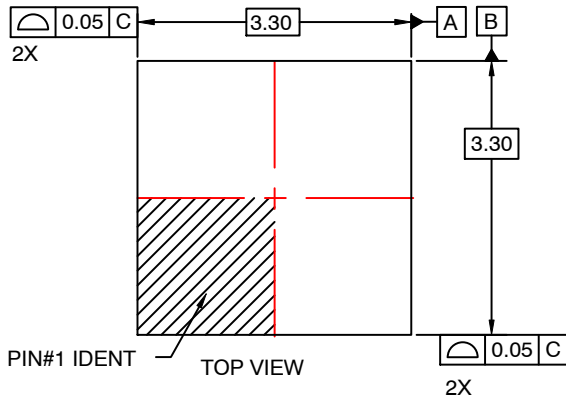
## PACKAGE DIMENSIONS

ON Semiconductor®

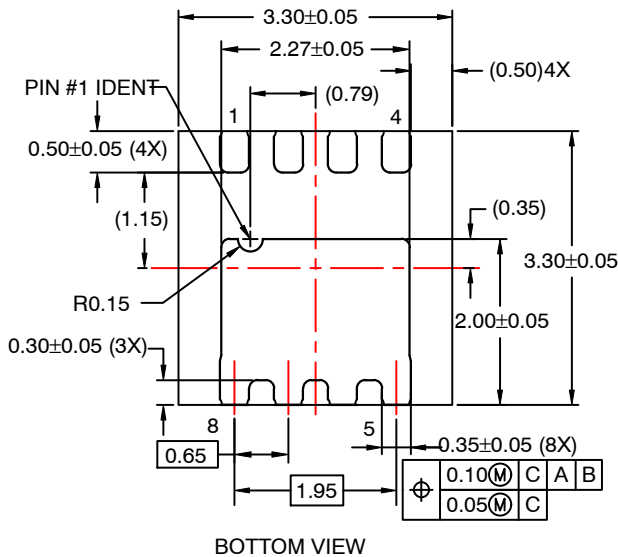
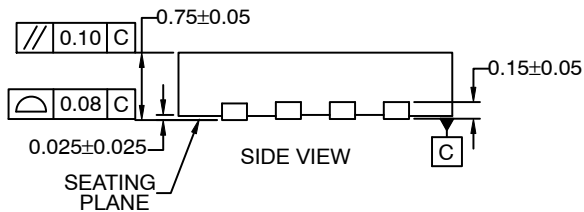


WDFN8 3.3x3.3, 0.65P  
CASE 511DH  
ISSUE O

DATE 31 JUL 2016



RECOMMENDED LAND PATTERN



BOTTOM VIEW

NOTES:

- A. DOES NOT CONFORM TO JEDEC REGISTRATION MO-229
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

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