

150 mA, Very Low Dropout Bias Rail CMOS Voltage Regulator

NCP120

The NCP120 is a 150 mA VLDO equipped with NMOS pass transistor and a separate bias supply voltage (V_{BIAS}). The device provides very stable, accurate output voltage with low noise suitable for space constrained, noise sensitive applications. In order to optimize performance for battery operated portable applications, the NCP120 features low I_Q consumption. The XDFN6 1.2 mm x 1.2 mm package is optimized for use in space constrained applications.

Features

- Input Voltage Range: 0.8 V to 5.5 V
- Bias Voltage Range: 2.4 V to 5.5 V
- Fixed Output Voltage Device
- Output Voltage Range: 0.8 V to 2.1 V
- $\pm 1.5\%$ Accuracy over Temperature, $0.5\% V_{OUT}$ @ 25°C
- Ultra-Low Dropout: 75 mV Maximum at 150 mA
- Very Low Bias Input Current of Typ. 80 μA
- Very Low Bias Input Current in Disable Mode: Typ. 0.5 μA
- Logic Level Enable Input for ON/OFF control
- Output Active Discharge Option available
- Stable with a 1 μF Ceramic Capacitor
- Available in XDFN6 – 1.2 mm x 1.2 mm x 0.4 mm package
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Battery-powered Equipment
- Smartphones, Tablets
- Cameras, DVRs, STB and Camcorders

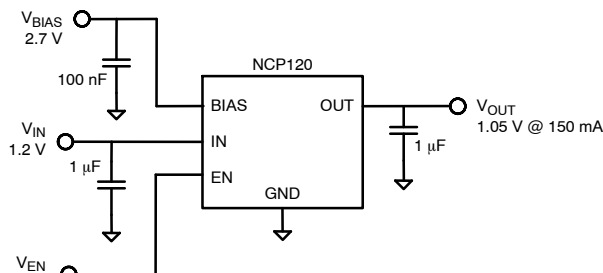


Figure 1. Typical Application Schematics

MARKING DIAGRAM

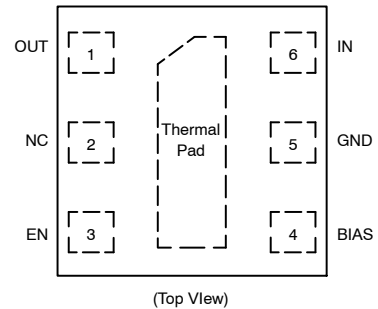


XDFN6
CASE 711AT



XX = Specific Device Code
M = Date Code

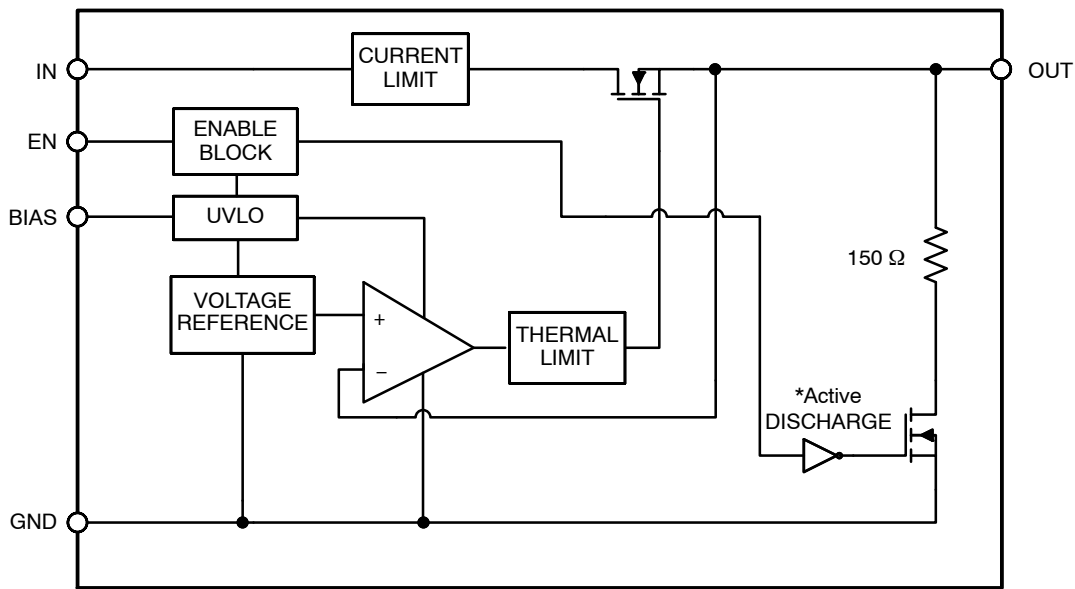
PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 7 of this data sheet.

NCP120



*Active output discharge function is present only in NCP120AMXyyyTCG devices.
yyy denotes the particular output voltage option.

Figure 2. Simplified Schematic Block Diagram

PIN FUNCTION DESCRIPTION

| Pin No. | Pin Name | Description |
|---------|----------|--|
| 1 | OUT | Regulated Output Voltage pin |
| 2 | N/C | Not internally connected |
| 3 | EN | Enable pin. Driving this pin high enables the regulator. Driving this pin low puts the regulator into shutdown mode. |
| 4 | BIAS | Bias voltage supply for internal control circuits. This pin is monitored by internal Under-Voltage Lockout Circuit. |
| 5 | GND | Ground pin |
| 6 | IN | Input Voltage Supply pin |
| Pad | | Should be soldered to the ground plane for increased thermal performance. |

ABSOLUTE MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|--------------------|-------------------------------|------|
| Input Voltage (Note 1) | V_{IN} | -0.3 to 6 | V |
| Output Voltage | V_{OUT} | -0.3 to $(V_{IN}+0.3) \leq 6$ | V |
| Chip Enable and Bias Input | V_{EN}, V_{BIAS} | -0.3 to 6 | V |
| Output Short Circuit Duration | t_{SC} | unlimited | s |
| Maximum Junction Temperature | T_J | 150 | °C |
| Storage Temperature | T_{STG} | -55 to 150 | °C |
| ESD Capability, Human Body Model (Note 2) | ESD_{HBM} | 2000 | V |
| ESD Capability, Machine Model (Note 2) | ESD_{MM} | 200 | V |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection (except OUT pin) and is tested by the following methods:
ESD Human Body Model tested per EIA/JESD22-A114
ESD Machine Model tested per EIA/JESD22-A115
Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

THERMAL CHARACTERISTICS

| Rating | Symbol | Value | Unit |
|--|-----------------|-------|------|
| Thermal Characteristics, XDFN6 1.2 mm x 1.2 mm Thermal Resistance, Junction-to-Air | $R_{\theta JA}$ | 170 | °C/W |

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ELECTRICAL CHARACTERISTICS

$-40^{\circ}\text{C} \leq T_J \leq 85^{\circ}\text{C}$; $V_{\text{BIAS}} = 2.7\text{ V}$ or $(V_{\text{OUT}} + 1.6\text{ V})$, whichever is greater, $V_{\text{IN}} = V_{\text{OUT(NOM)}} + 0.3\text{ V}$, $I_{\text{OUT}} = 1\text{ mA}$, $V_{\text{EN}} = 1\text{ V}$, unless otherwise noted. $C_{\text{IN}} = 1\text{ }\mu\text{F}$, $C_{\text{BIAS}} = 0.1\text{ }\mu\text{F}$, $C_{\text{OUT}} = 1\text{ }\mu\text{F}$ (effective capacitance) (Note 3). Typical values are at $T_J = +25^{\circ}\text{C}$. Min/Max values are for $-40^{\circ}\text{C} \leq T_J \leq 85^{\circ}\text{C}$ unless otherwise noted. (Note 4)

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Unit |
|-----------------------------------|--|---------------------------|----------------------------------|------------|------|----------------------------|
| Operating Input Voltage Range | | V_{IN} | $V_{\text{OUT}}+V_{\text{DO}}$ | | 5.5 | V |
| Operating Bias Voltage Range | | V_{BIAS} | $(V_{\text{OUT}}+1.35) \geq 2.4$ | | 5.5 | V |
| Undervoltage Lock-out | V_{BIAS} Rising Hysteresis | UVLO | | 1.6 0.2 | | V |
| Output Voltage Accuracy | $-40^{\circ}\text{C} \leq T_J \leq 85^{\circ}\text{C}$, $V_{\text{OUT(NOM)}} + 0.3\text{ V} \leq V_{\text{IN}} \leq 5.0\text{ V}$, 2.7 V or $(V_{\text{OUT(NOM)}} + 1.6\text{ V})$, whichever is greater < $V_{\text{BIAS}} < 5.5\text{ V}$, $1\text{ mA} < I_{\text{OUT}} < 150\text{ mA}$ | V_{OUT} | -1.5 | | +1.5 | % |
| Output Voltage Accuracy | | V_{OUT} | | ± 0.5 | | % |
| V_{IN} Line Regulation | $V_{\text{OUT(NOM)}} + 0.3\text{ V} \leq V_{\text{IN}} \leq 5.0\text{ V}$ | LineReg | | 0.01 | | %/V |
| V_{BIAS} Line Regulation | 2.7 V or $(V_{\text{OUT(NOM)}} + 1.6\text{ V})$, whichever is greater < $V_{\text{BIAS}} < 5.5\text{ V}$ | LineReg | | 0.01 | | %/V |
| Load Regulation | $I_{\text{OUT}} = 1\text{ mA}$ to 150 mA | LoadReg | | 1.5 | | mV |
| V_{IN} Dropout Voltage | $I_{\text{OUT}} = 150\text{ mA}$ (Note 5) | V_{DO} | | 37 | 75 | mV |
| V_{BIAS} Dropout Voltage | $I_{\text{OUT}} = 150\text{ mA}$, $V_{\text{IN}} = V_{\text{BIAS}}$ (Note 5) | V_{DO} | | 1.1 | 1.4 | V |
| Output Current Limit | $V_{\text{OUT}} = 90\% V_{\text{OUT(NOM)}}$ | I_{CL} | 200 | 330 | 600 | mA |
| Bias Pin Operating Current | $V_{\text{BIAS}} = 2.7\text{ V}$ | I_{BIAS} | | 80 | 110 | μA |
| Bias Pin Disable Current | $V_{\text{EN}} \leq 0.4\text{ V}$ | $I_{\text{BIAS(DIS)}}$ | | 0.5 | 1 | μA |
| Vinut Pin Disable Current | $V_{\text{EN}} \leq 0.4\text{ V}$ | $I_{\text{VIN(DIS)}}$ | | 0.5 | 1 | μA |
| EN Pin Threshold Voltage | EN Input Voltage "H" | $V_{\text{EN(H)}}$ | 0.9 | | | V |
| | EN Input Voltage "L" | $V_{\text{EN(L)}}$ | | | 0.4 | |
| EN Pull Down Current | $V_{\text{EN}} = 5.5\text{ V}$ | I_{EN} | | 0.3 | 1.0 | μA |
| Turn-On Time | $C_{\text{OUT}} = 1\text{ }\mu\text{F}$, From assertion of V_{EN} to $V_{\text{OUT}} = 98\% V_{\text{OUT(NOM)}}$, $V_{\text{OUT(NOM)}} = 1.05\text{ V}$ | t_{ON} | | 150 | | μs |
| Power Supply Rejection Ratio | V_{IN} to V_{OUT} , $f = 1\text{ kHz}$, $I_{\text{OUT}} = 150\text{ mA}$, $V_{\text{IN}} \geq V_{\text{OUT}} + 0.5\text{ V}$ | PSRR(V_{IN}) | | 70 | | dB |
| | V_{BIAS} to V_{OUT} , $f = 1\text{ kHz}$, $I_{\text{OUT}} = 150\text{ mA}$, $V_{\text{IN}} \geq V_{\text{OUT}} + 0.5\text{ V}$ | PSRR(V_{BIAS}) | | 80 | | |
| Output Noise Voltage | $V_{\text{IN}} = V_{\text{OUT}} + 0.5\text{ V}$, $V_{\text{OUT(NOM)}} = 1.05\text{ V}$, $f = 10\text{ Hz}$ to 100 kHz | V_{N} | | 40 | | μV_{RMS} |
| Thermal Shutdown Threshold | Temperature increasing | | | 160 | | $^{\circ}\text{C}$ |
| | Temperature decreasing | | | 140 | | |
| Output Discharge Pull-Down | $V_{\text{EN}} \leq 0.4\text{ V}$, $V_{\text{OUT}} = 0.5\text{ V}$, NCP120A options only | R_{DISCH} | | 150 | | Ω |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- Effective capacitance, including the effect of DC bias, tolerance and temperature. See the Application Information section for more information.
- Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at $T_A = 25^{\circ}\text{C}$. Low duty cycle pulse techniques are used during the testing to maintain the junction temperature as close to ambient as possible.
- Dropout voltage is characterized when V_{OUT} falls 3% below $V_{\text{OUT(NOM)}}$.

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APPLICATIONS INFORMATION

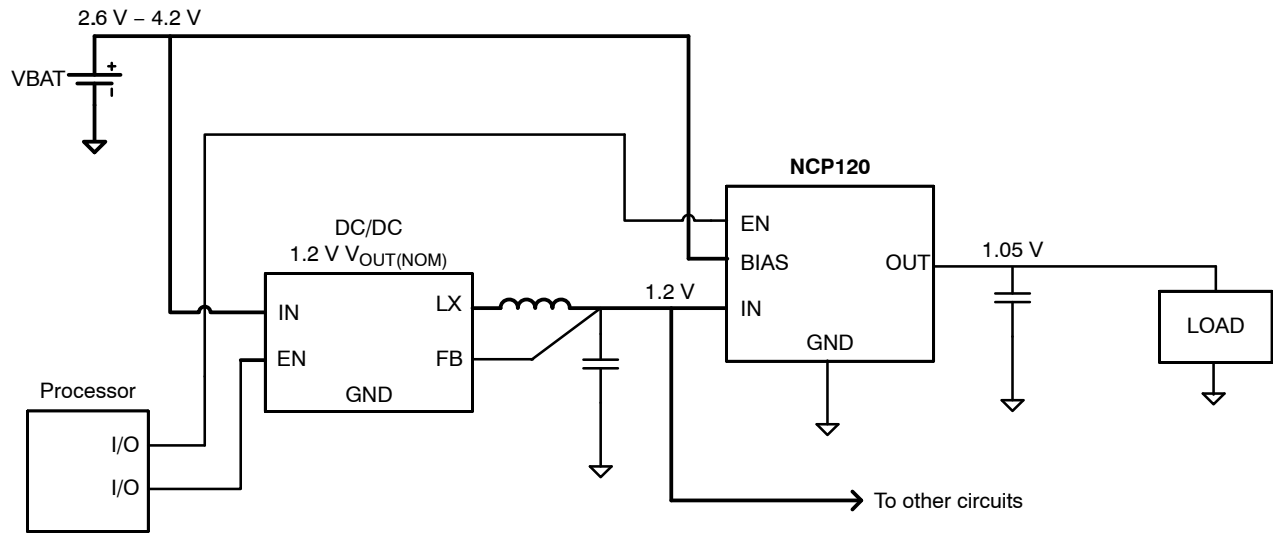


Figure 3. Typical Application: Low-Voltage Post-Regulator with ON/OFF functionality

NCP120

TYPICAL CHARACTERISTICS

AT $T_J = +25^\circ\text{C}$, $V_{IN} = V_{OUT(TYP)} + 0.3\text{ V}$, $V_{BIAS} = 2.7\text{ V}$, $V_{EN} = V_{BIAS}$, $V_{OUT(NOM)} = 1.05\text{ V}$, $I_{OUT} = 150\text{ mA}$, $C_{IN} = 1\text{ MF}$, $C_{BIAS} = 0.1\text{ MF}$, AND $C_{OUT} = 1\text{ MF}$ (EFFECTIVE CAPACITANCE), UNLESS OTHERWISE NOTED.

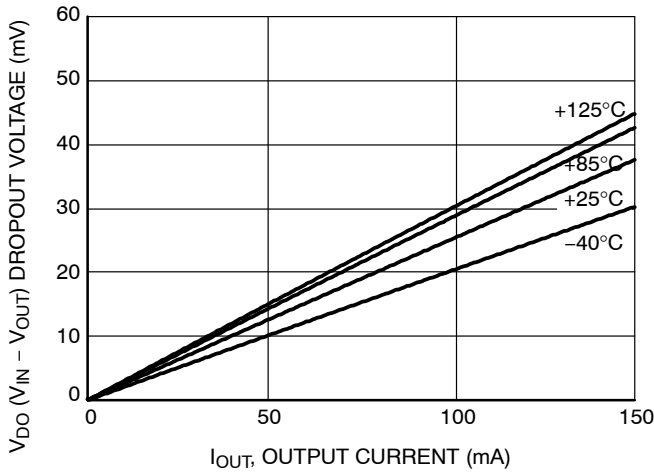


Figure 4. V_{IN} Dropout Voltage vs. I_{OUT} and Temperature T_J

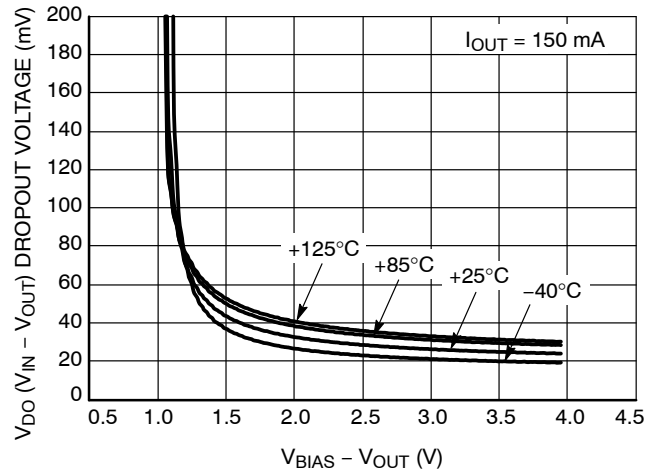


Figure 5. V_{IN} Dropout Voltage vs. $(V_{BIAS} - V_{OUT})$ and Temperature T_J

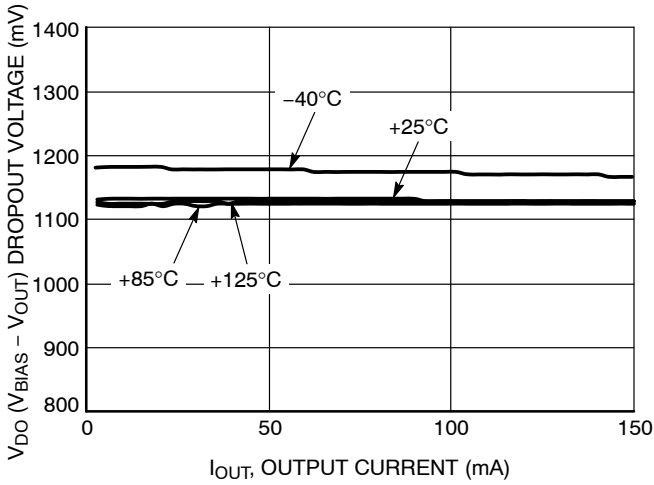


Figure 6. V_{BIAS} Dropout Voltage vs. I_{OUT} and Temperature T_J

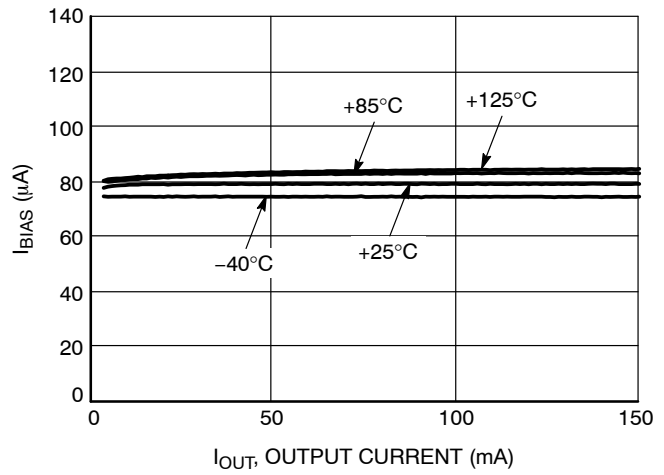


Figure 7. BIAS Pin Current vs. I_{OUT} and Temperature T_J

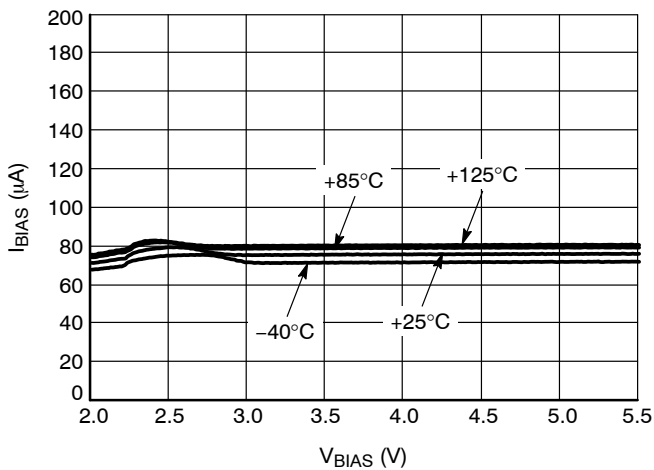


Figure 8. BIAS Pin Current vs. V_{BIAS} and Temperature T_J

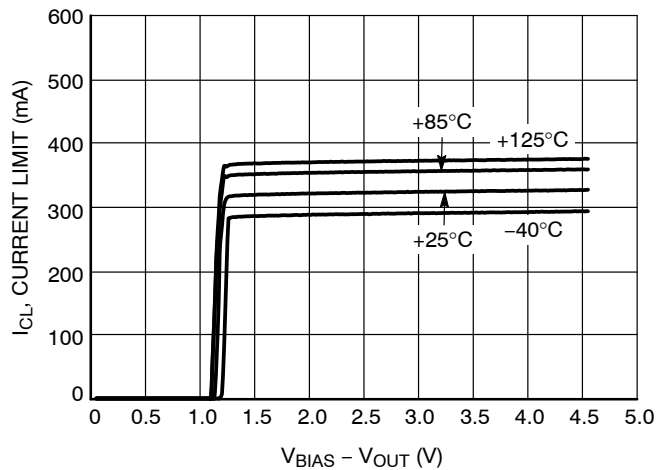


Figure 9. Current Limit vs. $(V_{BIAS} - V_{OUT})$

APPLICATIONS INFORMATION

The NCP120 dual-rail very low dropout voltage regulator is using NMOS pass transistor for output voltage regulation from V_{IN} voltage. All the low current internal control circuitry is powered from the V_{BIAS} voltage.

The use of an NMOS pass transistor offers several advantages in applications. Unlike a PMOS topology devices, the output capacitor has reduced impact on loop stability. V_{IN} to V_{OUT} operating voltage difference can be very low compared with standard PMOS regulators in very low V_{IN} applications.

The NCP120 offers smooth monotonic start-up. The controlled voltage rising limits the inrush current.

The Enable (EN) input is equipped with internal hysteresis.

NCP120 is a Fixed Voltage linear regulator.

Dropout Voltage

Because of two power supply inputs V_{IN} and V_{BIAS} and one V_{OUT} regulator output, there are two Dropout voltages specified.

The first, the V_{IN} Dropout voltage is the voltage difference ($V_{IN} - V_{OUT}$) when V_{OUT} starts to decrease by percents specified in the Electrical Characteristics table. V_{BIAS} is high enough, specific value is published in the Electrical Characteristics table.

The second, V_{BIAS} dropout voltage is the voltage difference ($V_{BIAS} - V_{OUT}$) when V_{IN} and V_{BIAS} pins are joined together and V_{OUT} starts to decrease.

Input and Output Capacitors

The device is designed to be stable for ceramic output capacitors with Effective capacitance in the range from 1 μ F to 10 μ F. The device is also stable with multiple capacitors in parallel, having the total effective capacitance in the specified range.

In applications where no low input supplies impedance available (PCB inductance in V_{IN} and/or V_{BIAS} inputs as example), the recommended $C_{IN} = 1 \mu$ F and $C_{BIAS} = 0.1 \mu$ F or greater. Ceramic capacitors are recommended. For the best performance all the capacitors should be connected to the NCP120 respective pins directly in the device PCB copper layer, not through vias having not negligible impedance.

When using small ceramic capacitor, their capacitance is not constant but varies with applied DC biasing voltage, temperature and tolerance. The effective capacitance can be much lower than their nominal capacitance value, most importantly in negative temperatures and higher LDO output voltages. That is why the recommended Output capacitor capacitance value is specified as Effective value in the specific application conditions.

Enable Operation

The enable pin will turn the regulator on or off. The threshold limits are covered in the electrical characteristics table in this data sheet. If the enable function is not to be used then the pin should be connected to V_{IN} or V_{BIAS} .

Current Limitation

The internal Current Limitation circuitry allows the device to supply the full nominal current and surges but protects the device against Current Overload or Short.

Thermal Protection

Internal thermal shutdown (TSD) circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When TSD activated, the regulator output turns off. When cooling down under the low temperature threshold, device output is activated again. This TSD feature is provided to prevent failures from accidental overheating.

NCP120

ORDERING INFORMATION

| Device | Nominal Output Voltage | Marking | Marking Rotation | Option | Package | Shipping [†] |
|-----------------------------|------------------------|---------|------------------|-------------------------|--------------------|---|
| NCP120AMX080TCG | 0.80 V | A | 180° | Output Active Discharge | XDFN6 (Pb-Free) | 3000 or 5000 / Tape & Reel (Note 6) |
| NCP120AMX105TCG | 1.05 V | D | 180° | | | |
| NCP120AMX110TCG (Note 6) | 1.10 V | E | 180° | | | |
| NCP120AMX115TCG | 1.15 V | F | 180° | | | |
| NCP120AMX120TCG | 1.20 V | J | 180° | | | |
| NCP120AMX150TCG | 1.50 V | K | 180° | | | |
| NCP120AMX180TCG | 1.80 V | L | 180° | | | |
| NCP120AMX210TCG | 2.10 V | P | 180° | | | |
| NCP120BMX080TCG | 0.80 V | A | 270° | Non-Active Discharge | | |
| NCP120BMX105TCG | 1.05 V | D | 270° | | | |
| NCP120BMX110TCG | 1.10 V | E | 270° | | | |
| NCP120BMX115TCG | 1.15 V | F | 270° | | | |
| NCP120BMX120TCG | 1.20 V | J | 270° | | | |
| NCP120BMX150TCG | 1.50 V | K | 270° | | | |
| NCP120BMX180TCG | 1.80 V | L | 270° | | | |
| NCP120BMX210TCG | 2.10 V | P | 270° | | | |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

To order other package and voltage variants, please contact your **onsemi** sales representative

6. Product processed after October 1, 2022 are shipped with quantity 5000 units / tape & reel.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

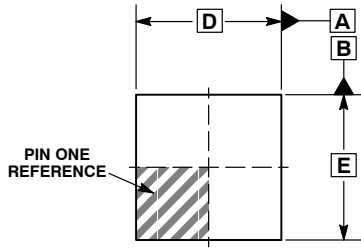
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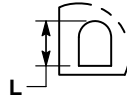
SCALE 4:1

XDFN6 1.20x1.20, 0.40P
CASE 711AT
ISSUE C

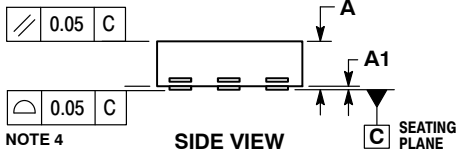
DATE 04 DEC 2015



TOP VIEW

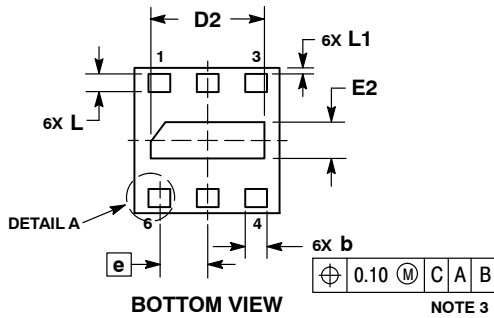


DETAIL A
OPTIONAL
CONSTRUCTION



SIDE VIEW

NOTE 4



BOTTOM VIEW

NOTE 3

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO THE PLATED TERMINALS.
4. COPLANARITY APPLIES TO THE PAD AS WELL AS THE TERMINALS.

| DIM | MILLIMETERS | | |
|-----|-------------|------|------|
| | MIN | TYP | MAX |
| A | 0.30 | 0.37 | 0.45 |
| A1 | 0.00 | 0.03 | 0.05 |
| b | 0.13 | 0.18 | 0.23 |
| D | 1.15 | 1.20 | 1.25 |
| D2 | 0.84 | 0.94 | 1.04 |
| E | 1.15 | 1.20 | 1.25 |
| E2 | 0.20 | 0.30 | 0.40 |
| e | 0.40 BSC | | |
| L | 0.15 | 0.20 | 0.25 |
| L1 | 0.00 | 0.05 | 0.10 |

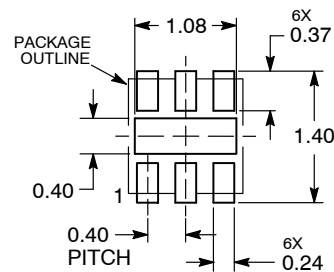
GENERIC
MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

RECOMMENDED
MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| | | |
|------------------|---------------------------|--|
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| DESCRIPTION: | XDFN6, 1.20 X 1.20, 0.40P | PAGE 1 OF 1 |

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