USB 3.1 SuperSpeed 10 Gbps Switch

FUSB340

Description

The FUSB340 is a 2:1 data switch for USB SuperSpeed Gen1 and Gen2, 5 Gbps and 10 Gbps data. It is targeted at the mobile device market and for use in Type−C applications where a reversible cable requires a switch.

The FUSB340 data switch offers superior performance various high speed data transmission protocols:

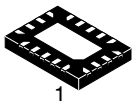
- USB 3.1 SuperSpeed (Gen 2), 10 Gbps
- PCI Express, Gen 3
- SATA
- Fibre Channel
- Display Port 1.3

Features

- 10 GHz Typical Bandwidth
- USB 3.1 SuperSpeed 5 Gbps and10 Gbps Switch
- −1.0 dB Typical Insertion Loss at 2.5 GHz
- Low Active Power of 12 μA Typical
- Low Shutdown Power of < 1 μA Max.
- 2 kV HBM ESD Protection
- Small Packaging, 18 Lead TMLP
- Wide V_{DD} Operating Range, 1.5 V−5.0 V
- This is a Pb−Free Device

Applications

- Smartphones
- Tablets
- Notebooks



X2QFN18
CASE 722AB

MARKING DIAGRAM

NK = Specific Device Code
&K = Lot Code
&2 = Date Code
&Z = Assembly Plant Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

BLOCK DIAGRAM

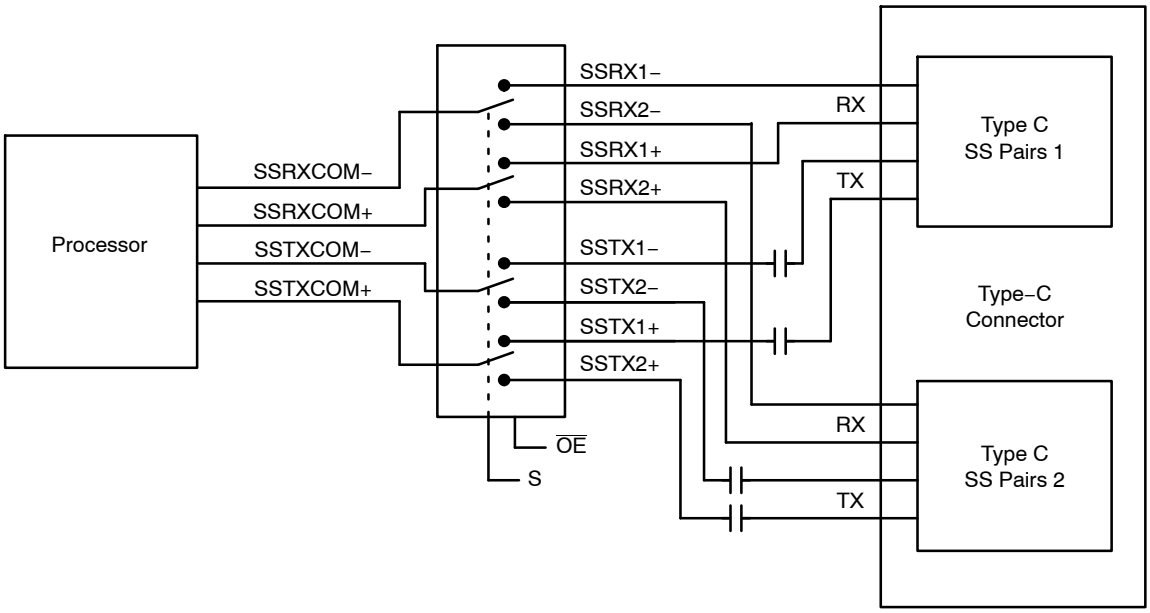


Figure 1. Block Diagram

TYPICAL APPLICATION

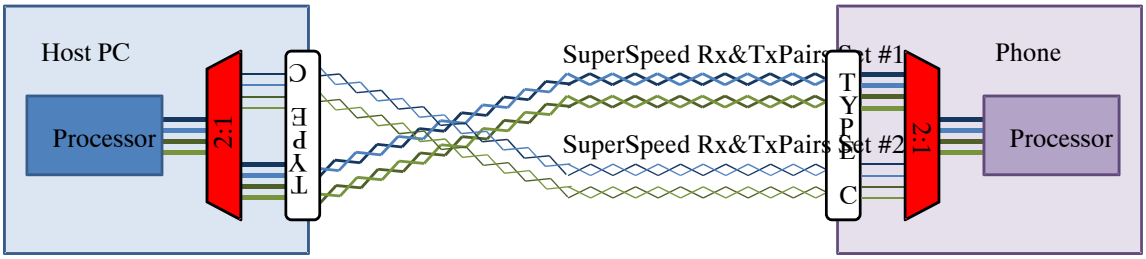


Figure 2. Typical Application

PIN CONFIGURATION

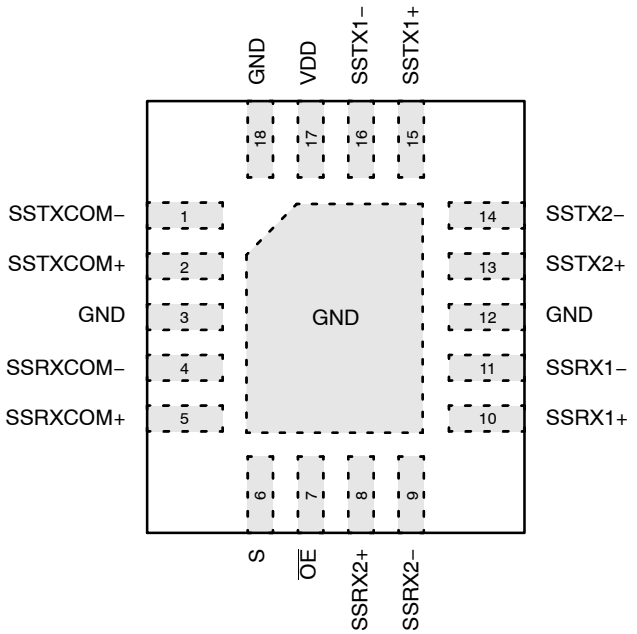


Figure 3. Pin Assignment (Top Through View)

PIN DESCRIPTIONS

Pin #	Name	Type	Description
1	SSTXCOM−	SW	SuperSpeed TX− Common
2	SSTXCOM+	SW	SuperSpeed TX+ Common
3	GND	GND	Ground (connected to die attach pad)
4	SSRXCOM−	SW	SuperSpeed RX− Common
5	SSRXCOM+	SW	SuperSpeed RX+ Common
6	S	Input	Switch Select (0 = SW1, 1 = SW2)
7	$\overline{OE}$	Input	Output Enable (0 = Switches Enabled, 1 = Switches Disabled)
8	SSRX2+	SW	SuperSpeed RX2+
9	SSRX2−	SW	SuperSpeed RX2−
10	SSRX1+	SW	SuperSpeed RX1+
11	SSRX1−	SW	SuperSpeed RX1−
12	GND	GND	Ground (connected to die attach pad)
13	SSTX2+	SW	SuperSpeed TX2+
14	SSTX2−	SW	SuperSpeed TX2−
15	SSTX1+	SW	SuperSpeed TX1+
16	SSTX1−	SW	SuperSpeed TX1−
17	V_{DD}	VDD	Device Power
18	GND	GND	Ground

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
V_{DD}	Supply Voltage		−0.5	6.0	V
V_{CNTRL}	DC Input Voltage (S, $\overline{OE}$) (Note 1)		−0.5	V_{DD}	V
V_{SW}	DC Switch I/O Voltage (Notes 1, 2)		−0.3	2.1	V
I_{IK}	DC Input Diode Current		−50	–	mA
I_{sw}	DC Switch Current		–	25	mA
T_{STG}	Storage Temperature		−65	+150	°C
MSL	Moisture Sensitivity Level (JEDEC J−STD−020A)		–	1	
ESD	Human Body Model, JEDEC: JESD22−A114	All Pins	2	–	kV
	IEC 61000−2−4, Level 4, for Switch Pins	Contact	8	–	
		Air	15	–	
	Charged Device Model, JESD22−C101		1	–	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.
2. V_{SW} refers to analog data switch paths.

RECOMMENDED OPERATING RANGES

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply Voltage	1.5	5.0	V
$t_{RAMP(VDD)}$	Power Supply Slew Rate	100	1000	μs/V
V_{CNTRL}	Control Input Voltage (S, $\overline{OE}$) (Note 3)	0	5.0	V
V_{SW}	Switch I/O Voltage (Both SSUSB Switch Paths)	0	2.0	V
T_A	Operating Temperature	−40	+85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. The control inputs must be held HIGH or LOW; they must not float.

DC AND TRANSIENT CHARACTERISTICS

All typical values are at T_A = 25°C unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD} (V)	T_A = −40°C to +85°C			Unit
				Min	Typ	Max	
V_{IK}	Clamp Diode Voltage S, $\overline{OE}$	I_{IN} = −18 mA	1.5	−1.2	–	−0.6	V
I_{IK}	Clamp Diode Current (Switch Pins)	V_{IN} = −0.3 V	0	–	–	18	μA
V_{IH}	Control Input Voltage High	S, $\overline{OE}$	1.5	1.30	–	–	V
		S, $\overline{OE}$	3.6	1.4	–	–	V
		S, $\overline{OE}$	5.0	1.5	–	–	V
V_{IL}	Control Input Voltage Low	S, $\overline{OE}$	1.5	–	–	0.4	V
		S, $\overline{OE}$	3.6	–	–	0.4	V
		S, $\overline{OE}$	5.0	–	–	0.4	V
I_{IN}	Control Input Leakage	V_{SW} = −0.6 to 2.0 V, V_{CNTRL} = 0 to V_{DD}	5.0	−500	–	500	nA
I_{OZ}	Off−State Leakage for Open Data Paths	V_{SW} = 0.0 ≤ DATA ≤ 2.0 V	5.0	−0.5	–	0.5	μA
I_{CL}	On−State Leakage for Closed Data Paths (Note 4)	V_{SW} = 0.0 ≤ DATA ≤ 2.0 V	5.0	−0.5	–	0.5	μA
I_{OFF}	Power−Off Leakage Current (All I/O Ports)	V_{SW} = 0 V or 2.0 V	0	−500	–	500	nA

DC AND TRANSIENT CHARACTERISTICS (continued)

All typical values are at T_A = 25°C unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD} (V)	T_A = −40°C to +85°C			Unit
				Min	Typ	Max	
R_{ON}	Switch On Resistance	V_{SW} = 0 V, I_{ON} = −8 mA	1.5	–	5.4	8.0	Ω
ΔR_{ON}	Difference in RON Between Positive−Negative	V_{SW} = 0 V, I_{ON} = −8 mA	1.5	–	0.1	–	Ω
R_{ONF}	Flatness for RON	V_{SW} = 0 ≤ DATA ≤ 2.0 V, I_{ON} =−8 mA	1.5	–	0.9	–	Ω
I_{CC}	Quiescent Supply Current	$V_{\overline{OE}}$ = 0, V_{SEL} = 0 or V_{DD}, I_{OUT} = 0	5.0	–	12	30	μA
I_{CCZ}	Quiescent Supply Current (High Impedance)	V_{SEL} = X, $V_{\overline{OE}}$ = V_{DD}, I_{OUT} = 0	5.0	–	–	1	μA
I_{CCT}	Increase in Quiescent Supply Current per VCNTRL	V_{SEL} or $V_{\overline{OE}}$ = 1.5 V	5.0	–	5	15	μA

4. For this test, the data switch is closed with the respective switch pin floating.

AC ELECTRICAL CHARACTERISTICS

All typical value are for V_{DD} = 3.6 V and T_A = 25°C unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD} (V)	T_A = −40°C to +85°C			Unit
				Min	Typ	Max	
t_{ON}	Turn−On Time, S to Output	R_L = 50 Ω, C_L = 0 pF, V_{SW} = 0 V, V_{SW} = 0.6 V	1.5 to 5.0 V	–	350	600	ns
t_{OFF}	Turn−Off Time, S to Output	R_L = 50 Ω, C_L = 0 pF, V_{SW} = 0 V, V_{SW} = 0.6 V	1.5 to 5.0 V	–	125	300	ns
$t_{ZHM,ZL}$	Enable Time, $\overline{OE}$ to Output	R_L = 50 Ω, C_L = 0 pF, V_{SW} = 0.6 V	1.5 to 5.0 V	–	60	150	μs
$t_{LZM,HZ}$	Disable Time, $\overline{OE}$ to Output	R_L = 50 Ω, C_L = 0 pF, V_{SW} = 0.6 V	1.5 to 5.0 V	–	35	240	ns
t_{PD}	Propagation Delay (Note 5)	C_L = 0 pF, R_L = 50 Ω	1.5 to 5.0 V	–	60	–	ps
t_{BBM}	Break−Before−Make (Note 5)	R_L = 50 Ω, C_L = 0 pF, V_{SW1} = 0.6 V, V_{SW2} = −0.6 V	1.5 to 5.0 V	100	–	350	ns
DO_{IRR}	Differential Off Isolation (Note 5)	V_S = 0dBm, R_L = 50 Ω, f = 2.5 GHz	3.6 V	–	−28	–	dB
		V_S = 0 dBm, R_L = 50 Ω, f = 5.0 GHz			−25		
SDDNEXT	Differential Channel Crosstalk (Note 5)	V_S = 0 dBm, R = 50 Ω, f = 2.5 GHz	3.6 V	–	−44	–	dB
		V_S = 0 dBm, R = 50 Ω, f = 5.0 GHz			−40		
DIL	Differential Insertion Loss (Note 5) (All Data Paths)	V_{IN} = 0dBm, f = 2.5 GHz, R_L = 50 Ω, C_L = 0 pF	3.6 V	–	−1.0	–	dB
		V_{IN} = 0 dBm, f = 5.0 GHz, R_L = 50 Ω, C_L = 0 pF			−1.8		
BW	Differential, −3 dB Bandwidth (Note 5)	V_{IN} = 1 Vpk−pk, R_L = 50 Ω, C_L = 0 pF (Both Data Paths)	3.6 V	–	10	–	GHz
$t_{SK(P)}$	Skew of Opposite Transitions of the Same Output (Note 5)	R_{PU} = 50 Ω to V_{DD}, C_L = 0 pF	3.6 V	–	6	–	ps
C_{IN}	Control Pin Input Capacitance (Note 5)	V_{DD} = 0 V, f = 1 MHz		–	2.7	–	pF
C_{ON}	On Capacitance (Note 5)	V_{DD} = 3.3 V, f = 2.5 GHz		–	0.5	–	pF
C_{OFF}	Off Capacitance (Note 5)	V_{DD} = 3.3 V, f = 2.5 GHz		–	0.4	–	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Guaranteed by characterization.

EYE DIAGRAMS

(All plots below are for V_{DD} = 3.6 V and T_A = 25°C with 0 dBm differential data.)

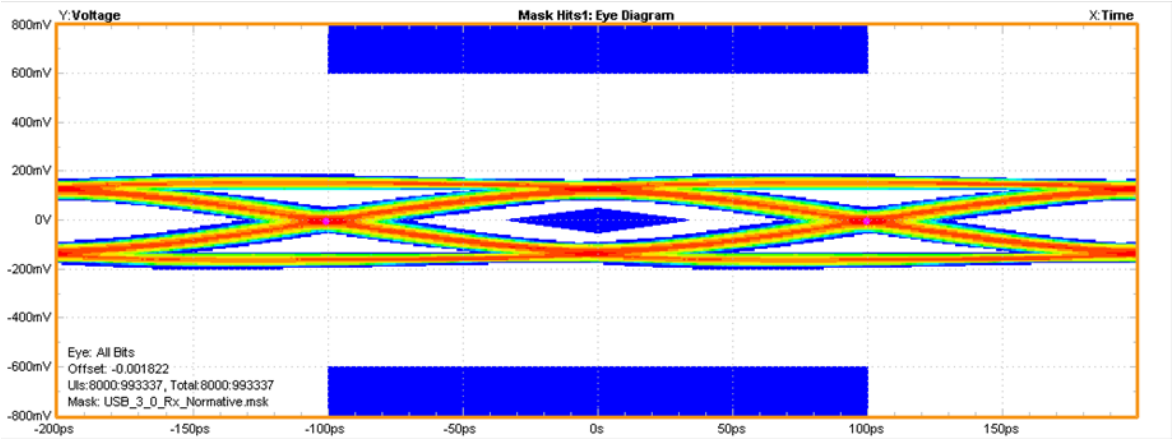


Figure 4. 5 Gbps Eye Diagram with Eye Mask

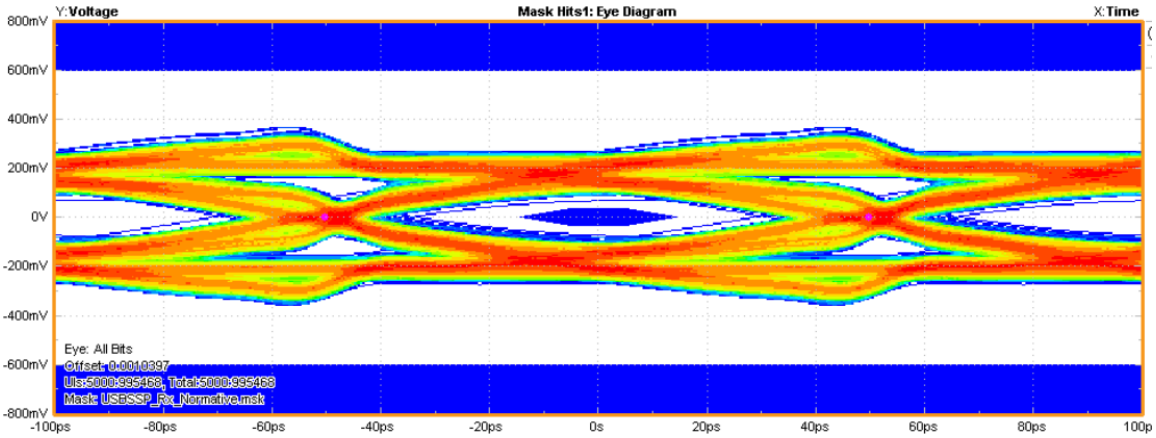


Figure 5. 10 Gbps Eye Diagram with Eye Mask

ORDERING INFORMATION

Part Number	Operating Temperature Range	Package	Shipping†
FUSB340TMX	−40 to +85°C	18−Lead, Quad, Ultra−ultrathin Molded Leadless Package (TMLP), 2.0 mm × 2.8 mm × 0.375 mm	5,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

The table below pertains to the UMLP Package drawing on the following page.

PRODUCT−SPECIFIC DIMENSIONS

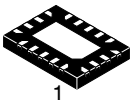
Product	A	B
FUSB340TMX	2.00 mm	2.80 mm

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

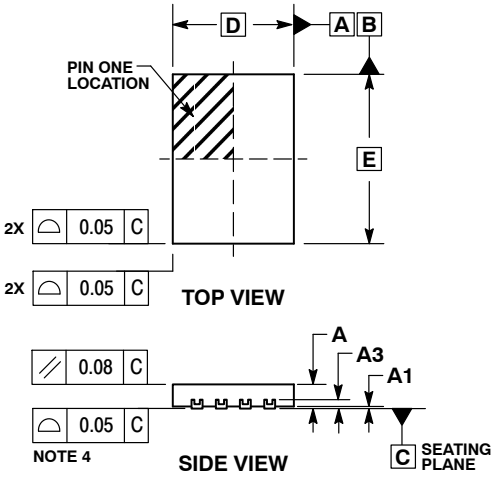
ON Semiconductor®

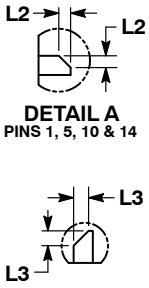
X2QFN18, 2.0x2.8, 0.4P
CASE 722AB
ISSUE O

DATE 17 MAY 2016



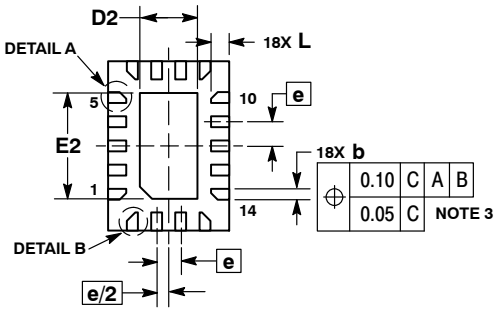
SCALE 4:1



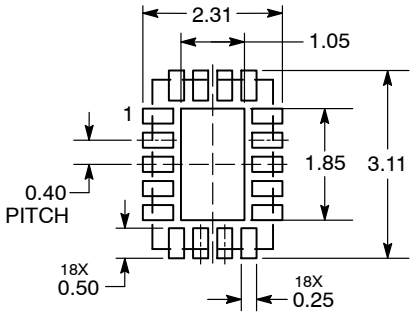


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	---	0.40
A1	0.00	0.05
A3	0.13 REF	
b	0.13	0.23
D	2.00 BSC	
D2	0.90	1.00
E	2.80 BSC	
E2	1.70	1.80
e	0.40 BSC	
L	0.25	0.35
L2	0.11 REF	
L3	0.14 REF	



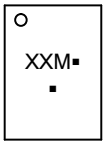
RECOMMENDED MOUNTING FOOTPRINT



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Month Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present.

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DESCRIPTION:	**X2QFN18, 2.0 X 2.8, 0.4P**	**PAGE 1 OF 1**

PUBLICATION ORDERING INFORMATION

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