LM392

Low Power Operational Amplifier and Comparator

The LM392 contains two functions: an op amp and a comparator. Both devices can operate on single−supply power and both have a common−mode range down to ground. Operation from split power supplies is also possible. Low power−supply current is independent of the supply voltage level. The output of the comparator interfaces directly with either TTL or CMOS logic. Low quiescent current makes the LM392 ideal for portable equipment.

Features

- Wide Power−Supply Range: 3 V to 32 V
- Low Input Offset Voltage: 2 mV
- Low Quiescent Current: 600 μA
- Input CMV Range includes GND
- Op Amp is Unity Gain Stable
- These Devices are Pb−Free and are RoHS Compliant

Typical Applications

- Level Detectors
- Voltage Controlled Oscillators
- Transducer Amplifiers

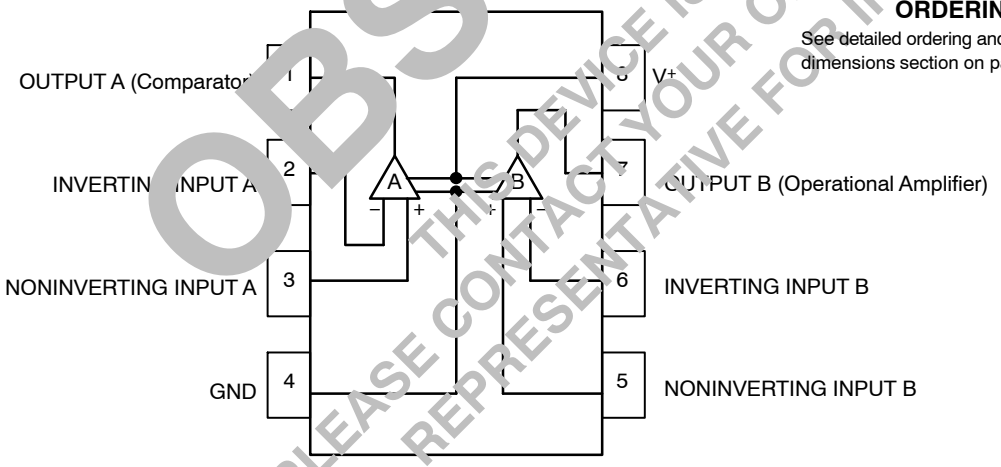


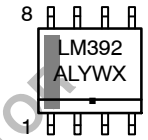
Figure 1. Logic Diagram and Pinout

ON Semiconductor®

http://onsemi.com

SOIC−8 NB
CASE 751

MARKING DIAGRAM



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_S	32 or ±16	V
Differential Input Voltage	V_{IDR}	32	V
Input Voltage	V_I	0.3 to 32	V
Output Short – Circuit to Ground	t_{SO}	Continuous	
Thermal Impedance	θ_{JA}	160	°C/W
Storage Temperature Range	T_{stg}	–65 to 150	°C
Lead Temperature (Soldering, 10 Seconds)		260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

ELECTRICAL CHARACTERISTICS (Both Amplifiers) (V^+ = 5 V, T_A= 25°C unless otherwise stated)

Parameter	Conditions		T_A	LM392 Min	LM392 Typ	LM392 Max	Unit
Input Offset Voltage	At output switch point, V_O = 1.4 V, R_s = 0 Ω, V^+ = 5 V to 30 V, V_{CM} = 0 to (V^+ − 1.5 V)		25°C		±2	±5	mV
			0°C to 70°C			±7	
Input Bias Current	IN(+) or IN(−), V_{CM} = 0 V		25°C		50	205	nA
	IN(+) or IN(−)		0°C to 70°C			400	
Input Offset Current	IN(+) or IN(−)		25°C		±5	±50	nA
			0°C to 70°C			±150	
Input Common−Mode Voltage Range	V^+ = 30 V (Note 1)		25°C	0		V^+−1.5	V
			0°C to 70°C	0		V^+−2	
Supply Current	No Load	V^+ = 30 V	0°C to 70°C		1	2	mA
		V^+ = 5 V			0.5	1	
Amplifier−to−Amplifier Coupling	f = 1 kHz to 20 kHz, Input Referred		25°C		−78		dB
Differential Input Voltage	All $V_{IN} \geq$ V (or V−, If Used)		0°C to 70°C			32	V

ELECTRICAL CHARACTERISTICS (V^+ = 5 V, T_A= 25°C unless otherwise stated)

Parameter	Conditions	T_A	LM392 Min	LM392 Typ	LM392 Max	Unit
OP AMP ONLY						
Large Signal Voltage Gain	V^+ = V, V_o Swing = 1 V to 11 V, R_L = kΩ	25°C		100		V/mV
Output Voltage Swing, High (V_{OH})	R_L = kΩ	25°C	V^+−1.7			V
Output Voltage Swing, Low (V_{OL})	R_L = 2 kΩ	25°C			20	mV
Common−Mode Rejection Ratio	V_{CM} = 0 to V^+ − 1.5 V	25°C	65	70		dB
Power Supply Rejection Ratio		25°C	65	100		dB
Output Current Source	$V_{IN(+)}$ = 1 V, $V_{IN(−)}$ = 0 V, V^+ = 15 V, V_O = 2 V	25°C	20	40		mA
Output Current Sink	$V_{IN(−)}$ = 1 V, $V_{IN(+)}$ = 0 V, V^+ = 15 V, V_O = 2 V	25°C	10	20		mA
	$V_{IN(−)}$ = 1 V, $V_{IN(+)}$ = 0 V, V^+ = 15 V, V_O = 200 mV	25°C	12	50		μA
Input Offset Voltage Drift	R_S = 0 Ω (0°C to 70°C)	0°C to 70°C		7		μV/°C
Input Offset Current Drift	R_S = 0 Ω (0°C to 70°C)	0°C to 70°C		10		pA/°C
COMPARATOR ONLY						
Voltage Gain	$R_L \geq$ 15 kΩ, V^+ = 15 V	25°C	50	200		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, V_{REF} = 1.4 V, V_{RL} = 5 V, R_L = 5.1 kΩ	25°C		200		ns
Response Time	V_{RL} = 5 V, R_L = 5.1 kΩ	25°C		600		ns
Output Sink Current	$V_{IN(−)}$ = 1 V, $V_{IN(+)}$ = 0 V, $V_O \leq$ 1.5 V	25°C	6	16		mA
Saturation Voltage	$V_{IN(−)} \geq$ 1 V, $V_{IN(+)}$ = 0, $I_{SINK} \leq$ 4 mA	25°C		250	400	mV
	$V_{IN(−)} \geq$ 1 V, $V_{IN(+)}$ = 0, $I_{SINK} \leq$ 4 mA	0°C to 70°C			700	mV
Output Leakage Current	$V_{IN(−)}$ = 0, $V_{IN(+)} \geq$ 1 V, V_O = 5 V	25°C		0.1		nA
	$V_{IN(−)}$ = 0, $V_{IN(+)} \geq$ 1 V, V_O = 30 V	25°C			1.0	μA

1. The input common−mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common−mode voltage range is V^+ − 1.5 V, but either or both inputs can go to 32 V without damage.

ORDERING INFORMATION

Device	Operating Temperature Range	Package	Shipping†
LM392DR2G	0°C to +70°C	SOIC−8 (Pb−Free)	2500 / Tape & Reel

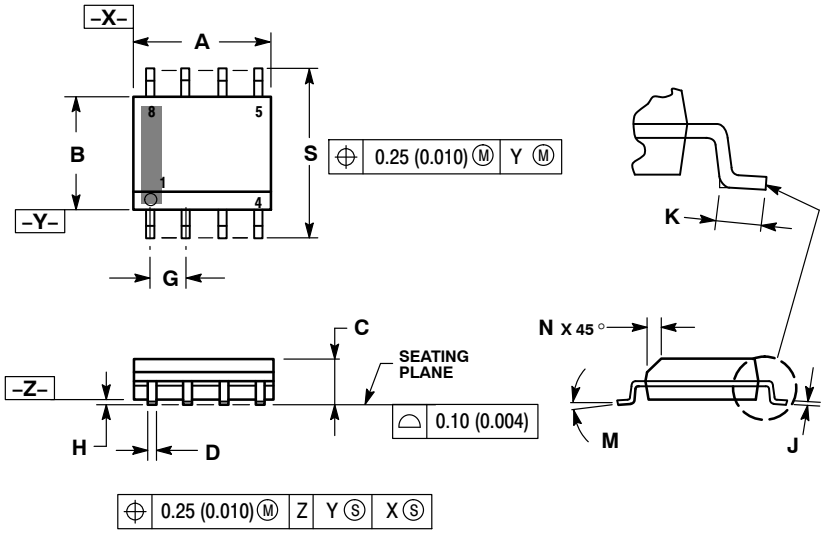
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

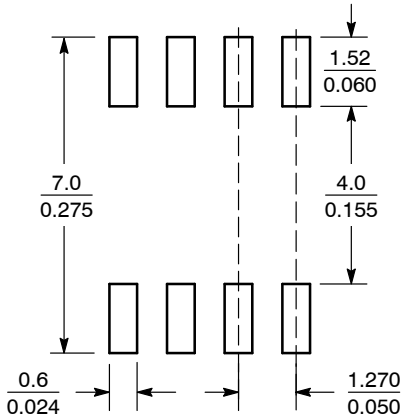
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

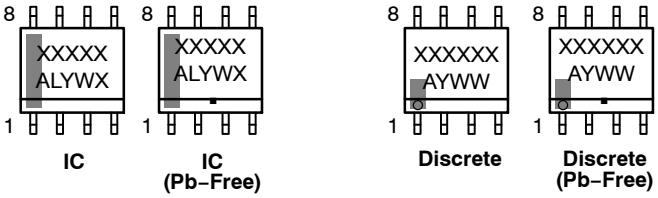
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC | IC (Pb−Free) | Discrete | Discrete (Pb−Free)

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**SOIC−8 NB**	**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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