NCV7361A

Voltage Regulator with Integrated LIN Transceiver

The NCV7361A consists of a low drop voltage regulator, 5.0 V/50 mA and a LIN bus transceiver. The LIN transceiver is suitable for LIN bus systems compatible to "LIN−Protocol Specification" Rev. 1.3, 2.0 and SAE J2602.

The combination of voltage regulator and bus transceiver make it ideal for a powerful and inexpensive cost effective slave node in a LIN Bus system.

Features

- Operating Voltage V_{SUP} = 5.5 to 18 V
- Very Low Standby Current Consumption < 110 μA in Normal Mode (< 50 μA in Sleep Mode)
- LIN−Bus Transceiver:
  - PNP−Bipolar Transistor Driver
  - Slew Rate Control and Wave Shaping for Best EMC Behavior
  - BUS Input Voltage −24 V to 30 V (Independent of V_{SUP})
  - Wake−Up Via LIN Bus
  - Baud Rate up to 20 kBaud
  - Compatible to LIN Specification 1.3, 2.0 and SAE J2602
  - Compatible to ISO9141 Functions
- Wake−Up by LIN BUS and Startup Capable Independent of EN Voltage Level
- Linear Low Drop Voltage Regulator:
  - Output Voltage 5.0 V ±2%
  - Output Current Max. 50 mA
  - Output Current Limit
  - Overtemperature Shutdown
- Reset Time 100 ms and Reset Threshold Voltage 4.65 V
- CMOS Compatible Interface to Microcontroller
- Load Dump Protected (40 V Peak)
- Resistant Against Transient Pulses According to ISO 7637 at Pin V_{SUP}, BUS and EN
- NCV Prefix for Automotive and Other Applications Requiring Site and Change Control

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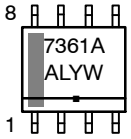
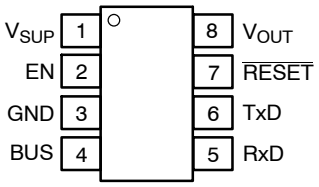
MARKING DIAGRAM

SO−8
D SUFFIX
CASE 751



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCV7361AD	SO−8	98 Units/Rail
NCV7361ADG	SO−8 (Pb−Free)	98 Units/Rail
NCV7361ADR2	SO−8	2500 Tape & Reel
NCV7361ADR2G	SO−8 (Pb−Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

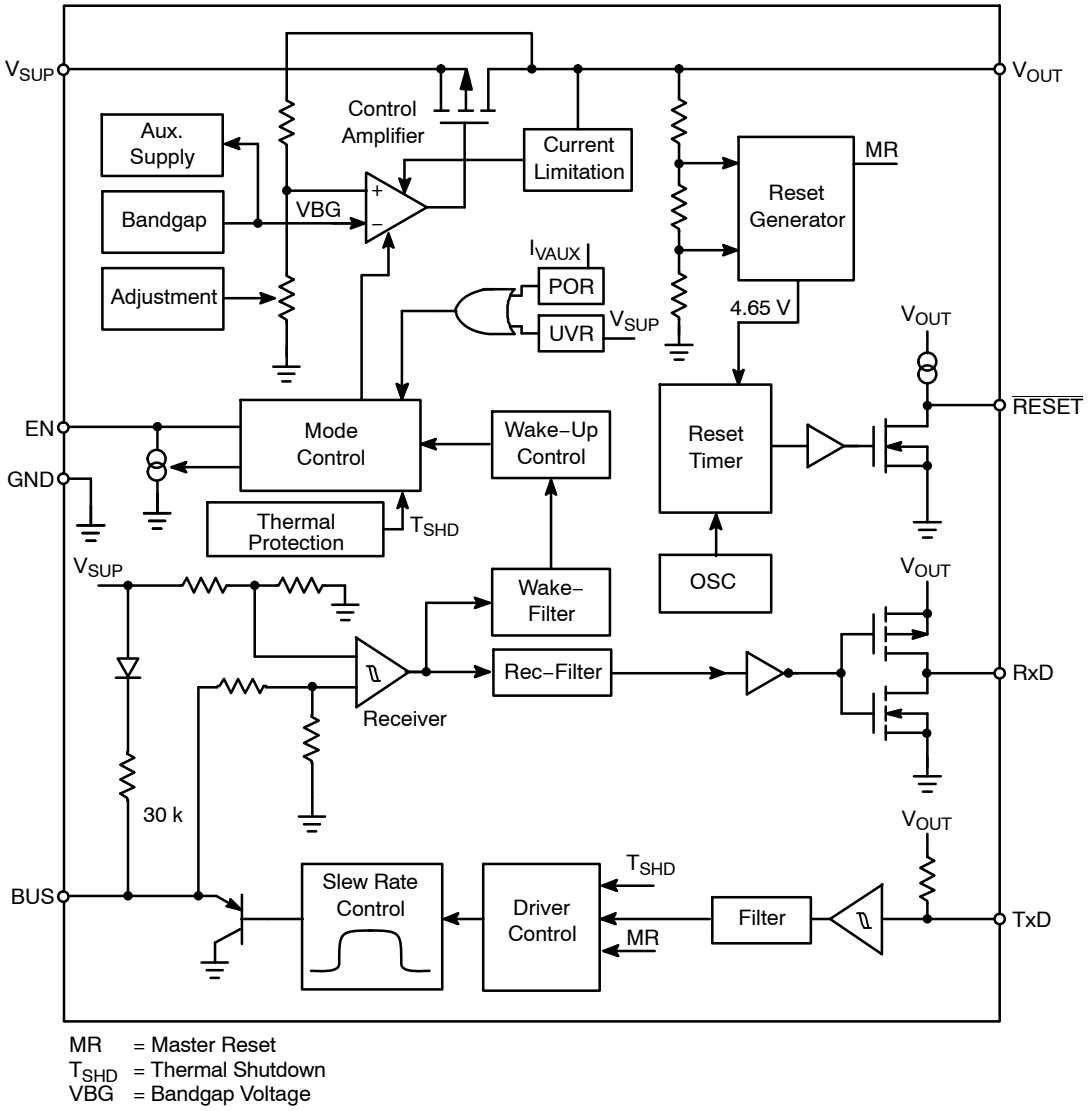


Figure 1. Block Diagram

PACKAGE PIN DESCRIPTION

Pin	Symbol	Description
1	V_{SUP}	Supply voltage.
2	EN	Enable input controls the regulator. Active high.
3	GND	Ground
4	BUS	LIN bus line.
5	RxD	Receive output (push−pull to V_{OUT}).
6	TxD	Transmit input (pullup−input to V_{OUT}).
7	$\overline{RESET}$	Reset output, active low (pullup to V_{OUT}).
8	V_{OUT}	Regulator output 5.0 V/50 mA.

ELECTRICAL SPECIFICATIONS

All voltages are referenced to ground (GND). Positive currents flow into the IC.

The maximum ratings (in accordance with IEC 134) given in the table below are limiting values that do not lead to a permanent damage of the device but exceeding any of these limits may do so. Long term exposure to limiting values may affect the reliability of the device. Correct operating of the device can't be guaranteed if any of these limits are exceeded.

OPERATING CONDITIONS

Characteristic	Symbol	Min	Max	Unit
Supply Voltage	V_{SUP}	5.25	18	V
Operating Ambient Temperature	T_A	−40	+125	°C
Junction Temperature	T_J	−	+150	°C

MAXIMUM RATINGS

Rating	Symbol	Condition	Min	Max	Unit
V_{SUP}	V_{SUP}	−	−1.0	30	V
		T ≤ 500 ms	−	40	
BUS	V_{BUS}	−	−24	30	V
		T ≤ 500 ms	−	40	
Difference V_{SUP}−V_{OUT}	V_{SUP}−V_{OUT}	−	−0.3	40	V
EN	V_{INEN}	−	−0.3	V_{SUP} + 0.3	V
TxD, RxD, $\overline{\text{RESET}}$	V_{IN}	−	−0.3	V_{OUT} + 0.3	V
EN, TxD, RxD, $\overline{\text{RESET}}$	I_{IN}	−	−25	25	mA
Short Circuit of Pin V_{SUP} and V_{OUT}	I_{INSH}	−	−500	500	mA
ESD Capability − All Pins	ESD_{HB}	Human Body Model, 100 pF via 1.5 kΩ	−2.0	2.0	kV
Junction Temperature	T_J	−	−	150	°C
Storage Temperature	T_{STG}	−	−55	150	°C
Lead Temperature Soldering Reflow: (SMD styles only)	T_{sld}	60 second maximum above 183°C −5°C/+0°C allowable conditions	−	240 peak	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

THERMAL RATINGS

Parameter	Test Conditions Typical Value		Units
SO−8 Package	**Min−Pad Board** (Note 1)	**1.0 in Pad Board** (Note 2)	
Junction−to−Tab (psi−JL2, Ψ_{JL2}) (Note 3)	48	43	°C/W
Junction−to−Ambient ($R_{\theta JA}$, θ_{JA})	183	120	°C/W

1. 1 oz copper, 54 mm^2 copper area, 0.062" thick FR4.
2. 1 oz copper, 714 mm^2 copper area, 0.062" thick FR4.
3. psi−JL2 temperature was made at foot of lead #2.

ELECTRICAL CHARACTERISTICS (5.25 V ≤ V_{SUP} ≤ 18 V, −40°C ≤ T_A ≤ 125°C unless otherwise noted)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
V_{SUP}						
Supply Current with V_{OUT} "No Load" (Note 4)	I_{SnI}	V_{EN} = V_{SUP} = 12 V, V_{BUS} > V_{SUP} − 0.5 V, Pins 5 to 8 Open	–	–	110	μA
Supply Current, "Sleep Mode"	I_{Ssleep}	V_{SUP} = 12 V, V_{EN} = 0 V, V_{BUS} > V_{SUP} − 0.5 V	–	35	50	μA
Thermal Shutdown (Note 5)	T_{JSHD}	–	155	–	175	°C
Thermal Recovery (Note 5)	T_{Jrec}	–	126	–	130	°C
V_{SUP} Undervoltage Reset "OFF"	V_{SUVR_OFF}	V_{SUP} Ramp Up	–	3.5	3.9	V
V_{SUP} Undervoltage Reset "ON"	V_{SUVR_ON}	V_{SUP} Ramp Down	–	3.0	3.3	V
V_{SUP} Undervoltage Hysteresis	V_{SUVR_HYS}	V_{SUVR_OFF} − V_{SUVR_ON}	0.2	–	–	V
Operating Voltage	V_{SUP}		5.25	12	18	V
V_{OUT}						
Output Voltage	V_{OUTt}	5.5 V ≤ V_{SUP} ≤ 18 V 0 < I_{OUT} < 50 mA	4.90	5.0	5.10	V
	V_{OUTh}	V_{SUP} > 18 V	4.90	5.0	5.25	V
	V_{OUTl}	IV_{OUT} = 20 mA, V_{SUP} = 3.3 V	–	V_{SUP}−V_D	–	V
		IV_{OUT} = 50 mA, V_{SUP} = 3.3 V	–	V_{SUP}−V_D	–	V
Drop−Out Voltage (Note 6) V_D = V_{SUP}−V_{OUT}	V_D	IV_{OUT} = 20 mA	–	–	150	mV
		IV_{OUT} = 50 mA	–	–	500	mV
Output Current	IV_{OUT}	3.0 V < V_{SUP} < 18 V V_{OUT} = 0 V	50	–	150	mA
Load Capacity	C_{load}	Reference Figure 35	4.7	–	–	μF
ENABLE (EN)						
Input Voltage Low	V_{ENL}	–	−0.3	–	1.6	V
Input Voltage High	V_{ENH}	–	2.5	–	V_{SUP} +0.3	V
Hysteresis (Note 5)	V_{ENHYS}	–	100	–	–	mV
Pulldown Current	I_{pdEN}	V_{EN} > V_{ENH}	1.0	4.0	7.0	μA
		V_{EN} < V_{ENL}	70	100	130	μA
$\overline{\text{RESET}}$						
Output Voltage Low	V_{OL}	I_{OUT} = 1.0 mA, V_{SUP} > 5.5 V	–	–	0.8	V
		10 kΩ $\overline{\text{RESET}}$ to V_{OUT} V_{SUP} = V_{OUT} = 0.8 V	–	–	0.2	V
Pullup Current	I_{pu}	–	−500	−375	−250	μA
$\overline{\text{RESET}}$ Threshold	V_{RES}	Referred to V_{OUT}, V_{SUP} > 4.6 V	4.5	4.65	4.8	V
Master Reset Threshold (Note 5)	V_{MRes}	–	3.0	3.15	3.3	V

4. See Figure 6 for test setup.
5. Not production tested, guaranteed by design and qualification.
6. Measured when the output voltage has dropped 100 mV from the V_{SUP} = 12 V nominal value.

ELECTRICAL CHARACTERISTICS (5.25 V ≤ V_{SUP} ≤ 18 V, −40°C ≤ T_A ≤ 125°C unless otherwise noted)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
LIN BUS INTERFACE						
Receive Threshold	V_{thr_rec}, V_{thr_dom}	7.0 V ≤ V_{SUP} ≤ 18 V	0.4 *V_{SUP}	–	0.6 *V_{SUP}	V
Receive Center Point V_{thr_cnt} = (V_{thr_rec} + V_{thr_dom})/2	V_{thr_cnt}		0.475 *V_{SUP}	0.5 *V_{SUP}	0.525 *V_{SUP}	
Receive Hysteresis V_{thr_hys} = V_{thr_rec} − V_{thr_dom}	V_{thr_hys}		0.12 *V_{SUP}	0.135 *V_{SUP}	0.15 *V_{SUP}	
BUS Input Current (Recessive) (Note 7)	I_{INBUSR}	8.0 ≤ V_{BUS} ≤ 18 V, V_{SUP} = V_{BUS} − 0.7 V, TxD = 4.5 V	–	–	20	μA
BUS Input Current (Recessive)	$-I_{INBUSR}$	V_{SUP} = 0 V, V_{BUS} = −12 V	−1.0	–	–	mA
BUS Input Current (Recessive)	$-I_{INBUSR}$	V_{SUP} = Open, V_{BUS} = −18 V	−1.0	–	–	mA
BUS Pullup Resistor	R_{BUSpu}	–	20	30	47	kΩ
BUS Output Voltage (Dominant) (Note 7)	V_{BUSdom}	7.0 ≤ V_{SUP} ≤ 18 V, TxD = 0 V, R_L = 500 Ω	–	–	1.2	V
BUS Output Voltage (Recessive) (Notes 7 and 8)	V_{BUSrec}	7.0 ≤ V_{SUP} ≤ 18 V, TxD = 4.5 V	0.8 *V_{SUP}	–	–	V
BUS Current Limit	I_{LIM}	V_{BUS} > 2.5 V, TxD = 0 V	40	–	120	mA
TxD						
Pullup Resistance	R_{pu_TxD}	–	9.5	15	21	kΩ
Input Low Level	V_{IL}	–	–	–	1.25	V
Input High Level	V_{IH}	–	3.75	–	–	V
RxD						
Output Voltage Low	V_{OL}	I_{OUT} = 1.0 mA	–	–	0.8	V
Output Voltage High	V_{OH}	I_{OUT} = −1.0 mA	4.2	–	–	V

7. See Figures 7, 8, and 9 for test setup.
8. The recessive voltage on BUS should not be less than 80% direct battery. The LIN specification requires an external reverse battery diode between the battery and V_{SUP}. V_{SUP} = V_{BAT} −0.7 V.

ELECTRICAL CHARACTERISTICS (7.0 V ≤ V_{SUP} ≤ 18 V, −40°C ≤ T_A ≤ 125°C unless otherwise noted)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
$\overline{\text{RESET}}$ AC CHARACTERISTICS						
Reset Time	t_{Res}	–	50	100	140	ms
Reset Rise Time (Note 9)	t_{rr}	–	3.0	7.5	15	μs
BUS Debounce Time (Note 14)	t_{deb_BUS}	–	1.5	2.8	4.0	μs
Wake−Up Time	t_{Wake_BUS}	–	25	60	120	μs
GENERAL LIN BUS INTERFACE AC CHARACTERISTICS						
Transmit Propagation Delay TxD −> BUS (Notes 10 and 11)	t_{dr_TxD}, t_{df_TxD}	R_L/C_L at BUS 1.0 kΩ/1.0 nF 660 Ω/6.8 nF 500 Ω/10 nF V_{SUPMIN} = 8 V	–	–	4.0	μs
Symmetry of Propagation Delay BUS −> RxD (Note 10)	t_{dsym_TxD}	$t_{dr\_TxD} - t_{df\_TxD}$ V_{SUPMIN} = 8 V	−2.0	–	2.0	μs
Receiver Propagation Delay BUS −> RxD (Notes 10 and 11)	t_{dr_RxD} t_{df_RxD}	$C_{L(RxD)}$ = 50 pF V_{SUPMIN} = 8 V	–	–	6.0	μs
Symmetry of Propagation Delay TxD −> BUS (Note 10)	t_{dsym_RxD}	$t_{dr\_RxD} - t_{df\_RxD}$ V_{SUPMIN} = 8 V	−2.0	–	2.0	μs
Slew Rate BUS Rising Edge (Note 9)	dV/dT_{rise}	20% ≤ V_{BUS} ≤ 80% C_L = 1.0 nF, R_L = 1.0 kΩ V_{SUPMIN} = 8 V	1.0	1.7	2.5	V/μs
Slew Rate BUS Falling Edge (Note 9)	dV/dT_{fall}	20% ≤ V_{BUS} ≤ 80% C_L = 1.0 nF, R_L = 1.0 kΩ V_{SUPMIN} = 8 V	−2.5	−1.7	−1.0	V/μs
LIN BUS PARAMETER ACCORDING TO LIN SPEC. REV. 1.3						
Slope Time, Transition from Recessive to Dominant (Notes 11 and 12)	t_{sdom}	V_{SUP} = 8.0 V R_L = 500 Ω/C_L = 10 nF	–	–	12	μs
Slope Time, Transition from Dominant to Recessive (Notes 11 and 13)	t_{srec}	V_{SUP} = 8.0 V R_L = 500 Ω/C_L = 10 nF	–	–	12	μs
Slope Time Symmetry	t_{ssym}	V_{SUP} = 8.0 V R_L = 500 Ω/C_L = 10 nF $T_{ssym} = t_{sdom} - t_{srec}$	−7.0	–	1.0	μs
Slope Time, Transition from Recessive to Dominant (Notes 11 and 12)	t_{sdom}	V_{SUP} = 18 V R_L = 500 Ω/C_L = 10 nF	–	–	18	μs
Slope Time, Transition from Dominant to Recessive (Notes 11 and 13)	t_{srec}	V_{SUP} = 18 V R_L = 500 Ω/C_L = 10 nF	–	–	18	μs
Slope Time Symmetry	t_{ssym}	V_{SUP} = 18 V R_L = 500 Ω/C_L = 10 nF $T_{ssym} = t_{sdom} - t_{srec}$	−5.0	–	5.0	μs

9. Not production tested, guaranteed by design and qualification.
10. See Figures 2 and 3, Timing Diagrams.
11. See Figures 5, 6, 7, 8, and 9 for test setup.
12. $t_{sdom} = (t_{VBUS40\%} - t_{VBUS95\%}) / 0.55$.
13. $t_{sdom} = (t_{VBUS60\%} - t_{VBUS5\%}) / 0.55$.
14. See Figure 18.

ELECTRICAL CHARACTERISTICS (V_{SUP} = 7.0 V to 18 V; BUS loads: 1.0 k / 1 nF; 660 / 6.8 nF; 500 / 10 nF, T_{xD} Signal: t_{Bit} = 50 μs, $t_{wH} = T_{wL} = t_{Bit}$; $t_{rise} = t_{fall}$ < 100 ns, −40°C ≤ T_A ≤ 125°C unless otherwise noted)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
LIN BUS PARAMETER ACCORDING TO LIN SPEC. REV. 2.0						
Minimal Recessive Bit Time (Notes 15 and 16)	$t_{rec(min)}$	–	40	50	58	μs
Maximum Recessive Bit Time (Notes 15 and 16)	$t_{rec(max)}$	–	40	50	58	μs
Duty Cycle 1	D_1	$D_1 = t_{rec(min)} / (2 * t_{Bit})$	0.396	–	–	
Duty Cycle 2	D_2	$D_2 = t_{rec(max)} / (2 * t_{Bit})$	–	–	0.581	

15. See Timing Diagrams.
16. See Test Circuits for Dynamic and Static Characteristics.

TIMING DIAGRAMS

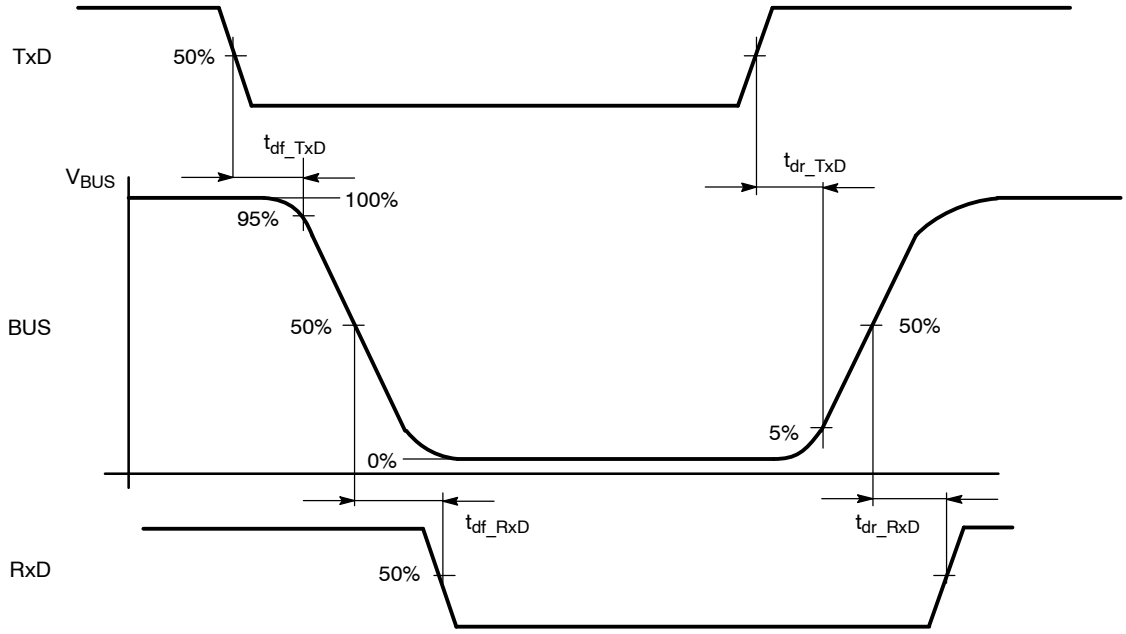


Figure 2. Timing Diagram for Propagation Delay According to LIN 1.3 and 2.0

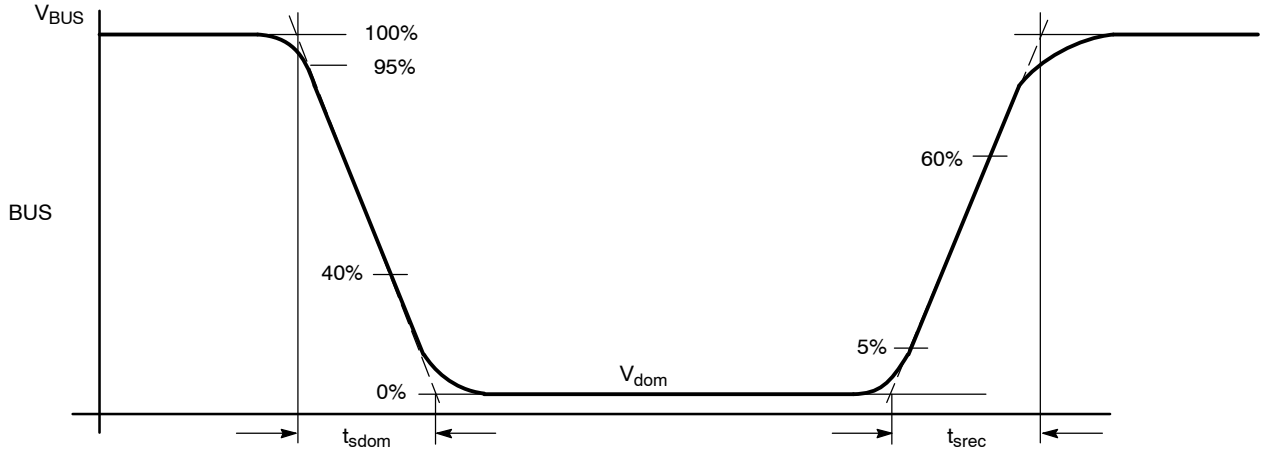


Figure 3. Timing Diagram for Slope Times According to LIN 1.3

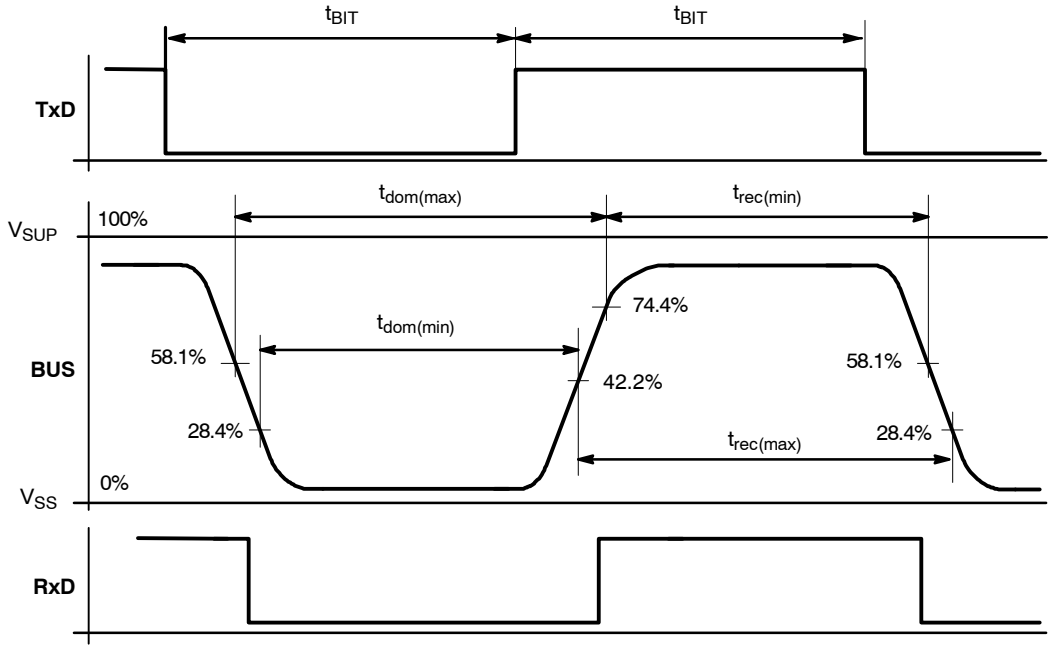


Figure 4. Timing Diagram for Duty Cycle According to LIN 2.0

TEST CIRCUITS

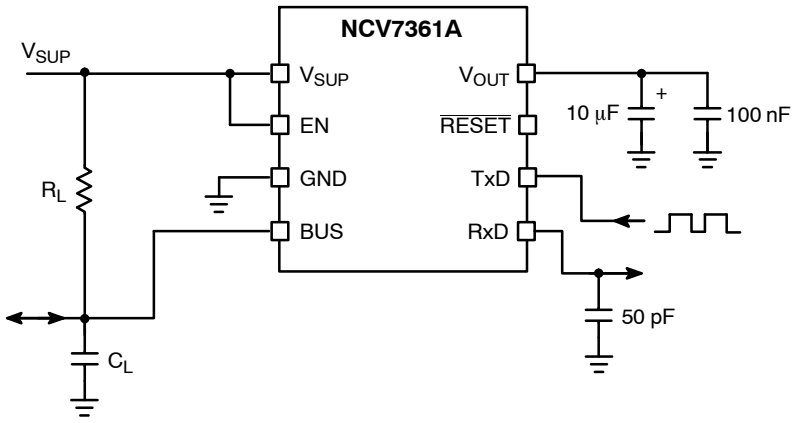


Figure 5. Test Circuit for Delay Time, Slope Time, and Duty Cycle

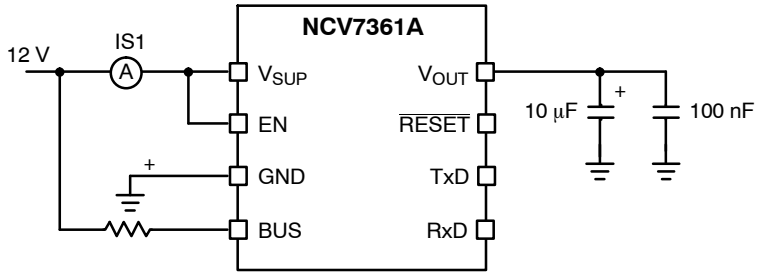


Figure 6. Test Circuit for Supply Current I_{SnI}

TEST CIRCUITS (continued)

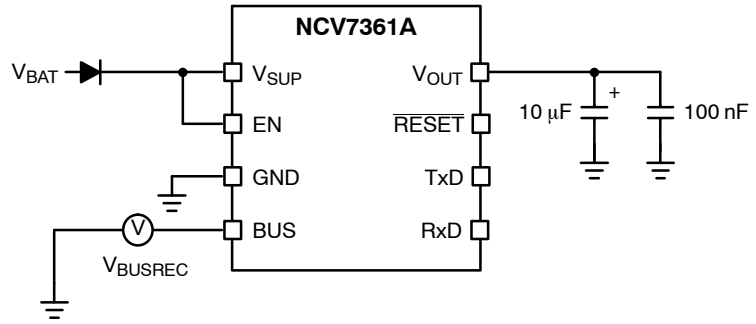


Figure 7. Test Circuit for Bus Voltage "Recessive" (V_{BUSREC})

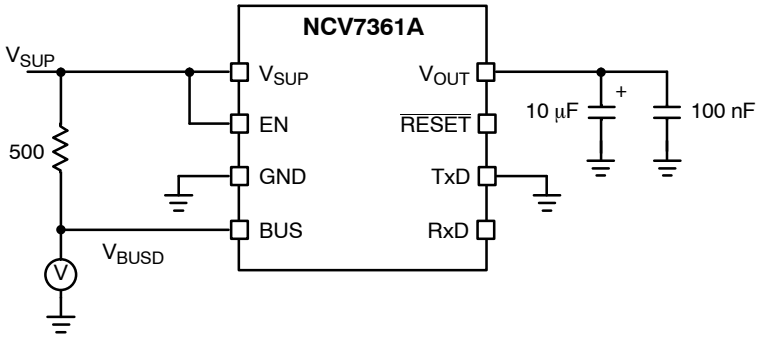


Figure 8. Test Circuit for Bus Voltage "Dominant" V_{BUSDOM}

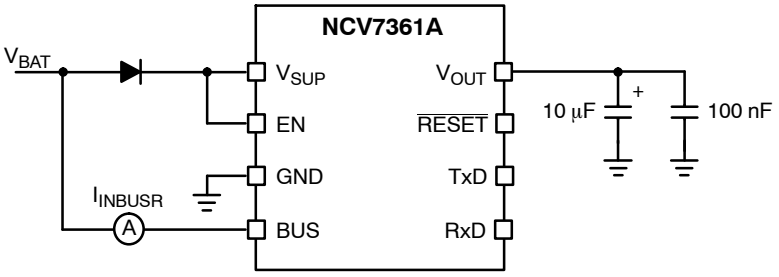


Figure 9. Test Circuit for Bus Current "Recessive" I_{INBUSR}

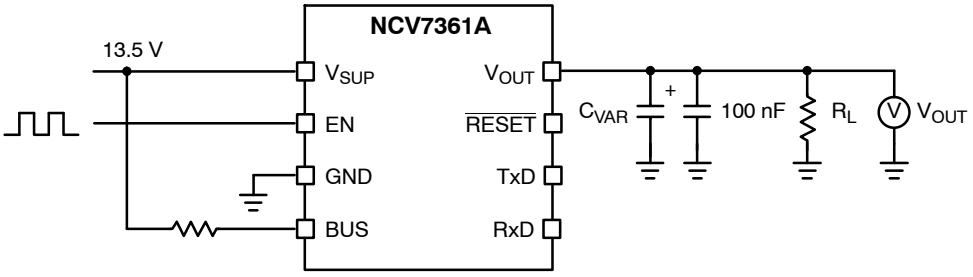


Figure 10. Test Circuit for V_{OUT} Rise Time vs. Load Capacitance and Resistance

TYPICAL OPERATING CHARACTERISTICS

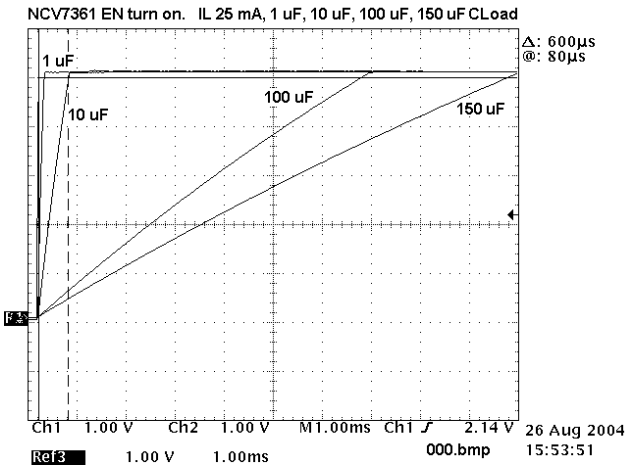


Figure 11. V_{out} Rise Time with 1 μF, 10 μF, 100 μF, and 150 μF Capacitors and 200 Ω Load using EN to Enable the Output.

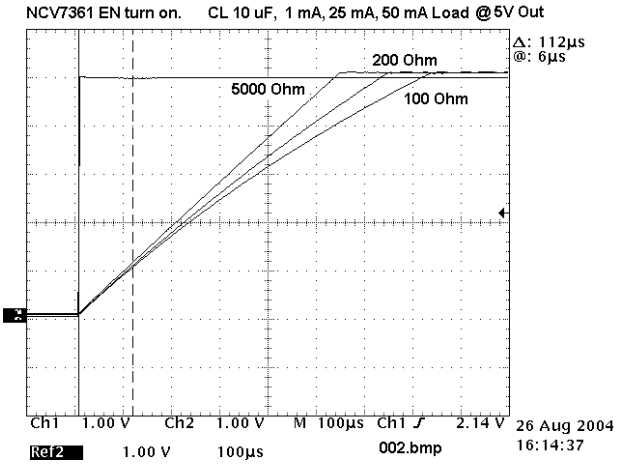


Figure 12. V_{out} Rise Time with a 10 μF Load Capacitor and 1 kΩ, 200 Ω, and 100 Ω Load using EN to Enable the Output.

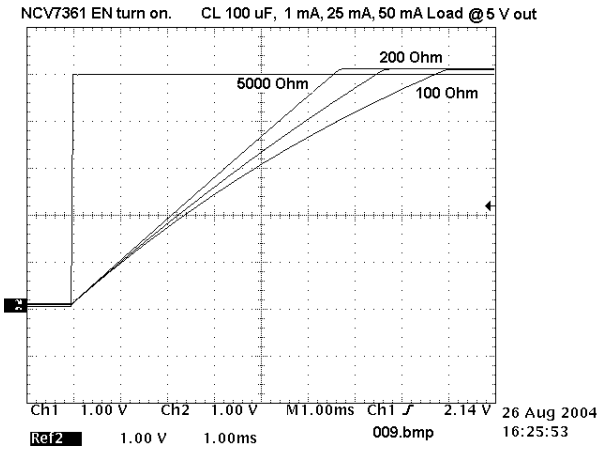


Figure 13. V_{out} Rise Time with a 100 μF Load Capacitor and 1 kΩ, 200 Ω, and 100 Ω Load using EN to Enable the Output.

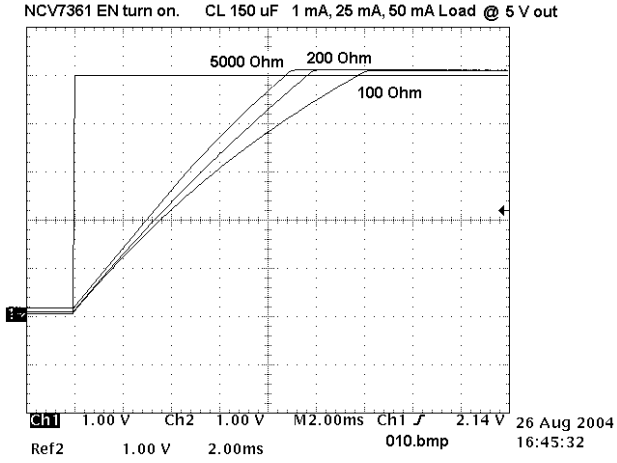


Figure 14. V_{out} Rise Time with a 150 μF Load Capacitor and 1 kΩ, 200 Ω, and 100 Ω Load using EN to Enable the Output.

FUNCTIONAL DESCRIPTION

The NCV7361A consists of a low drop voltage regulator 5.0 V/50 mA and a LIN Bus transceiver, which is a bidirectional bus interface for data transfer between the LIN bus and the LIN protocol controller.

Additionally, the NCV7361A features a $\overline{\text{RESET}}$ output with a reset delay of 100 ms and a fixed threshold of 4.65 V and Enable (EN) control for the regulator.

Operating Modes

The NCV7361A provides two main operating modes “normal” and “sleep” and the intermediate states “POR”, “Ini−state” and “thermal shutdown”. The main modes are fixed states defined by basic actions (V_{SUP} start, EN or wake−up). The intermediate states are soft states. They aren’t defined by logical actions but by changes of voltage (V_{SUP}, V_{OUT}) or junction temperature.

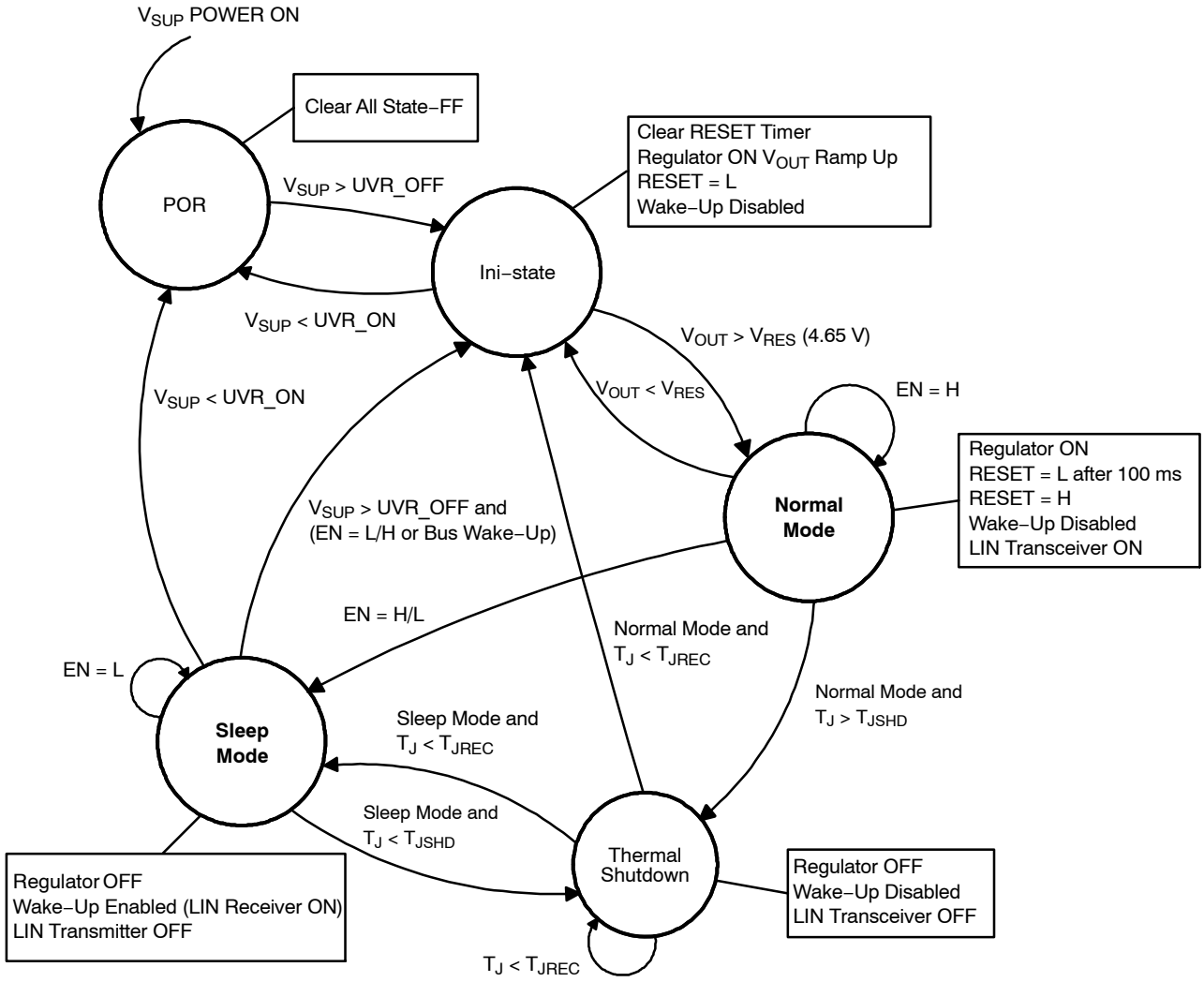


Figure 15. State Diagram of Operating Modes

Normal Mode

The whole NCV7361A is active. Switching to normal mode can be done via the following actions:

- Start of V_{SUP} or after Undervoltage Reset
- Rising Edge at EN (EN = High) (Local Wake−Up)
- Activity on the LIN Bus (Remote Wake−Up)

Sleep Mode

Sleep mode is most current saving. With a falling edge on EN (EN = Low) the NCV7361A is switched from normal mode into sleep mode. The voltage regulator will be switched off and the LIN transceiver is in recessive state.

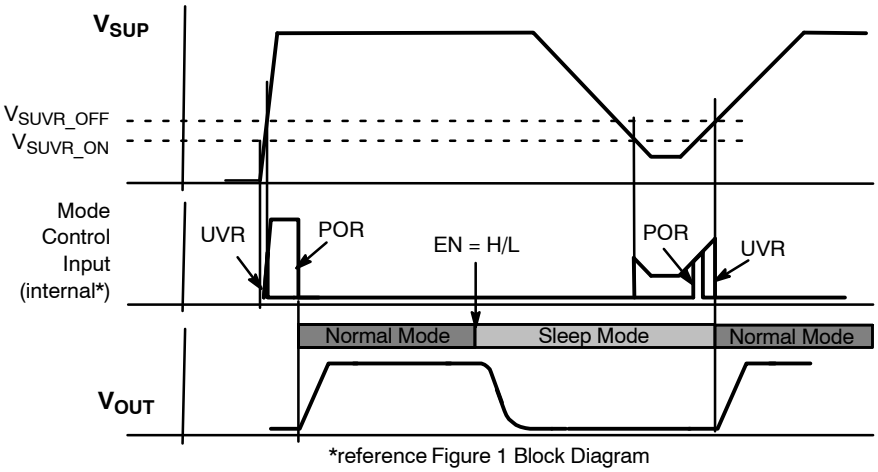


Figure 16. Operating of Power On and Undervoltage RESET

Switching into sleep mode can be done independently from the current transceiver state. That means if the transmitter is in dominant state this state will be cancelled and it will be switched to recessive state.

POR−state

This is the power−on−reset state of the NCV7361A, while $V_{SUP} < V_{SUVR\_OFF}$. If the prior state was sleep mode, the NCV7361A switches via the Ini−state to normal mode.

Ini−state

This is an intermediate state, which will pass through after switch−on of V_{SUP} or V_{OUT}. The NCV7361A remains in this state if V_{OUT} is below V_{RES} (Reset Output = L) and $V_{SUP} > V_{SUVR\_ON}$.

Thermal Shutdown

If the junction temperature T_J is higher than T_{JSHD} (>155°C), the NCV7361A will be switched into the thermal shutdown mode. The behavior within this mode is comparable with the sleep mode except for LIN transceiver operating. The transceiver is completely disabled, no wake−up functionality is available.

If T_J falls below the thermal recovery temperature T_{JREC} (typical 140°C) the NCV7361A will be recover to the previous state (normal or sleep).

Initialization

Initialization is started if the power supply is switched on as well as every rising edge on of the NCV7361A via the EN pin.

V_{SUP} − Power On

If V_{SUP} is switched on the NCV7361A starts to normal mode via the POR− and Ini−state. A combination of dynamic POR and undervoltage reset circuitry generates a POR signal, which switches the NCV7361A into normal mode. This power on behavior is independent from the status of the EN pin.

Power−on−Reset and undervoltage reset operates independent from each other, which secures the independence from the rise time of V_{SUP}. During fast V_{SUP} edges the Power−on−Reset will be active. If the increasing of V_{SUP} is very slow (> 1 ms/V) the undervoltage reset unit initializes the voltage regulator if $V_{SUP} > V_{SUVR\_OFF}$ (typical 3.5 V).

The effects of both POR circuits at different V_{SUP} slopes as shown in Figure 16.

After POR the voltage regulator starts and V_{OUT} will be output. If $V_{OUT} > V_{MRes}$ the bus interface will be activated. If the V_{OUT} voltage level is higher than V_{RES}, the reset time t_{Res} = 100 ms is started. After t_{Res} the RESET output switches from low to high (Figure 16).

Start of Linear Regulator via Wake−Up

The initialization is only being done for the V_{OUT} circuitry parts. This procedure begins with leaving the master reset state ($V_{OUT} > V_{MRes}$) and runs in the same manner as the V_{SUP} − Power−On.

Wake−Up

If the regulator is put into sleep mode it can be “waked−up” with the BUS interface. Every pulse on the BUS (high pulse or low pulse) with a pulse width of minimum 60 μs switches on the regulator.

After the BUS has “waked−up” the regulator, it can only be switched off with a high level followed by a low level on the EN pin.

V_{SUP} Undervoltage Reset

The undervoltage detection unit inhibit an undefined behavior of the NCV7361A under low voltage condition. If V_{SUP} drops below V_{SUVR_ON} (typical 3 V) the undervoltage detection becomes active and the IC will be switched to POR state. The following increasing of V_{SUP} above V_{SUVR_OFF} (typical 3.5 V) cancels this POR state and the voltage regulator starts with the initialization sequence.

V_{SUP} Undervoltage in Normal Mode

Supply Voltages below V_{SUVR_OFF} do not influence the voltage regulator. The output voltage V_{OUT} follows V_{SUP}.

V_{SUP} Undervoltage in Sleep Mode

No exit from the sleep mode will take place if the V_{SUP} voltage drops down to V_{SUVR_ON} (typical 3.0 V). The undervoltage reset becomes active (POR−state). As a result of this operating, the sleep mode is left to the normal mode. If V_{SUP} rises again above V_{SUVR_OFF} (typical 3.5 V), the IC initializes the voltage regulator and continues to work with the normal mode.

The undervoltage reset unit secures stable operating in the undervoltage range of V_{SUP} down to GND level. The dynamic Power−On−Reset secures a defined internal state independent from the duration of the V_{SUP} drop, which secures a stable restart.

Overtemperature Shutdown

If the junction temperature is 155°C < T_J < 170°C the overtemperature recognition will be activated and the regulator voltage will be switched off. The V_{OUT} voltage drops down, the reset state is entered and the bus−transceiver is switched off (recessive state).

After T_J falls below 140°C the NCV7361A will be initialized again (Figure 17) independently from the voltage levels on EN and BUS. Within the thermal shutdown mode the transceiver can not be switched to the normal mode neither with local nor with remote wake−up.

The operation of the NCV7361A is possible between T_{Amax} (125°C) and the switch−off temperature, but small parameter differences can appear.

After overtemperature switch−off the IC behaves as described in Figure 17.

LIN BUS Transceiver

The NCV7361A is a bidirectional bus interface device for data transfer between the LIN bus and the LIN protocol controller.

The transceiver consists of a pnp−driver (1.2 V @ 40 mA) with slew rate control, wave shaping and current limit, and a high voltage receiver/comparator followed by a filter circuit.

Transmit Mode

During transmission the data at the TxD pin will be transferred to the BUS driver for generating a BUS signal. To minimize the electromagnetic emission of the bus line, the BUS driver has integrated slew rate control and wave shaping circuitry.

Transmitting will be interrupted in the following cases:

- Sleep Mode
- Thermal Shutdown Active
- Master Reset (V_{OUT} < 3.15 V)

The recessive BUS level is generated from the integrated 30 k pullup resistor in series with a diode This diode prevents reverse current on V_{BUS} when V_{BUS} > V_{SUP}.

No additional termination resistor is necessary to use the NCV7361A in LIN slave nodes. If this IC is used for LIN master nodes, it is necessary to terminate the bus pin with an external 1.0 kΩ resistor in series with a diode to V_{BAT}.

Receive Mode

The data signal from the BUS pin will be transferred continuously to the pin RxD. Short spikes on the bus are suppressed by the internal filter circuit (τ = 2.8 μs).

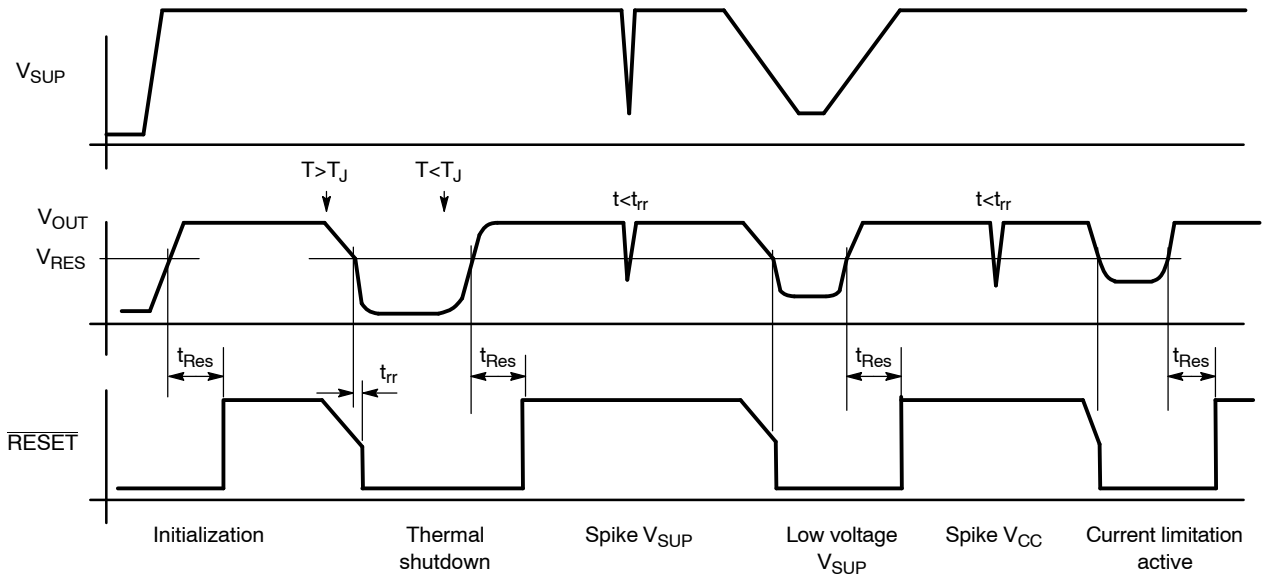


Figure 17. $\overline{\text{RESET}}$ Behavior

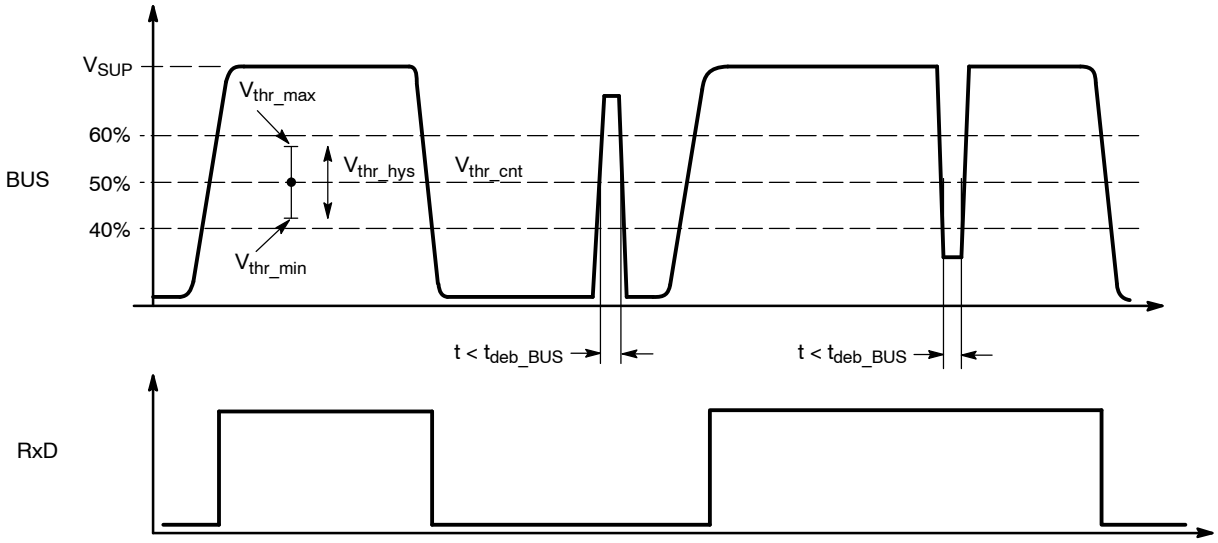


Figure 18. Receive Mode Impulse Diagram

The receive threshold values V_{thr_max} and V_{thr_min} are symmetrical to $0.5*V_{SUP}$ with a hysteresis of $0.135*V_{SUP}$. The LIN specific receive threshold is between $0.4*V_{SUP}$ and $0.6 * V_{SUP}$.

Data Rate

The NCV7361A is a *constant slew rate* transceiver. The bus driver works with a fixed slew rate range of 1.0 V/μs $\leq \Delta V/\Delta T \leq$ 2.5 V/μs. This principle provides good symmetry of the slope times between recessive to dominant and dominant to recessive slopes within the LIN bus load range (C_{BUS}, R_{term}).

The NCV7361A guarantees data rates up to 20 kb within the complete bus load range under worst case conditions. The constant slew rate principle holds appropriate voltage levels and can operate within the LIN Protocol Specification for RC oscillator systems with a matching tolerance up to ±2% between 2 nodes.

TxD Input

The 5.0 V input TxD directly controls the BUS level:

TxD = low → BUS = low (dominant level)

TxD = high → BUS = high (recessive level)

The TxD pin has an internal pullup resistor connected to V_{OUT}. This guarantees that an open TxD pin generates a recessive BUS level.

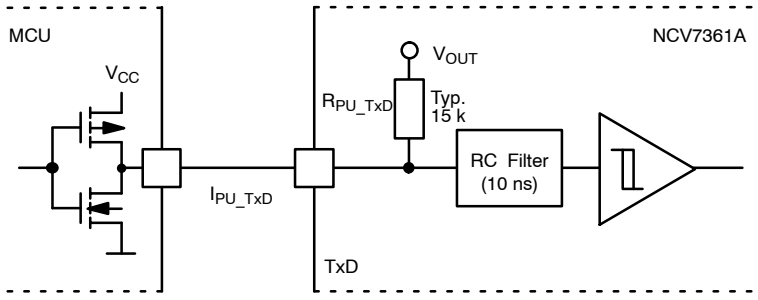


Figure 19. TxD Input Circuitry

RxD Output

The received BUS signal will be output to the 5.0 V RxD pin:

$BUS < V_{thr\_cnt} - 0.5 * V_{thr\_hys} \rightarrow RxD = low$

$BUS > V_{thr\_cnt} + 0.5 * V_{thr\_hys} \rightarrow RxD = high$

This output is a push−pull driver between V_{OUT} and GND with an output current capability of 1.0 mA.

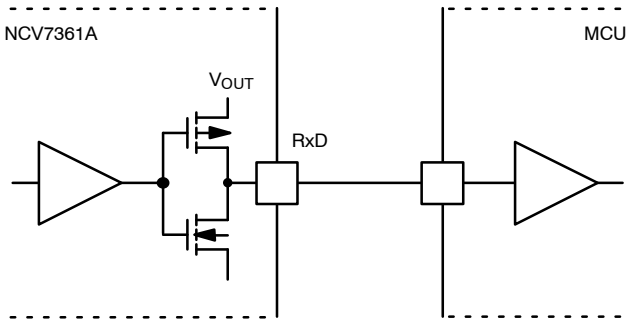


Figure 20. RxD Output Circuitry

Linear Regulator

The NCV7361A has an integrated low dropout linear regulator with a P−Channel MOSFET output driver whose output is 5.0 V ±2% at ≤50 mA and 5.5 V ≤ V_{SUP} ≤ 18 V. Figure 21 shows typical current limit based on the output voltage.

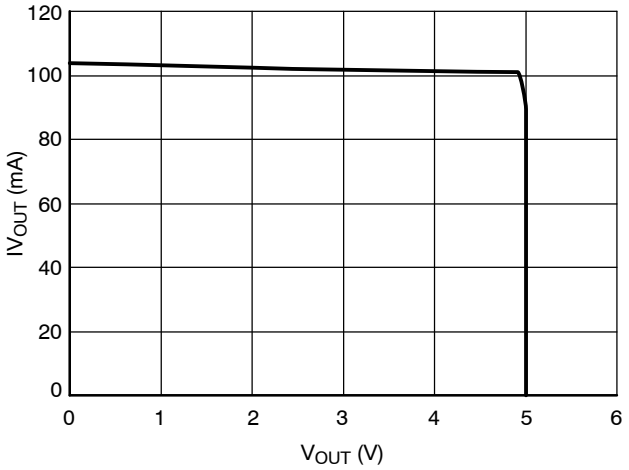


Figure 21. Characteristic of Current Limit vs. Output Voltage

$\overline{\text{RESET}}$

$\overline{\text{RESET}}$ switches from low to high if V_{SUP} is switched on and $V_{OUT} > V_{RES}$ for t_{Res}.

If V_{OUT} drops below V_{RES}, the $\overline{\text{RESET}}$ output goes from high to low after t_{rr}. Short transients will be filtered.

The $\overline{\text{RESET}}$ output driver is driven from V_{OUT} to guarantee proper operation.

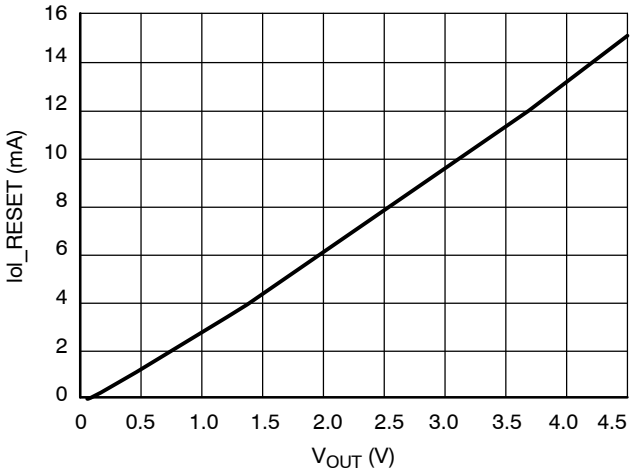


Figure 22. Output Current of Reset Output vs. V_{OUT} Voltage

Initialization

The initialization is started if V_{SUP} is switched on. This is independent of the EN pin.

V_{SUP} Power ON

The NCV7361A starts in the normal mode when V_{SUP} is applied [>3.15 V (typical)]. The internal circuitry on V_{OUT} as well as the internal regulator starts the initialization with power−on−reset. The voltage regulator is switched on.

If $V_{OUT} > V_{POR}$ the bus−interface will be activated.

If V_{OUT} is higher than V_{Res}, the reset time t_{Res} = 100 ms is started. After t_{Res} the $\overline{\text{RESET}}$ output switches from low to high (Figure 22).

The initialization procedure at power on is started independent from the EN state. The regulator can only be turned off with a high level followed by a low level on the EN pin.

Mode Input EN

The NCV7361A is switched into the sleep mode when EN goes from high to low. The normal mode will be kept as long as EN = high.

The regulator can be turned off by switching EN high to low independent of the state of the bus−transceiver.

The EN input is internally pulled down to guarantee a low with no connection. In the high state, the pulldown current will be switched off to reduce the quiescent current.

The maximum input voltage is V_{SUP}. The threshold is typical 2.1 V and therefore CMOS levels can be used as input signals. Figure 23 shows the internal circuitry of the EN pin.

The EN input is internally pulled down to secure that if this pin is not connected a low level will be generated. It will be used two different pull down current sources for high and low level to minimize the sleep mode current.

The 4 μA pulldown current source is used if the input voltage V_{IN} > high level voltage V_{ENH}. If the input voltage drops below the low level of EN V_{ENL}, the second current source is used. The resulting pulldown current in this case is 100 μA.

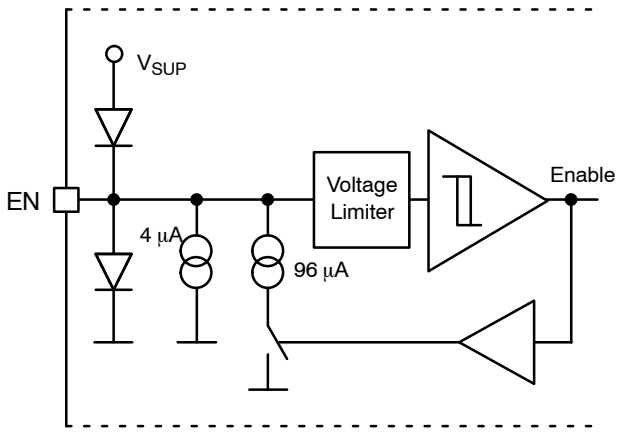


Figure 23. EN Input Circuitry

The wide input voltage range allows different EN control possibilities. If the EN input is connected to an CMOS output of the MCU, a falling edge switches the NCV7361A into sleep mode (the regulator is also switched off). The wake−up is only possible via the bus line.

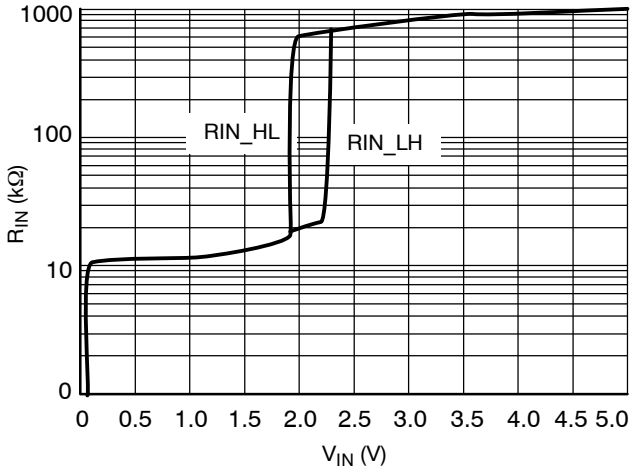


Figure 24. R_{IN} Characteristics of EN Input

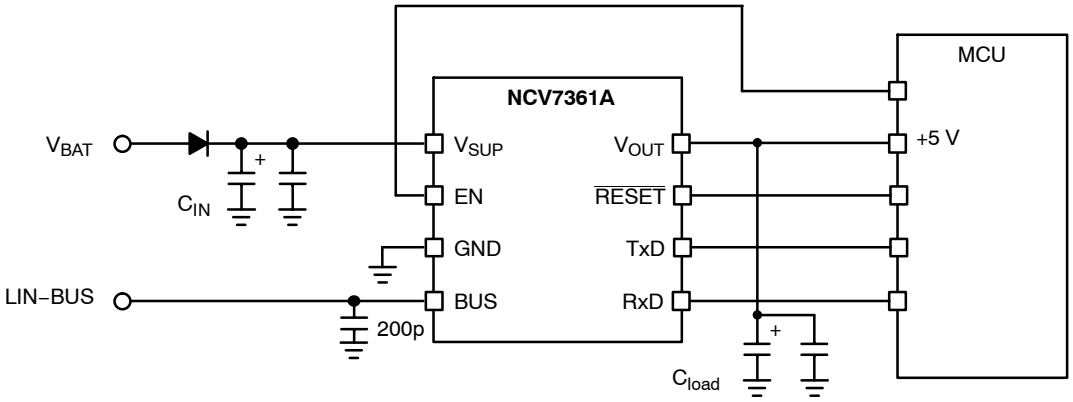


Figure 25. EN Controlled via MCU

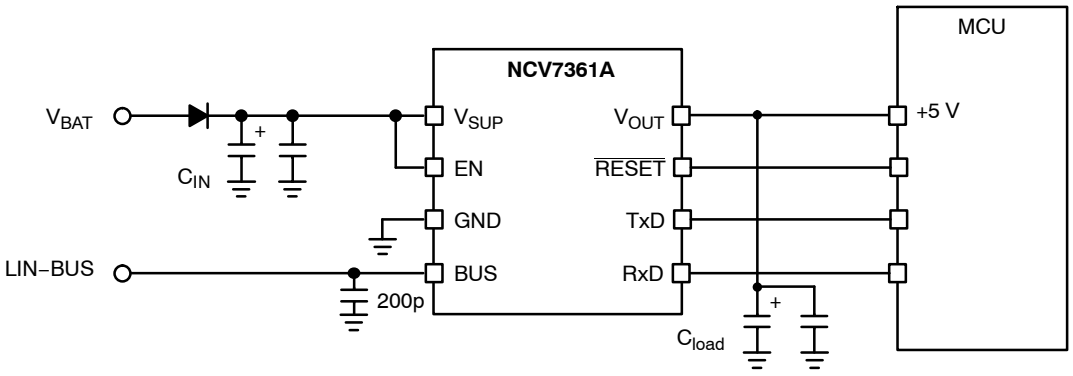


Figure 26. Permanent Normal Mode

If the application does not need the wake−up capability of the NCV7361A, a direct connection EN to V_{SUP} is possible. In this case, the NCV7361A operates in permanent normal mode. Also possible is the external (outside of the module) control of the EN line via a V_{BAT} signal.

Wake−Up

If the regulator is in a standby (sleep) mode, it can be woken up with the BUS interface. Every pulse on the BUS (high pulse or low pulse) with a pulse width of minimum 25 μs switches on the regulator.

After the BUS wake−up for the regulator, it can only be turned off with a high level followed by a low level on the EN pin.

Overtemperature Shutdown

The thermal shutdown threshold is 155°C < T_J < 175°C. When exceeded, the overtemperature shutdown will be active and the regulator voltage will be switched off. V_{OUT} drops down, the reset state is entered and the bus−transceiver is switched off (recessive state).

After T_J falls below 140°C, the NCV7361A will be initialized (see Figure 17), independent from the voltage levels on EN and BUS. Within the thermal shutdown mode, the transceiver can't be switched to the normal mode with local or with remote wake−up.

Function of the NCV7361A is possible between T_{Amax} (125°C) and the switch−off temperature, but small parameter differences can appear.

After overtemperature switch−off the IC behaves as described in the $\overline{\text{RESET}}$ chapter.

APPLICATION HINTS

LIN System Parameter

Bus Loading Requirements

Parameter	Symbol	Min	Typ	Max	Unit
Operating Voltage Range	V_{BAT}	8.0	–	18	V
Voltage Drop of Reverse Protection Diode	V_{Drop_rev}	0.4	0.7	1.0	V
Voltage Drop at the Series Diode in Pull Up Path	$V_{SerDiode}$	0.4	0.7	1.0	V
Battery Shift Voltage	V_{Shift_BAT}	0	–	0.1	V_{BAT}
Ground Shift Voltage	V_{Shift_GND}	0	–	0.1	V_{BAT}
Master Termination Resistor	R_{master}	900	1000	1100	Ω
Slave Termination Resistor	R_{slave}	20	30	60	kΩ
Number of System Nodes	N	2	–	16	–
Total Length of Bus Line	LEN_{BUS}	–	–	40	m
Line Capacitance	C_{LINE}	–	100	150	pF/m
Capacitance of Master Node	C_{Master}	–	220	–	pF
Capacitance of Slave Node	C_{Slave}	–	220	250	pF
Total Capacitance of the Bus including Slave and Master Capacitance	C_{BUS}	1.0	4.0	10	nF
Network Total Resistance	$R_{Network}$	537	–	863	Ω
Time Constant of Overall System	τ	1.0	–	5.0	μs

Recommendations for System Design

The goal of the LIN physical layer standard is to have a universal definition of the LIN system for plug and play solutions in LIN networks up to 20 kbd bus speeds.

In case of small and medium LIN networks, it's recommended to adjust the total network capacitance to at least 4.0 nF for good EMC and EMI behavior. This can be done by setting only the master node capacitance. The slave node capacitance should have a unit load of typically 220 pF for good EMC/EMI behavior.

In large networks with long bus lines and the maximum number of nodes, some system parameters can exceed the defined limits and the LIN system designer must intervene.

The whole capacitance of a slave node is not only the unit load capacitor itself. Additionally, there is the capacitance of wires and connectors, and the internal capacitance of the LIN transmitter. This internal capacitance is strongly dependent on the technology of the IC manufacturer and should be in the range of 30 pF to 150 pF. If the bus lines have a total length of nearly 40m, the total bus capacitance can exceed the LIN system limit of 10 nF.

A second parameter of concern is the integrated slave termination resistor tolerance. If most of the slave nodes have a slave termination resistance near by the allowed maximum of 60 kΩ, the total network resistance is more than 700 Ω. Even if the total network capacitance is below or equal to the maximum specified value of 10 nF, the network time constant is higher than 7.0 μs.

This problem can be solved only by adjusting the master termination resistor to the required maximum network time constant of 5.0 μs (max).

The LIN bus output driver of the NCV7361A provides a higher drive capability than necessary (40 mA @ 1.2 V) within the LIN standard (33.6 mA @ 1.2 V). With this driver stage the system designer can increase the maximum LIN networks with a total network capacitance of more than 10 nF. The total network resistance can be decreased to:

$$R_{tl\_min} = (V_{Bat\_max} - V_{BUSdom})/I_{BUS\_max}$$
$$= (18\ V - 1.2\ V)/40\ mA = 420\ \Omega$$

NOTE: The NCV7361A meets the requirements for implementation in RC−based slave nodes. The LIN Protocol Specification requires the deviation of the slave node clock to the master node clock after synchronization must not differ by more than ±2%.

Setting the network time constant is necessary in large networks (primary resistance) and also in small networks (primary capacitance).

MIN/MAX SLOPE TIME CALCULATION

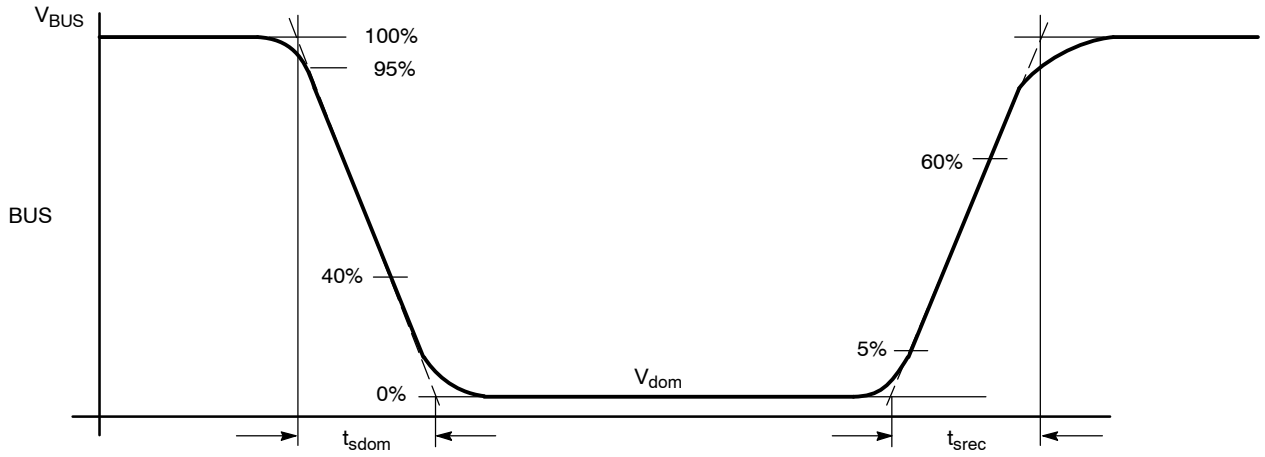


Figure 27. Slope Time Calculation

The slew rate of the bus voltage is measured between 40% and 60% of the output voltage swing (linear region). The output voltage swing is the difference between dominant and recessive bus voltage.

$$dV/dt = 0.2 * V_{swing}/(t_{40\%}-t_{60\%})$$

The slope time is the extension of the slew rate tangent until the upper and lower voltage swing limits:

$$t_{slope} = 5 * (t_{40\%}-t_{60\%})$$

The slope time of the recessive to dominant edge is directly determined by the slew rate control of the transmitter:

$$t_{slope} = V_{swing}/dV/dt$$

The dominant to recessive edge is influenced from the network time constant and the slew rate control, because it's a passive edge. In case of low battery voltages and high bus loads the rising edge is only determined by the network. If the rising edge slew rate exceeds the value of the dominant one, the slew rate control determines the rising edge.

Power Dissipation and Operating Range

The max power dissipation depends on the thermal resistance of the package and the PCB, the temperature difference between Junction and Ambient as well as the airflow.

The power dissipation can be calculated with:

$$P_D = (V_{SUP} - V_{OUT}) * I_{VOUT} + P_{D\_TX}$$

The power dissipation of the transmitter P_{D_TX} depends on the transceiver configuration and its parameters as well as on the bus voltage $V_{BUS} = V_{BAT} - V_D$, the resulting termination resistance R_L, the capacitive bus load C_L and the bit rate. Figure 28 shows the dependence of power dissipation of the transmitter as function of V_{SUP}. The conditions for calculation the power dissipation was: R_L = 500 Ω, C_L = 10 nF, Bitrate = 20 kbit and duty cycle on TxD of 50%.

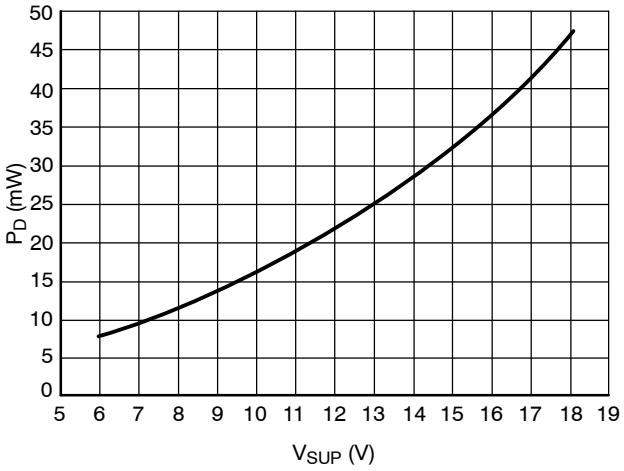


Figure 28. Power Dissipation LIN Transceiver @ 20 kbit

The permitted package power dissipation can be calculated:

$$P_{Dmax} = \frac{T_J - T_A}{R_{\theta J-A}}$$

If we consider that $P_{D\_TX\_max} = f(V_{SUP})$, it can be calculated the max output current IV_{OUT} on V_{OUT}:

$$I_{VOUTmax} = \frac{\frac{T_J-T_A}{R_{\theta J-A}} - P_{D\_TX\_max} @ VSUP}{VSUP - VOUT}$$

T_J–T_A is the temperature difference between junction and ambient, and R_{th} is the thermal resistance of the package. The thermal energy is transferred via the package and the pins to the ambient. This transfer can be improved with additional ground areas on the PCB as well as ground areas under the IC.

Table 1. SO−8 Thermal RC Network Models*

Copper Area (1 oz thick)			54 mm²	714 mm²		54 mm²	714 mm²	
(SPICE Deck Format)			Cauer Network			Foster Network		
			54 mm²	714 mm²	Units	Tau	Tau	Units
C_C1	**Junction**	**GND**	**1.08E−05**	**1.08E−05**	W−s/C	1.00E−06	1.00E−06	sec
C_C2	**node1**	**GND**	**4.10E−05**	**4.10E−05**	W−s/C	1.00E−05	1.00E−05	sec
C_C3	**node2**	**GND**	**1.13E−04**	**1.13E−04**	W−s/C	1.00E−04	1.00E−04	sec
C_C4	**node3**	**GND**	**4.42E−04**	**4.40E−04**	W−s/C	5.00E−04	5.00E−04	sec
C_C5	**node4**	**GND**	**1.74E−03**	**1.71E−03**	W−s/C	1.00E−03	1.00E−03	sec
C_C6	**node5**	**GND**	**1.39E−03**	**1.34E−03**	W−s/C	1.00E−02	1.00E−02	sec
C_C7	**node6**	**GND**	**2.08E−02**	**1.78E−02**	W−s/C	1.00E−01	1.00E−01	sec
C_C8	**node7**	**GND**	**1.08E−02**	**9.75E−03**	W−s/C	1.00E+00	1.00E+00	sec
C_C9	node8	GND	1.14E−01	1.84E−01	W−s/C	1.00E+01	1.00E+01	sec
C_C10	node9	GND	8.11E−01	3.00E+00	W−s/C	5.00E+01	5.00E+01	sec
						R's	**R's**	
R_R1	**Junction**	**node1**	**0.119**	**0.119**	C/W	0.070	0.070	C/W
R_R2	**node1**	**node2**	**0.286**	**0.286**	C/W	0.152	0.152	C/W
R_R3	**node2**	**node3**	**0.857**	**0.859**	C/W	0.481	0.481	C/W
R_R4	**node3**	**node4**	**1.181**	**1.189**	C/W	0.690	0.690	C/W
R_R5	**node4**	**node5**	**1.241**	**1.276**	C/W	0.584	0.584	C/W
R_R6	**node5**	**node6**	**2.574**	**2.690**	C/W	3.223	3.223	C/W
R_R7	**node6**	**node7**	**18.065**	**21.708**	C/W	0.823	0.823	C/W
R_R8	**node7**	**node8**	**27.965**	**26.035**	C/W	26.801	35.166	C/W
R_R9	node8	node9	80.896	49.821	C/W	63.710	52.538	C/W
R_R10	node9	GND	49.468	15.252	C/W	86.119	25.510	C/W

*Bold face items in the tables above represent the package without the external thermal system.

The Cauer networks generally have physical significance and may be divided between nodes to separate thermal behavior due to one portion of the network from another. The Foster networks, though when sorted by time constant (as above) bear a rough correlation with the Cauer networks, are really only convenient mathematical models. Cauer networks can be easily implemented using circuit simulating tools, whereas Foster networks may be more easily implemented using mathematical tools (for instance, in a spreadsheet program), according to the following formula:

$$R(t) = \sum_{i=1}^{n} R_i \left(1 - e^{-t/tau_i}\right)$$

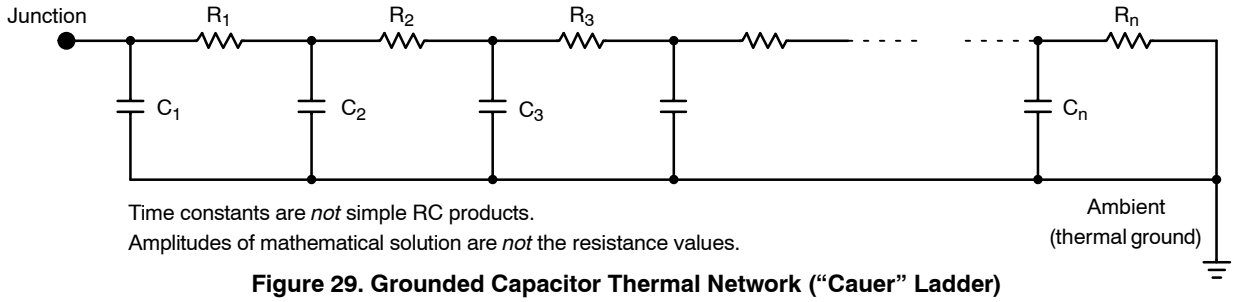


Figure 29. Grounded Capacitor Thermal Network ("Cauer" Ladder)

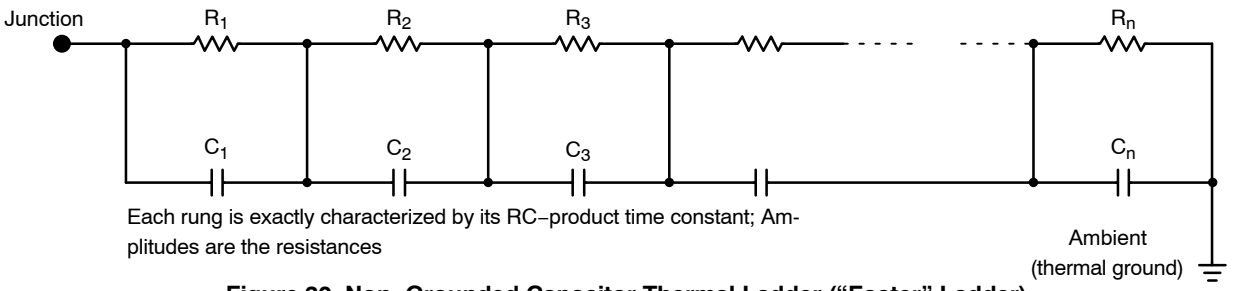


Figure 30. Non−Grounded Capacitor Thermal Ladder ("Foster" Ladder)

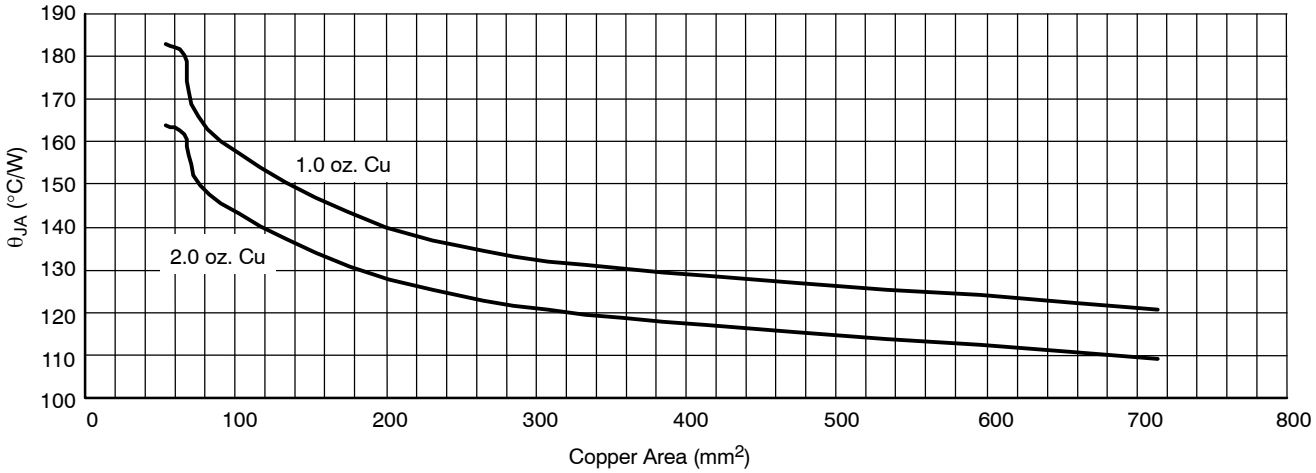


Figure 31. SO−8, θ_{JA} as a Function of the Pad Copper Area Including Traces, Board Material

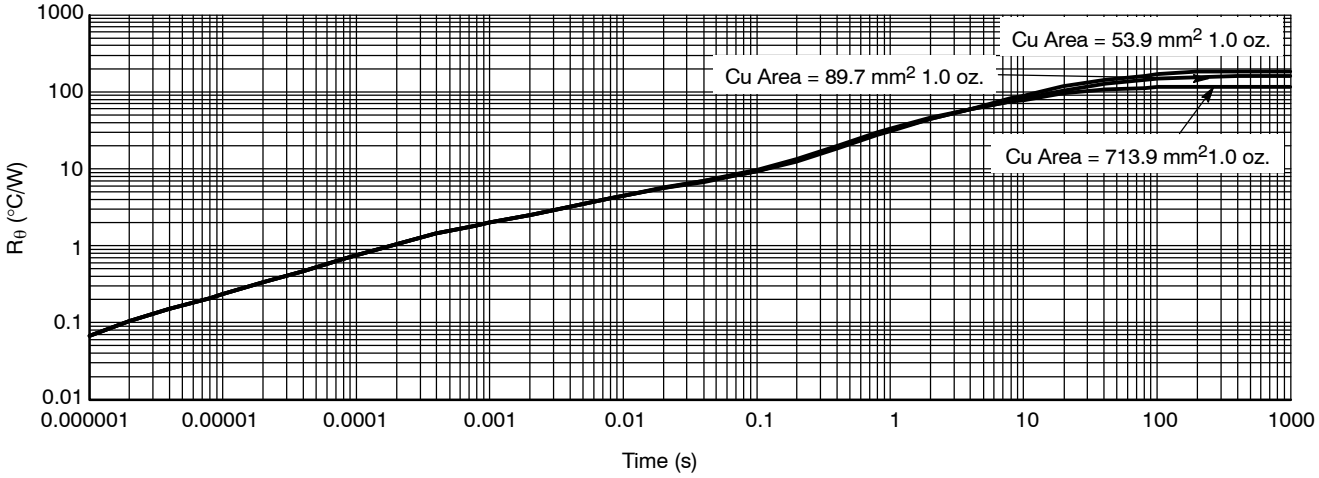


Figure 32. SO−8 Thermal Transient Response on Typical Test Boards

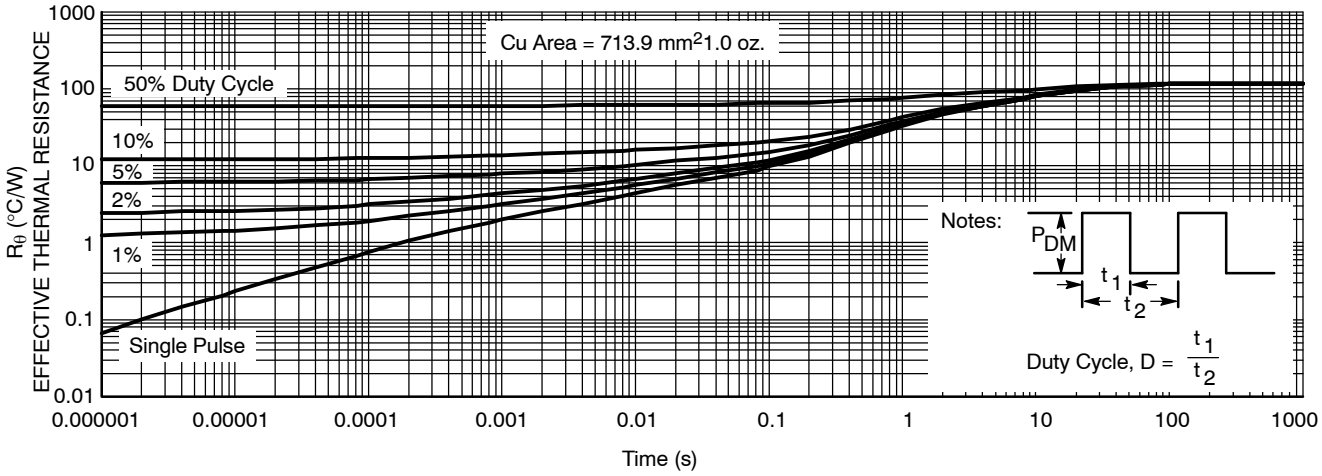


Figure 33. SO−8 Thermal Duty Cycle Curves on 1.0 in. Spreader Test Board

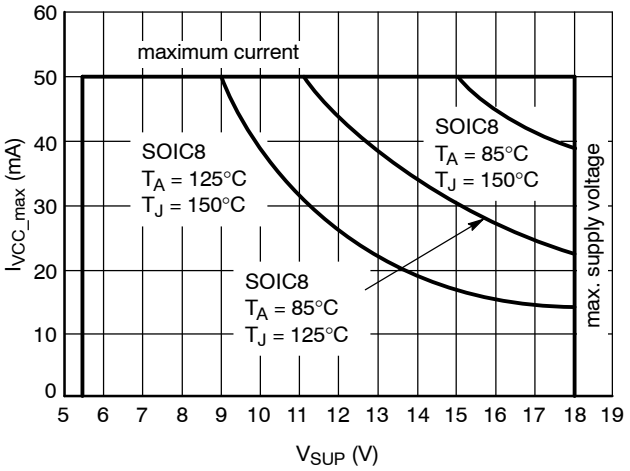


Figure 34. Safe Operating Area

The linear regulator of the NCV7361A operates with input voltages up to 18 V and can output a current of 50 mA. The maximum power dissipation limits the maximum output current at high input voltages and high ambient temperatures. The output current of 50 mA at an ambient temperature of T_A = 125°C is only possible with small voltage differences between V_{SUP} and V_{CC}. See Figure 34 for safe operating areas for different ambient and junction temperatures.

Regulator Circuitry

Low Dropout Regulator

The voltage regulator of the NCV7361A is a low dropout regulator (LDO) with a P−MOSFET as the driving transistor.

This type of regulator has a standard pole, generated from the internal frequency compensation and an additional pole, which is dependent from the load and the load capacity. This additional pole can cause an instable behavior of the regulator! It requires a zero point to compensate this additional pole. It can be realized via an additional load resistor in series with a load capacity. It is used for this compensation the Equivalent Series Resistance (ESR) of the load capacity. Every real capacity is characterized with an ESR value. With the help of this ESR value an additional zero point is implemented into the amplification loop and therefore the result of the negative phase shift is compensated.

Because of this correlation the regulator has a stable operating area which is defined by the load resistance R_L, the load capacity C_L and the corresponding ESR value. The load resistance resp. load current is defined by the application itself and therefore the compensation of the pole can only be done via variation of the load capacity and ESR value.

Input Capacity on V_{SUP} C_{IN}

It is necessary to have an input capacity of C_{IN} = 4.7 μF. Higher capacity values improve the line transient response and the supply noise rejection behavior. The combination of electrolytic capacity (e.g.100 μF) in parallel with a ceramic RF−capacity (e.g. 100 nF) archives good disturbance suppressing.

The input capacity should be placed as close as possible (< 1 cm) to the V_{SUP} pin.

Load Capacity on V_{OUT} C_L

The regulator is stabilized by the output capacitor C_L. The NCV7361A requires a minimum of 4.7 μF capacity connected to the 5.0 V output to insure stability. This capacitor should maintain its ESR in the stable region of the ESR curve (Figure 35) over the full operating temperature range of the application. The capacity value and the ESR of a capacitor changes with temperature. The minimal capacity value must be kept within the whole operating temperature range.

Example 1:

The regulator is stabilized using a 47 μF aluminum electrolytic capacitor load (ESR = 0.7 Ω @ 25°C). The capacitance decreases to 42 μF and the ESR increases to 8.9 Ω at an ambient temperature of −40°C. The ESR value is located in the unstable region. The regulator will be unstable at −40°C.

Example 2:

The regulator is stabilized using a 47 μF tantalum capacitor load (ESR = 0.1 Ω @ 25°C). The capacitance decreases to 45 μF and the ESR increases to 0.11 Ω at an ambient temperature of −40°C. The ESR value is located in the stable region. The regulator will be stable at −40°C.

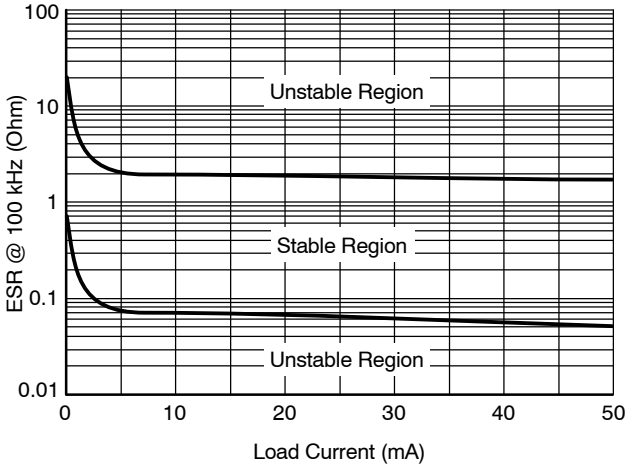


Figure 35. ESR Curves for 6.8 μF ≤ C_L ≤ 100 μF and Frequency of 100 kHz

The value and type of the output capacitor can be selected by using the diagram shown in Figure 35.

Capacity Value

The capacity value of an electrolytic capacitor is dependence from the voltage, temperature and the frequency. The temperature coefficient of the capacity value is positive, that means that the value increases with increasing of the temperature. The capacity value decreases with increasing of the frequency. This behavior of a capacitor can cause that at T_A = −40°C the capacity value falls below the minimum required capacity for the regulator. In this case the regulator becomes instable, which means the regulator starts oscillation. The nominal value of the capacitor at T_A = 25°C has to be chosen with enough margin under consideration of the capacitor specification. The instable behavior will be amplified because of the decreasing of the capacity with this oscillation.

ESR

The Equivalent Serial Resistance is the resistor part of the equivalent circuit diagram of a capacitor. The ESR value is dependent from the temperature and frequency. Normally the specified ESR values for a capacitor is valid at a temperature of T_A = 25°C and a frequency of f = 100 kHz.

The temperature coefficient is negative, which means with increasing of the temperature the ESR value decreases. In the choice of the capacity has to be taken into account that the ESR can decrease at T_A = −40°C dramatically that the valid operating area can be left, which causes that the regulator will be instable.

Tantalum Capacitors

This type of capacitor has a low dependence of the capacity and the ESR from the temperature and is therefore well suitable as V_{OUT} load capacity.

Aluminum Capacitors

These capacitors show a strong influence of the capacity and the ESR from the temperature. These characteristic restrains the usability as load capacity for the low drop regulator of NCV7361A.

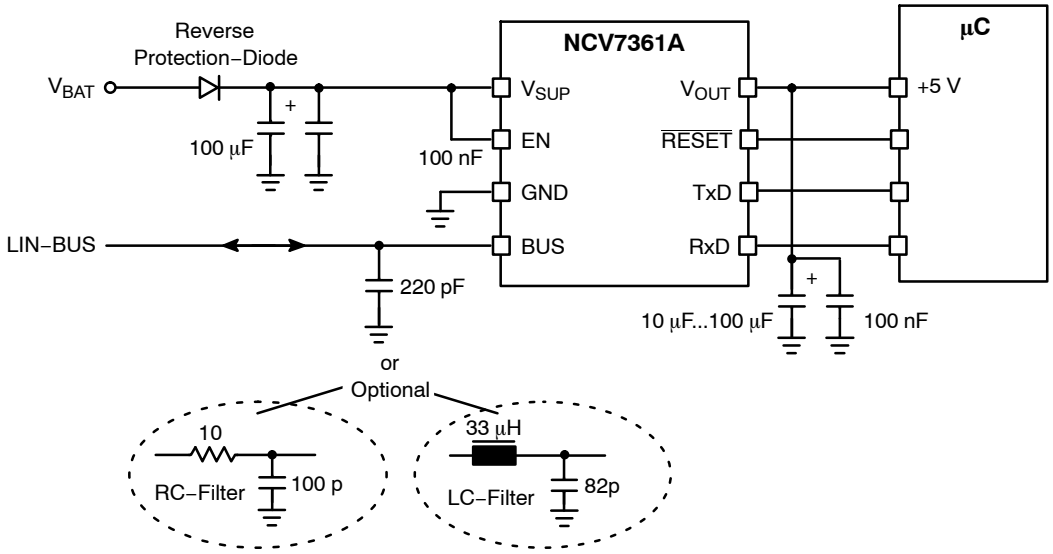


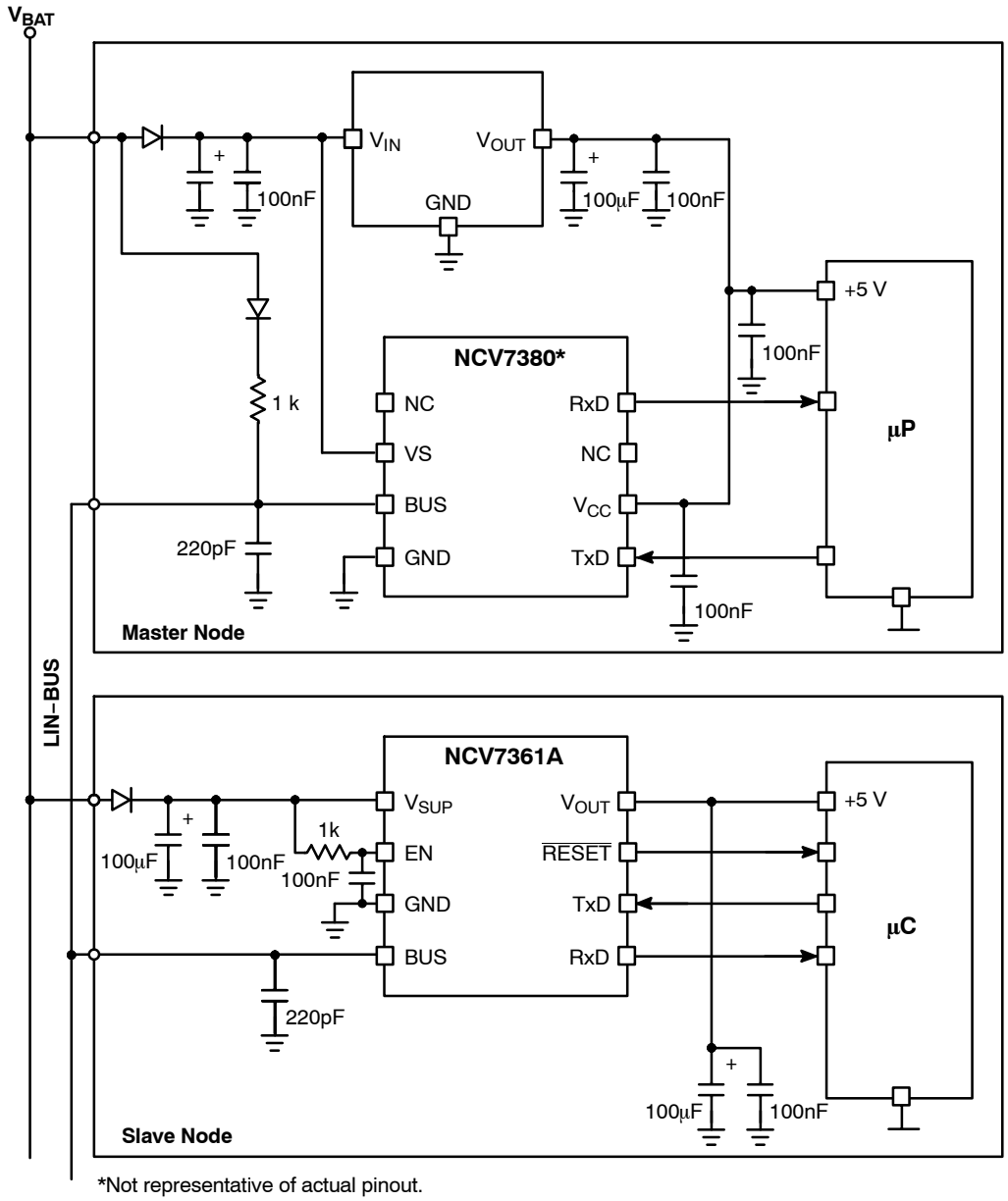
Figure 36. Application Circuit (Slave Node)

EMI Suppressing

To minimize the influence of EMI from the bus line, a 220 pF capacitor should be directly connected to the BUS pin (see Figure 36).

The value of the filter capacity can be adjusted to the size of the LIN network. 220 pF should be used for bigger networks. Values from 333 pF up to 1.0 nF should be used for middle to small LIN networks. Finally the size of the filter capacitor influences the effectiveness of the EMI suppressing in conformance to the maximum LIN bus capacity of 10 nF.

LC−filters or RC−filters can also be used. The value of C, L or R, depends on the corner frequency, the maximum LIN bus capacity (10 nF) and the compliance with the DC− and AC LIN bus parameters.



*Not representative of actual pinout.

Figure 37. Application Circuit for LIN Sub−Bus with NCV7361A as Slave Node

Connection to Flash−MCU

During programming of a flash MCU the NCV7361A should be disconnected from the MCU. This can be done by disconnecting the supply voltage of the NCV7361A or by turning off the NCV7361A with the EN pin. A blocking diode must be used between the MCU and the RxD pin to avoid loading of the programming data.

The programming of the flash is also possible via the LIN pin, if the MCU supports this kind of flash mode.

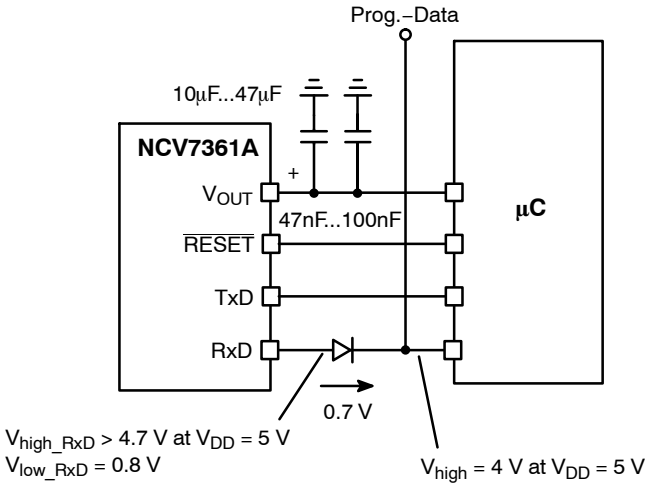


Figure 38. Example Circuitry for Connection of RxD to MCU for Flash Programming

Operating During Disturbance

Operating Without V_{SUP} or GND

The BUS pin is designed for voltages of GND − 24 V up to GND + 30 V. This prevents loss of communication between other bus nodes with the loss of V_{SUP} or loss of GND. The BUS pin will remain at V_{BAT} and current draw will be minimal with the loss of GND or V_{SUP}.

Short Circuit BUS to V_{BAT}

- Recessive LIN bus is blocked, no influence to the NCV7361A
- Dominant Current limit, thermal shutdown of NCV7361A if power dissipation raises T_J

Short Circuit BUS to GND

The LIN bus is blocked. There is no influence to the NCV7361A.

Short Circuit TxD to GND

The LIN transceiver is permanent in the dominant state as is the LIN bus. This state can only be detected from the LIN controller. In this case the controller must switch−off the LIN node via the EN input of the NCV7361A and look for a recessive state. A thermal shutdown of NCV7361A will appear if the thermal shutdown threshold is exceeded.

TxD Open

The internal pullup resistor forces the LIN node to the recessive state. The communication between the other bus−nodes will not be disturbed.

Short Circuit V_{OUT} to GND

The V_{OUT} pin is protected via a current limit. This state is comparable with the behavior in the sleep mode.

Overload of V_{OUT}

Thermal Switch−Off

The power dissipation is increasing if the load current is between I_{VOUT_max} and I_{LVOUT}. If the IC exceeds the thermal shutdown threshold of > 155°C, the transceiver will be switched off. The voltage regulator will also be switched off and a reset signal is forced.

Overcurrent

If the current limit is active the voltage on V_{OUT} drops down. If this voltage is below the threshold V_{RES}, a reset will be forced.

Undervoltage V_{SUP}, V_{OUT}

The reset circuit guarantees the correct behavior of the driver during undervoltage. The BUS pin generates the recessive state if $V_{OUT} < V_{MRes}$. The inputs EN and TxD have pull−down and pull−up circuits respectively.

If $V_{MRes} \leq V_{OUT} \leq 4.5$ V the TxD signal is transmitted to the bus. The receive mode is also active.

Short Circuit RxD, RESET to GND or V_{OUT}

Both outputs are short circuit proof to V_{OUT} and ground.

ESD/EMC Remarks

General Remarks

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD). Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

ESD Test

The NCV7361A is tested according to MIL883−3015.7 (Human Body Model).

EMC

The test on EMC impacts is done according to ISO 7637−1 for power supply pins and ISO 7637−3 for data and signal pins.

POWER SUPPLY PIN V_{SUP}

Test Pulse	Condition	Duration
1	t_1 = 5.0 s/U_S = −100 V/t_D = 2.0 ms	5000 Pulses
2	t_1 = 0.5 s/U_S = 100 V/t_D = 0.05 ms	5000 Pulses
3a/b	U_S = −150 V/U_S = 100 V Burst 100 ns/10 ms/90 ms Break	1 h
5	R_i = 0.5 Ω, t_D = 400 ms t_r = 0.1 ms/U_P + U_S = 40 V	10 Pulses Every 1 Min

DATA AND SIGNAL PINS EN, BUS

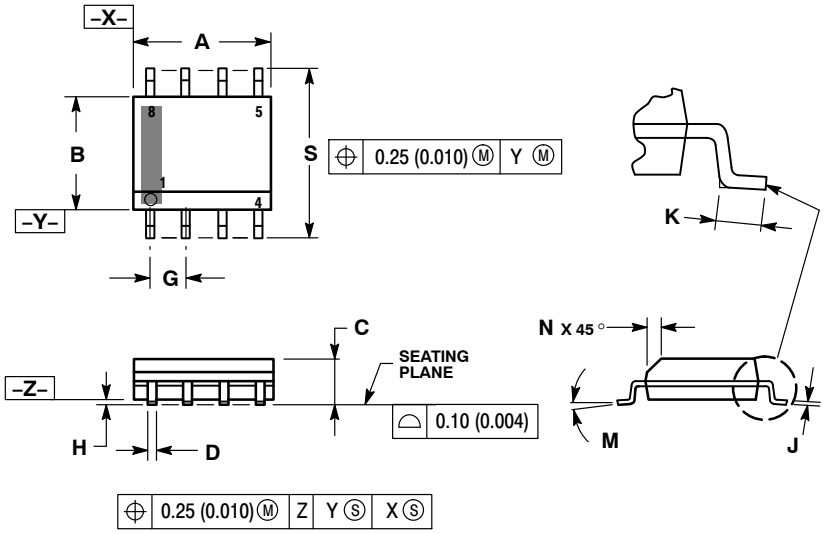
Test Pulse	Condition	Duration
1	t_1 = 5.0 s/U_S = −100 V/t_D = 2.0 ms	1000 Pulses
2	t_1 = 0.5 s/U_S = 100 V/t_D = 0.05 ms	1000 Pulses
3a/b	U_S = −150 V/U_S = 100 V Burst 100 ns/10 ms/90 ms Break	1000 Burst

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

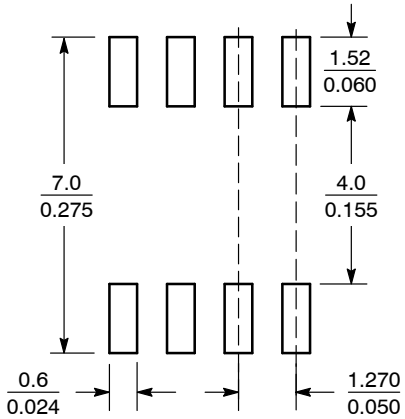
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

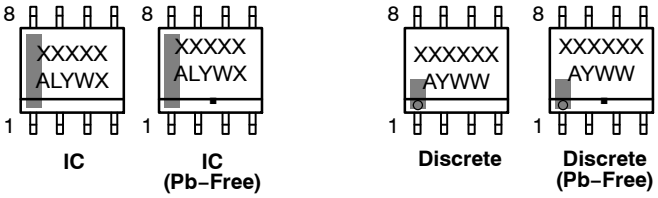
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC | IC (Pb−Free) | Discrete | Discrete (Pb−Free)

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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DESCRIPTION:	**SOIC−8 NB**	**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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