

NDD60N745U1

N-Channel Power MOSFET 600 V, 745 mΩ

Features

- 100% Avalanche Tested
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

ABSOLUTE MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter		Symbol	Value	Unit	
Drain-to-Source Voltage		V _{DSS}	600	V	
Gate-to-Source Voltage		V _{GS}	±25	V	
Continuous Drain Current R _{θJC}	Steady State	I _D	T _C = 25°C	6.6	A
			T _C = 100°C	4.2	
Power Dissipation – R _{θJC}	Steady State	P _D	84	W	
Pulsed Drain Current	t _p = 10 μs	I _{DM}	27	A	
Operating Junction and Storage Temperature		T _J , T _{STG}	-55 to +150	°C	
Source Current (Body Diode)		I _S	6.6	A	
Single Pulse Drain-to-Source Avalanche Energy (I _D = 2.5 A)		EAS	38	mJ	
Peak Diode Recovery (Note 1)		dv/dt	15	V/ns	
Lead Temperature for Soldering Leads		T _L	260	°C	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I_{SD} < 6.6 A, di/dt ≤ 400 A/μs, V_{DS peak} ≤ V_{(BR)DSS}, V_{DD} = 80% V_{(BR)DSS}

THERMAL RESISTANCE

Parameter		Symbol	Value	Unit
Junction-to-Case (Drain)	NDD60N745U1	R _{θJC}	1.5	°C/W
Junction-to-Ambient Steady State (Note 3)	NDD60N745U1	R _{θJA}	47	°C/W
	(Note 2) NDD60N745U1-1		98	
	(Note 2) NDD60N745U1-35		95	

2. Insertion mounted
3. Surface mounted on FR4 board using 1" sq. pad size (Cu area = 1.127 in sq [2 oz] including traces)

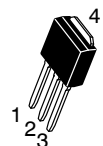
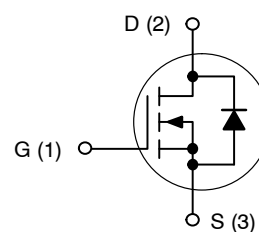


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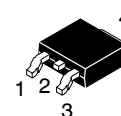
<http://onsemi.com>

V _{(BR)DSS}	R _{DS(ON) MAX}
600 V	745 mΩ @ 10 V

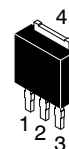
N-Channel MOSFET



IPAK
CASE 369D
STYLE 2



DPAK
CASE 369C
STYLE 2



IPAK
CASE 369AD
STYLE 2

ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

NDD60N745U1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 1 mA	600			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J			540		mV/°C
Drain-to-Source Leakage Current	I _{DSS}	V _{DS} = 600 V, V _{GS} = 0 V	T _J = 25°C		1	μA
			T _J = 125°C		100	
Gate-to-Source Leakage Current	I _{GSS}	V _{GS} = ±20 V			±100	nA

ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	V _{GS(TH)}	V _{DS} = V _{GS} , I _D = 250 μA	2	3.2	4	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J	Reference to 25°C, I _D = 250 μA		7.6		mV/°C
Static Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 3.25 A		610	745	mΩ
Forward Transconductance	g _{FS}	V _{DS} = 15 V, I _D = 3.25 A		5.6		S

DYNAMIC CHARACTERISTICS

Input Capacitance	C _{iss}	V _{DS} = 50 V, V _{GS} = 0 V, f = 1 MHz		440		pF
Output Capacitance	C _{oss}		27			
Reverse Transfer Capacitance	C _{rss}		1.5			
Effective output capacitance, energy related (Note 6)	C _{o(er)}	V _{GS} = 0 V, V _{DS} = 0 to 480 V		21		
Effective output capacitance, time related (Note 7)	C _{o(tr)}	I _D = constant, V _{GS} = 0 V, V _{DS} = 0 to 480 V		71		
Total Gate Charge	Q _g	V _{DS} = 300 V, I _D = 6.8 A, V _{GS} = 10 V		15		nC
Gate-to-Source Charge	Q _{gs}		2.9			
Gate-to-Drain Charge	Q _{gd}		7.3			
Plateau Voltage	V _{GP}		5.3		V	
Gate Resistance	R _g		4.4		Ω	

RESISTIVE SWITCHING CHARACTERISTICS (Note 5)

Turn-on Delay Time	t _{d(on)}	V _{DD} = 300 V, I _D = 6.8 A, V _{GS} = 10 V, R _G = 0 Ω		8		ns
Rise Time	t _r		10			
Turn-off Delay Time	t _{d(off)}		19			
Fall Time	t _f		7			

SOURCE-DRAIN DIODE CHARACTERISTICS

Diode Forward Voltage	V _{SD}	I _S = 6.6 A, V _{GS} = 0 V	T _J = 25°C	0.90	1.6	V
			T _J = 100°C	0.82		
Reverse Recovery Time	t _{rr}	V _{GS} = 0 V, V _{DD} = 30 V, I _S = 6.8 A, d _i /d _t = 100 A/μs		260		ns
Charge Time	t _a		130			
Discharge Time	t _b		130			
Reverse Recovery Charge	Q _{rr}		2.1		μC	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

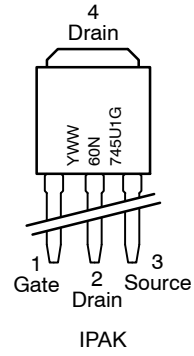
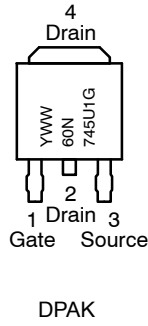
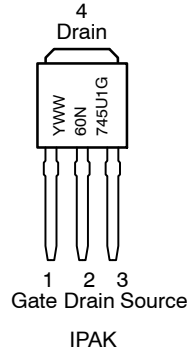
5. Switching characteristics are independent of operating junction temperatures.

6. C_{o(er)} is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{(BR)DSS}

7. C_{o(tr)} is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{(BR)DSS}

NDD60N745U1

MARKING DIAGRAMS



Y = Year
 WW = Work Week
 G = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping [†]
NDD60N745U1-1G	IPAK (Pb-Free, Halogen-Free)	75 Units / Rail
NDD60N745U1-35G	IPAK (Pb-Free, Halogen-Free)	75 Units / Rail
NDD60N745U1T4G	DPAK (Pb-Free, Halogen-Free)	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

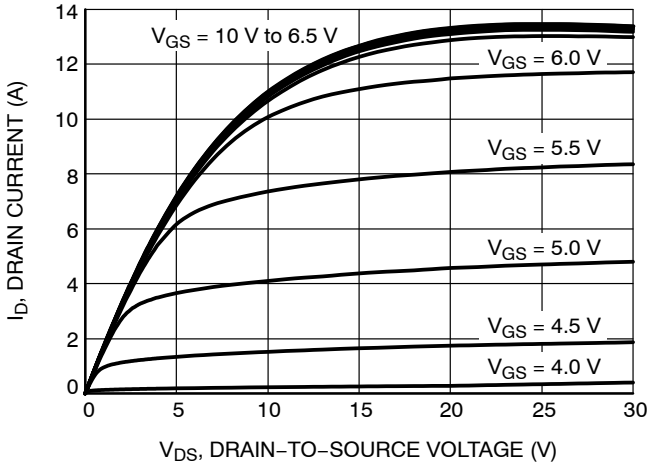


Figure 1. On-Region Characteristics

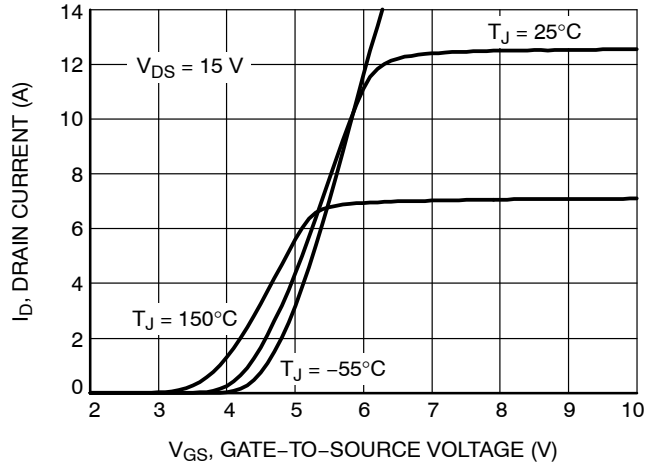


Figure 2. Transfer Characteristics

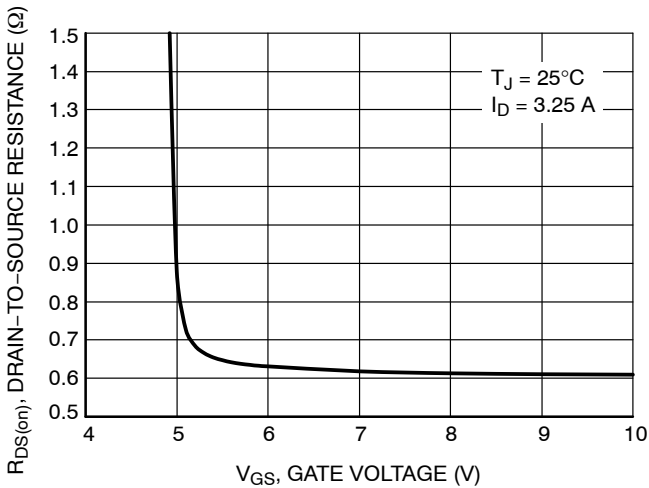


Figure 3. On-Resistance vs. Gate-to-Source Voltage

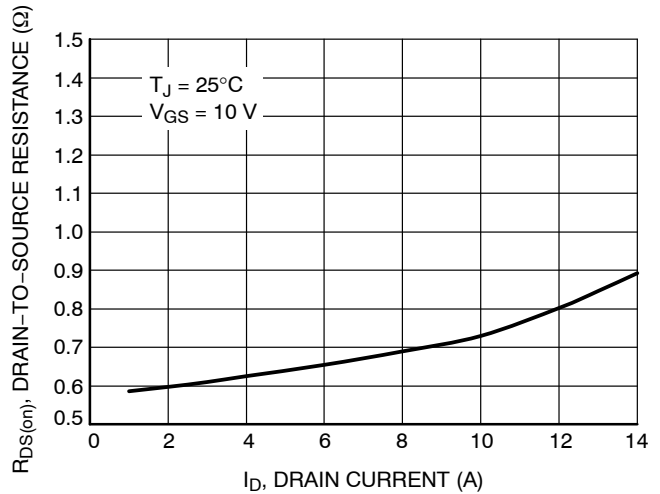


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

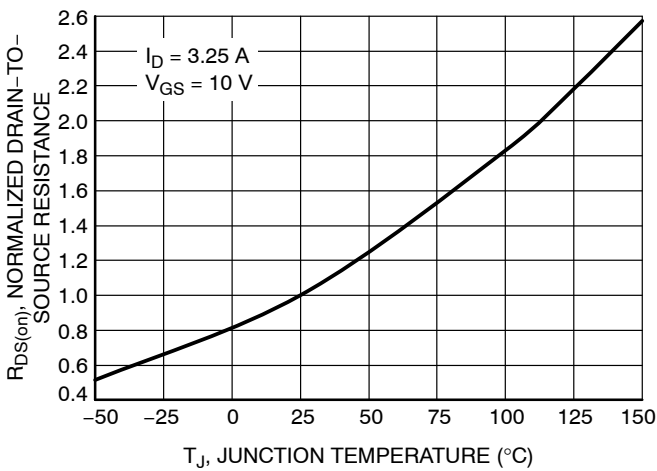


Figure 5. On-Resistance Variation with Temperature

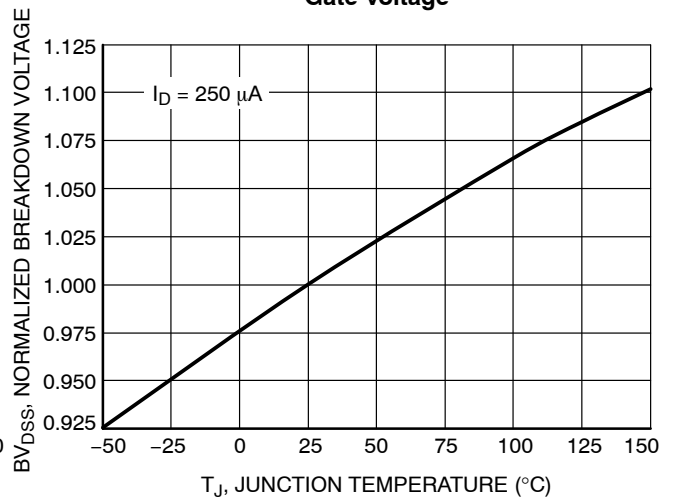


Figure 6. Breakdown Voltage Variation with Temperature

TYPICAL CHARACTERISTICS

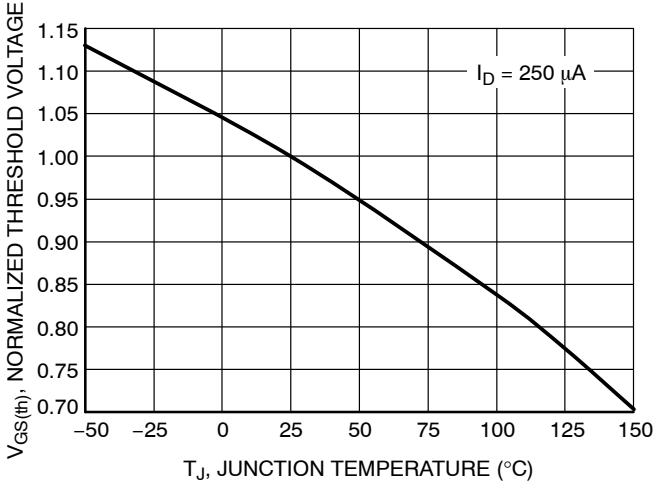


Figure 7. Threshold Voltage Variation with Temperature

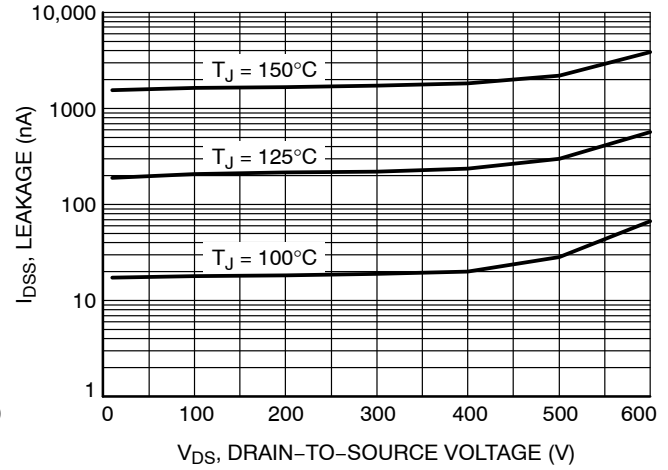


Figure 8. Drain-to-Source Leakage Current vs. Voltage

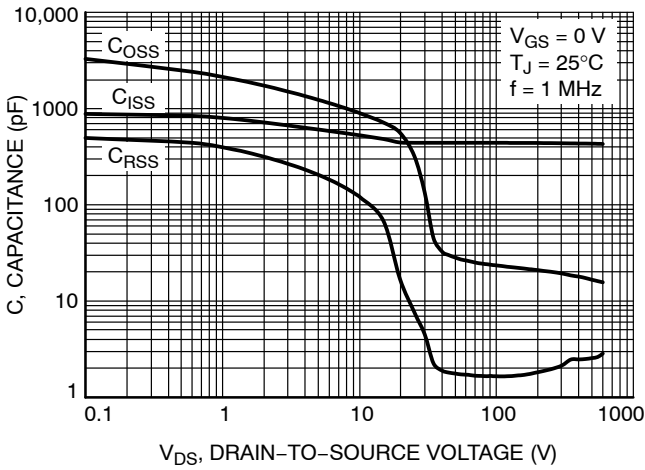


Figure 9. Capacitance Variation

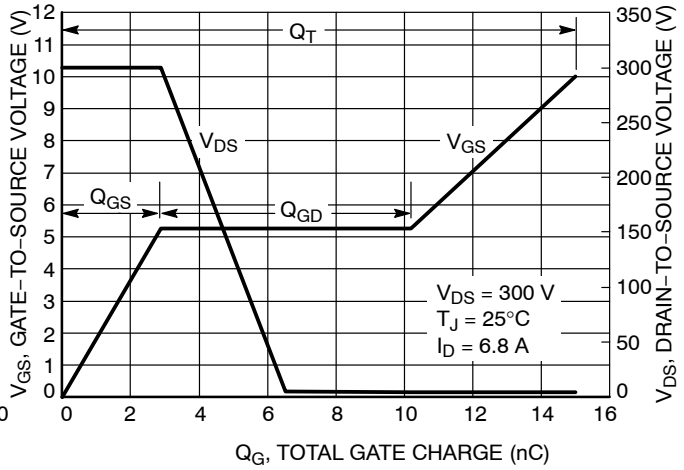


Figure 10. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

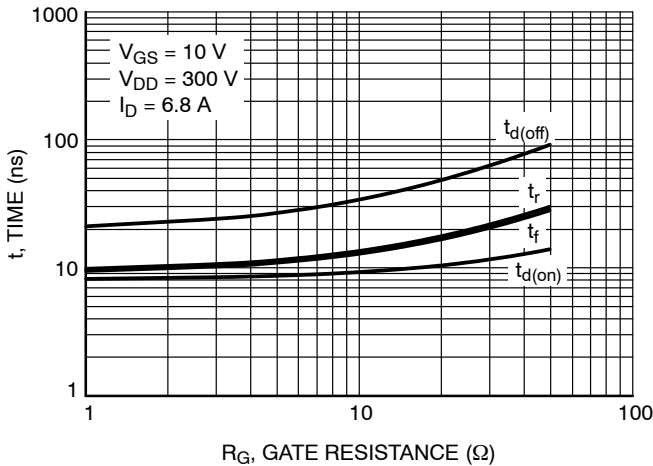


Figure 11. Resistive Switching Time Variation vs. Gate Resistance

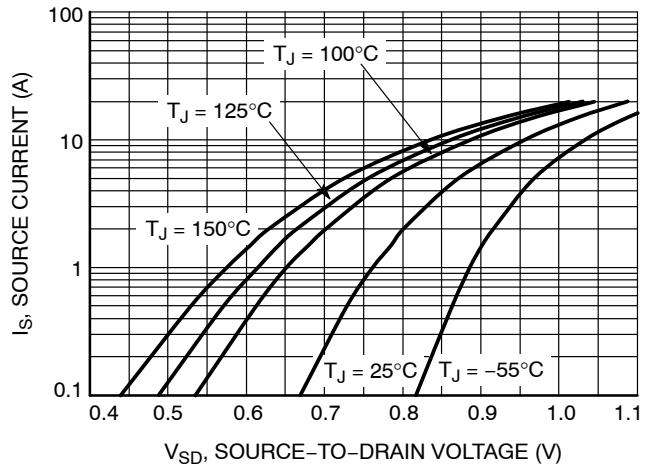


Figure 12. Diode Forward Voltage vs. Current

NDD60N745U1

TYPICAL CHARACTERISTICS

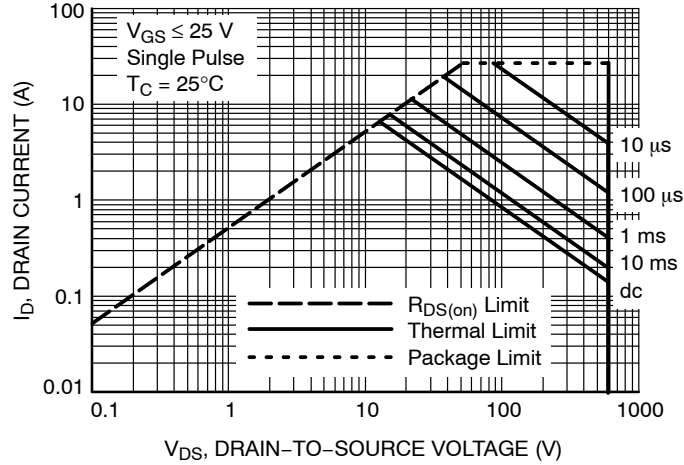


Figure 13. Maximum Rated Forward Biased Safe Operating Area

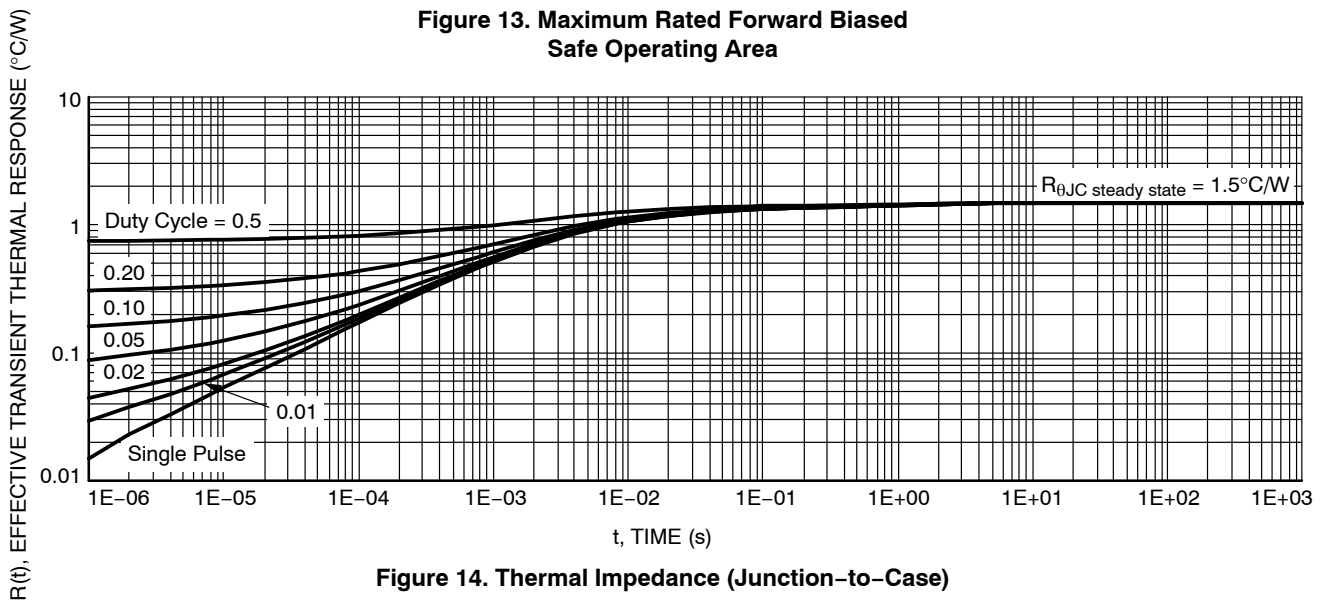


Figure 14. Thermal Impedance (Junction-to-Case)

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

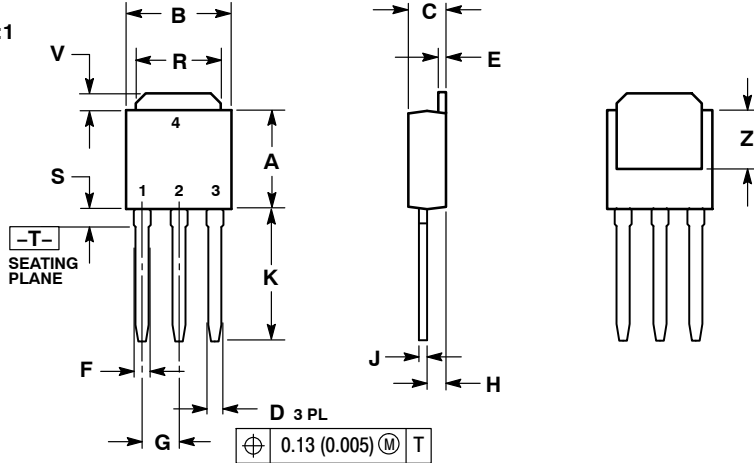
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IPAK CASE 369D-01 ISSUE C

DATE 15 DEC 2010

SCALE 1:1



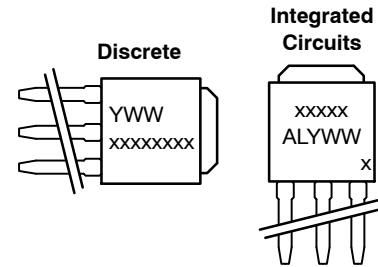
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090	BSC	2.29	BSC
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

MARKING DIAGRAMS

- STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR
- STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN
- STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE
- STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE
- STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE
- STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2
- STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR



- xxxxxxxx = Device Code
- A = Assembly Location
- IL = Wafer Lot
- Y = Year
- WW = Work Week

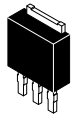
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DESCRIPTION:	IPAK (DPAK INSERTION MOUNT)	PAGE 1 OF 1

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

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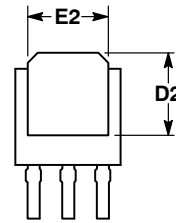
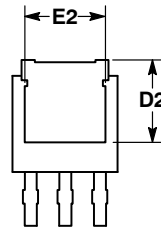
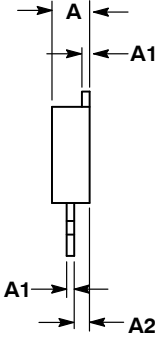
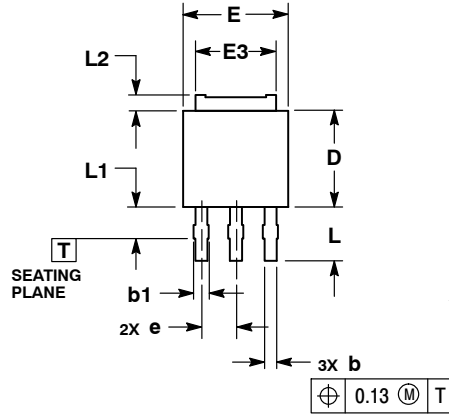
3.5 MM IPAK, STRAIGHT LEAD

CASE 369AD

ISSUE B

DATE 18 APR 2013

SCALE 1:1



OPTIONAL CONSTRUCTION

NOTES:

- 1.. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- 2.. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD GATE OR MOLD FLASH.

DIM	MILLIMETERS	
	MIN	MAX
A	2.19	2.38
A1	0.46	0.60
A2	0.87	1.10
b	0.69	0.89
b1	0.77	1.10
D	5.97	6.22
D2	4.80	---
E	6.35	6.73
E2	4.57	5.45
E3	4.45	5.46
e	2.28 BSC	
L	3.40	3.60
L1	---	2.10
L2	0.89	1.27

GENERIC MARKING DIAGRAMS*

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

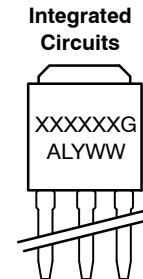
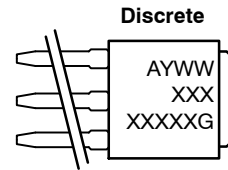
STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR



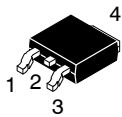
XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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DESCRIPTION:	3.5 MM IPAK, STRAIGHT LEAD	PAGE 1 OF 1

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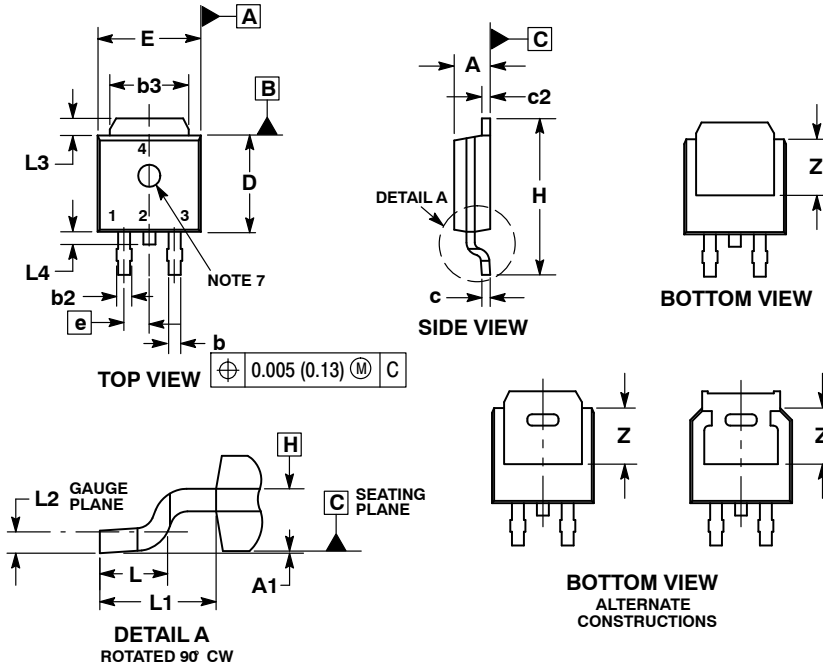
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



DPAK (SINGLE GAUGE) CASE 369C ISSUE F

DATE 21 JUL 2015

SCALE 1:1



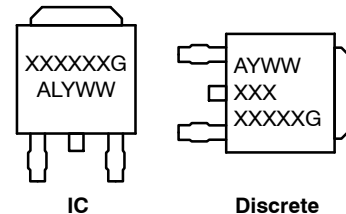
NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: INCHES.
- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
- DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
- OPTIONAL MOLD FEATURE.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090	BSC	2.29	BSC
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114	REF	2.90	REF
L2	0.020	BSC	0.51	BSC
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

GENERIC MARKING DIAGRAM*

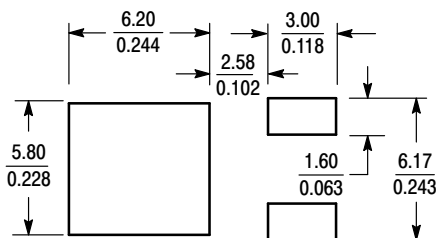
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|--|--|---|---|--|
| <p>STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR</p> | <p>STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN</p> | <p>STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE</p> | <p>STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE</p> | <p>STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE</p> |
| <p>STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2</p> | <p>STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR</p> | <p>STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE</p> | <p>STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE</p> | <p>STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE</p> |



- XXXXXX = Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

SOLDERING FOOTPRINT*



SCALE 3:1 (mm/inches)

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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