

MC74VHCT573A

Octal D-Type Latch with 3-State Output

The MC74VHCT573A is an advanced high speed CMOS octal latch with 3-state output fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

This 8-bit D-type latch is controlled by a latch enable input and an output enable input. When the output enable input is high, the eight outputs are in a high impedance state.

The VHCT inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3 V to 5.0 V, because it has full 5.0 V CMOS level output swings.

The VHCT573A input and output (when disabled) structures provide protection when voltages between 0 V and 5.5 V are applied, regardless of the supply voltage. These input and output structures help prevent device destruction caused by supply voltage-input/output voltage mismatch, battery backup, hot insertion, etc.

Features

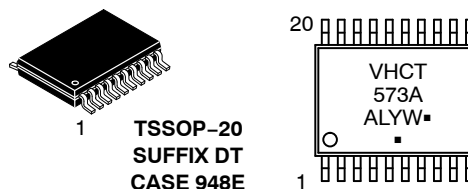
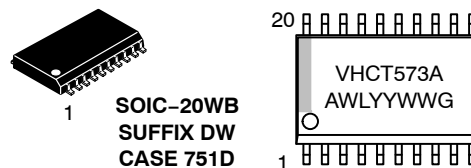
- High Speed: $t_{PD} = 7.7$ ns (Typ) at $V_{CC} = 5.0$ V
- Low Power Dissipation: $I_{CC} = 4$ μ A (Max) at $T_A = 25^\circ$ C
- TTL-Compatible Inputs: $V_{IL} = 0.8$ V; $V_{IH} = 2.0$ V
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Designed for 4.5 V to 5.5 V Operating Range
- Low Noise: $V_{OLP} = 1.6$ V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance:
 - Human Body Model > 2000 V;
 - Machine Model > 200 V
- Chip Complexity: 234 FETs or 58.5 Equivalent Gates
- These Devices are Pb-Free and are RoHS Compliant



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MARKING DIAGRAMS



A = Assembly Location
 WL, L = Wafer Lot
 YY, Y = Year
 WW, W = Work Week
 G or ▪ = Pb-Free Package
 (Note: Microdot may be in either location)

FUNCTION TABLE

| INPUTS | | | OUTPUT |
|-----------------|----|---|-----------|
| \overline{OE} | LE | D | Q |
| L | H | H | H |
| L | H | L | L |
| L | L | X | No Change |
| H | X | X | Z |

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

MC74VHCT573A

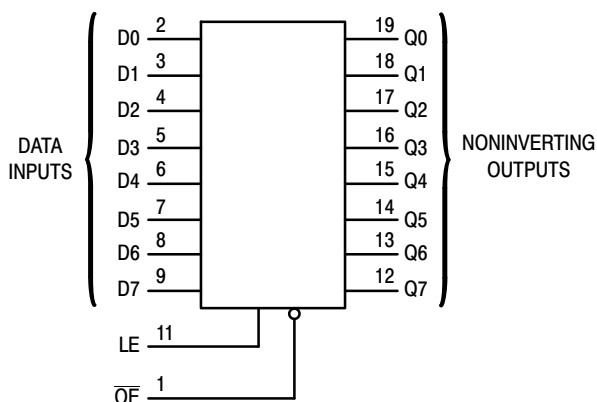


Figure 1. Logic Diagram

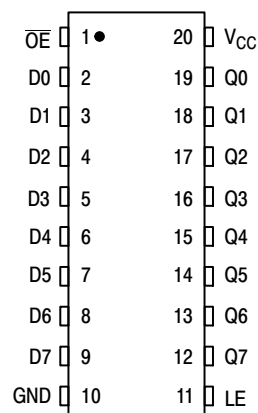


Figure 2. Pin Assignment

MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|-----------|--|---|------|
| V_{CC} | DC Supply Voltage | - 0.5 to + 7.0 | V |
| V_{in} | DC Input Voltage | - 0.5 to + 7.0 | V |
| V_{out} | DC Output Voltage Outputs in 3-State High or Low State | - 0.5 to + 7.0 - 0.5 to $V_{CC} + 0.5$ | V |
| I_{IK} | Input Diode Current | - 20 | mA |
| I_{OK} | Output Diode Current ($V_{OUT} < GND$; $V_{OUT} > V_{CC}$) | ± 20 | mA |
| I_{out} | DC Output Current, per Pin | ± 25 | mA |
| I_{CC} | DC Supply Current, V_{CC} and GND Pins | ± 75 | mA |
| P_D | Power Dissipation in Still Air, SOIC Package† TSSOP Package† | 500 450 | mW |
| T_{stg} | Storage Temperature | - 65 to + 150 | °C |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

†Derating - SOIC Packages: - 7 mW/°C from 65° to 125°C
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|------------|--|--------|-----------------|------|
| V_{CC} | DC Supply Voltage | 4.5 | 5.5 | V |
| V_{in} | DC Input Voltage | 0 | 5.5 | V |
| V_{out} | DC Output Voltage Outputs in 3-State High or Low State | 0 0 | 5.5 V_{CC} | V |
| T_A | Operating Temperature | - 40 | + 85 | °C |
| t_r, t_f | Input Rise and Fall Time $V_{CC} = 5.0V \pm 0.5V$ | 0 | 20 | ns/V |

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DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test Conditions | V _{CC} V | T _A = 25°C | | | T _A = -40 to 85°C | | Unit |
|------------------|---|---|----------------------|-----------------------|-----|-------|------------------------------|------|------|
| | | | | Min | Typ | Max | Min | Max | |
| V _{IH} | Minimum High-Level Input Voltage | | 4.5 to 5.5 | 2.0 | | | 2.0 | | V |
| V _{IL} | Maximum Low-Level Input Voltage | | 4.5 to 5.5 | | | 0.8 | | 0.8 | V |
| V _{OH} | Minimum High-Level Output Voltage V _{in} = V _{IH} or V _{IL} | I _{OH} = -50μA | 4.5 | 4.4 | 4.5 | | 4.4 | | V |
| | | I _{OH} = -8mA | 4.5 | 3.94 | | | 3.80 | | |
| V _{OL} | Maximum Low-Level Output Voltage V _{in} = V _{IH} or V _{IL} | I _{OL} = 50μA | 4.5 | | 0.0 | 0.1 | | 0.1 | V |
| | | I _{OL} = 8mA | 4.5 | | | 0.36 | | 0.44 | |
| I _{in} | Maximum Input Leakage Current | V _{in} = 5.5 V or GND | 0 to 5.5 | | | ±0.1 | | ±1.0 | μA |
| I _{OZ} | Maximum 3-State Leakage Current | V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND | 5.5 | | | ±0.25 | | ±2.5 | μA |
| I _{CC} | Maximum Quiescent Supply Current | V _{in} = V _{CC} or GND | 5.5 | | | 4.0 | | 40.0 | μA |
| I _{CCT} | Quiescent Supply Current | Per Input: V _{IN} = 3.4V Other Input: V _{CC} or GND | 5.5 | | | 1.35 | | 1.50 | mA |
| I _{OPD} | Output Leakage Current | V _{OUT} = 5.5V | 0 | | | 0.5 | | 5.0 | μA |

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3.0ns)

| Symbol | Parameter | Test Conditions | T _A = 25°C | | | T _A = -40 to 85°C | | Unit |
|--|--|--|-----------------------|------------|--------------|------------------------------|--------------|------|
| | | | Min | Typ | Max | Min | Max | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, LE to Q | V _{CC} = 5.0 ± 0.5V C _L = 15pF C _L = 50pF | | 7.7 8.5 | 12.3 13.3 | 1.0 1.0 | 13.5 14.5 | ns |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, D to Q | V _{CC} = 5.0 ± 0.5V C _L = 15pF C _L = 50pF | | 5.1 5.9 | 8.5 9.5 | 1.0 1.0 | 9.5 10.5 | ns |
| t _{PZL} , t _{PZH} | Output Enable Time, OE to Q | V _{CC} = 5.0 ± 0.5V R _L = 1kΩ C _L = 50pF | | 6.3 7.1 | 10.9 11.9 | 1.0 1.0 | 12.5 13.5 | ns |
| t _{PLZ} , t _{PHZ} | Output Disable Time, OE to Q | V _{CC} = 5.0 ± 0.5V R _L = 1kΩ C _L = 50pF | | 8.8 | 11.2 | 1.0 | 12.0 | ns |
| t _{OSLH} , t _{OSHL} | Output to Output Skew | V _{CC} = 5.5 ± 0.5V C _L = 50pF (Note 1) | | | 1.0 | | 1.0 | ns |
| C _{in} | Maximum Input Capacitance | | | 4 | 10 | | 10 | pF |
| C _{out} | Maximum 3-State Output Capacitance (Output in High-Impedance State) | | | 6 | | | | pF |
| C _{PD} | Power Dissipation Capacitance (Note 2) | Typical @ 25°C, V _{CC} = 5.0V | | | | | | pF |
| | | 25 | | | | | | |

- Parameter guaranteed by design. t_{OSLH} = |t_{PLHm} - t_{PLHn}|, t_{OSHL} = |t_{PHLm} - t_{PHLn}|.
- C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}/8 (per latch). C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

NOISE CHARACTERISTICS (Input t_r = t_f = 3.0ns, C_L = 50 pF, V_{CC} = 5.0V)

| Symbol | Parameter | T _A = 25°C | | Unit |
|------------------|--|-----------------------|------|------|
| | | Typ | Max | |
| V _{OLP} | Quiet Output Maximum Dynamic V _{OL} | 1.2 | 1.6 | V |
| V _{OLV} | Quiet Output Minimum Dynamic V _{OL} | -1.2 | -1.6 | V |
| V _{IHD} | Minimum High Level Dynamic Input Voltage | | 2.0 | V |
| V _{ILD} | Maximum Low Level Dynamic Input Voltage | | 0.8 | V |

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TIMING REQUIREMENTS (Input $t_r = t_f = 3.0\text{ns}$)

| Symbol | Parameter | Test Conditions | $T_A = 25^\circ\text{C}$ | | $T_A = -40 \text{ to } 85^\circ\text{C}$ | Unit |
|------------|-----------------------------|--------------------------------|--------------------------|-------|--|------|
| | | | Typ | Limit | Limit | |
| $t_{w(h)}$ | Minimum Pulse Width, LE | $V_{CC} = 5.0 \pm 0.5\text{V}$ | | 6.5 | 8.5 | ns |
| t_{su} | Minimum Setup Time, D to LE | $V_{CC} = 5.0 \pm 0.5\text{V}$ | | 1.5 | 1.5 | ns |
| t_h | Minimum Hold Time, D to LE | $V_{CC} = 5.0 \pm 0.5\text{V}$ | | 3.5 | 3.5 | ns |

ORDERING INFORMATION

| Device | Package | Shipping [†] |
|------------------|------------------------|-----------------------|
| MC74VHCT573ADWG | SOIC-20WB (Pb-Free) | 38 Units / Rail |
| MC74VHCT573ADWRG | SOIC-20WB (Pb-Free) | 1000 / Tape & Reel |
| MC74VHCT573ADTG | TSSOP-20* | 75 Units / Rail |
| MC74VHCT573ADTRG | TSSOP-20* | 2500 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

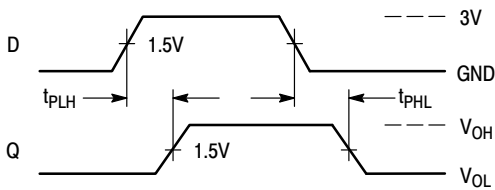


Figure 3. Switching Waveform

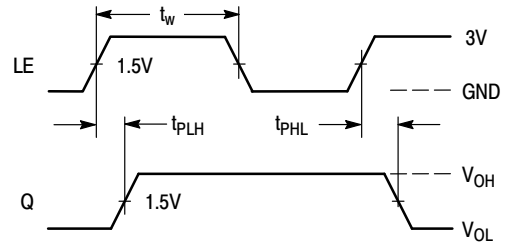


Figure 4. Switching Waveform

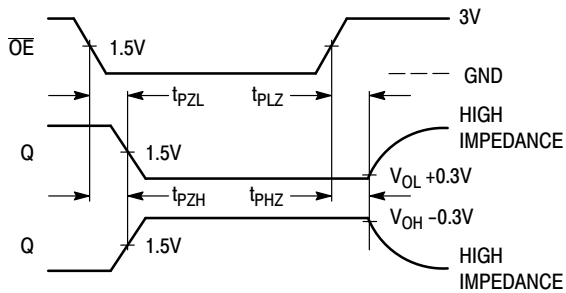


Figure 5. Switching Waveform

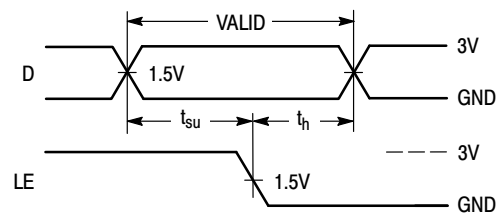
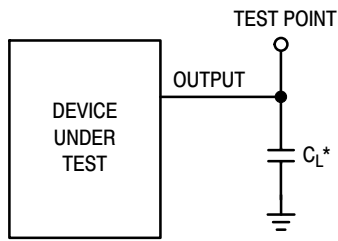


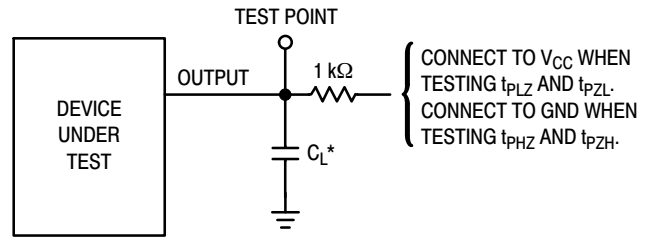
Figure 6. Switching Waveform

MC74VHCT573A



*Includes all probe and jig capacitance

Figure 7. Test Circuit



*Includes all probe and jig capacitance

Figure 8. Test Circuit

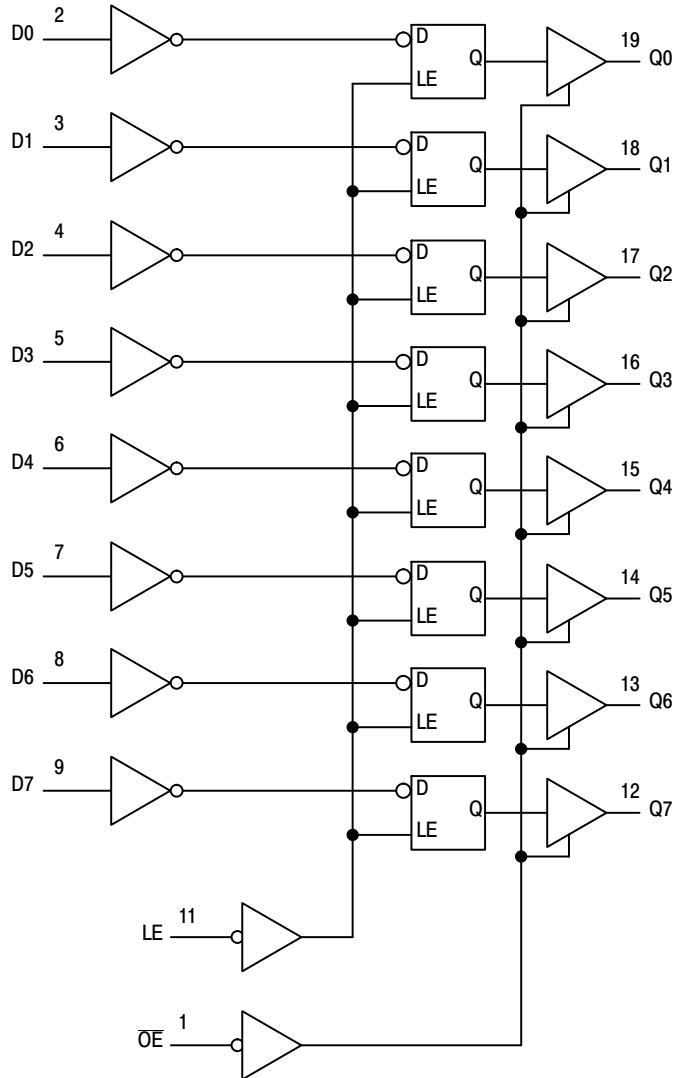


Figure 9. Expanded Logic Diagram

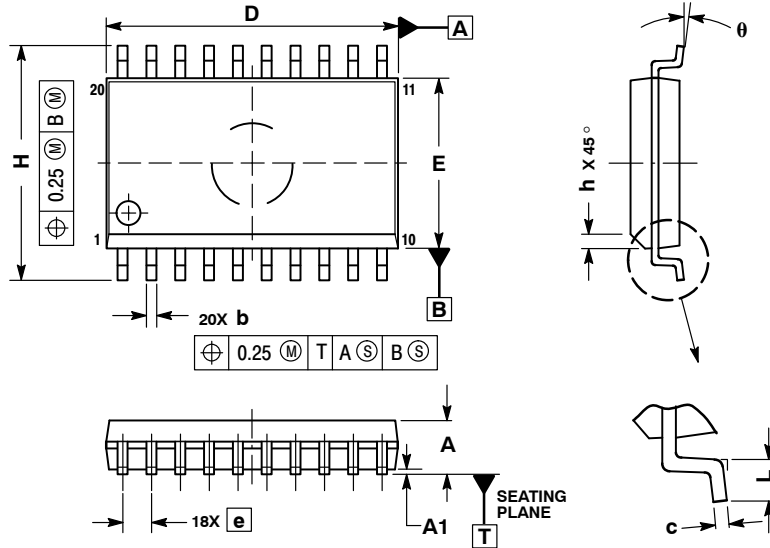
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-20 WB
CASE 751D-05
ISSUE H

DATE 22 APR 2015

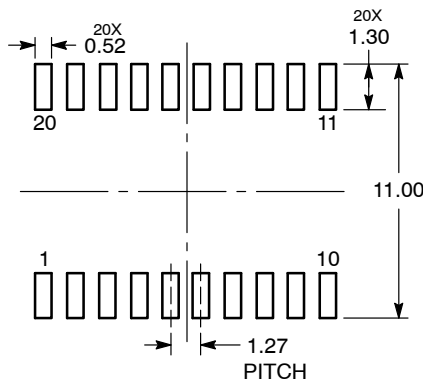


NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | |
|-----|-------------|-------|
| | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| b | 0.35 | 0.49 |
| c | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| θ | 0° | 7° |

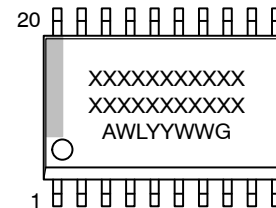
RECOMMENDED
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



TSSOP-20 WB
CASE 948E
ISSUE D

DATE 17 FEB 2016

SCALE 2:1



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 6.40 | 6.60 | 0.252 | 0.260 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.27 | 0.37 | 0.011 | 0.015 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |



SOLDERING FOOTPRINT



GENERIC MARKING DIAGRAM*



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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