LDO Regulator - Ultra-Low Noise, High PSRR, RF and Analog Circuits

450 mA

NCP148

The NCP148 is a linear regulator capable of supplying 450 mA output current. Designed to meet the requirements of RF and analog circuits, the NCP148 device provides low noise, high PSRR, low quiescent current, and very good load/line transients. The NCP148 offers soft−start function with optimized slew rate control to use in camera module. The device is designed to work with a 1 μF input and a 1 μF output ceramic capacitor. It is available in ultra−small 0.35P, 0.64 mm x 0.64 mm Chip Scale Package (CSP).

Features

- Operating Input Voltage Range: 1.9 V to 5.5 V
- Available in Fixed Voltage Option: 1.8 V to 5.14 V
- Optimized Start−up Slew Rate for Camera Sensor
- ±2% Accuracy Over Load/Temperature
- Low Quiescent Current Typ. 55 μA
- Standby Current: Typ. 0.1 μA
- Very Low Dropout: 150 mV at 450 mA
- Ultra High PSRR: Typ. 98 dB at 20 mA, f = 1 kHz
- Ultra Low Noise: 10 μV_{RMS}
- Stable with a 1 μF Small Case Size Ceramic Capacitors
- Available in WLCSP4 0.64 mm x 0.64 mm x 0.33 mm CASE 567JZ
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Camera Modules
- Battery−powered Equipment
- Smartphones, Tablets
- Cameras, DVRs, STB and Camcorders

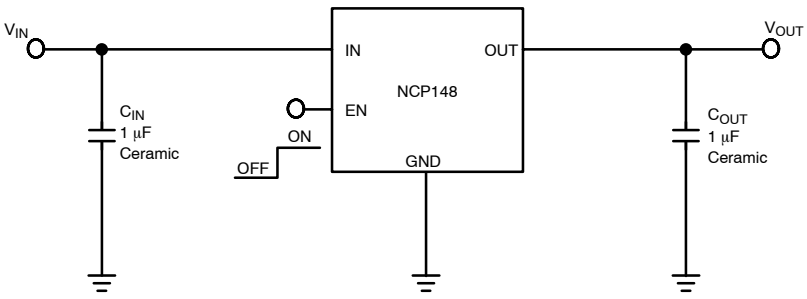
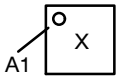


Figure 1. Typical Application Schematics

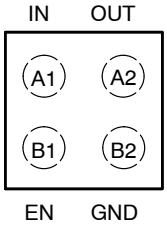
WLCSP4
CASE 567JZ

MARKING DIAGRAM



X = Specific Device Code
M = Date Code

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 12 of this data sheet.

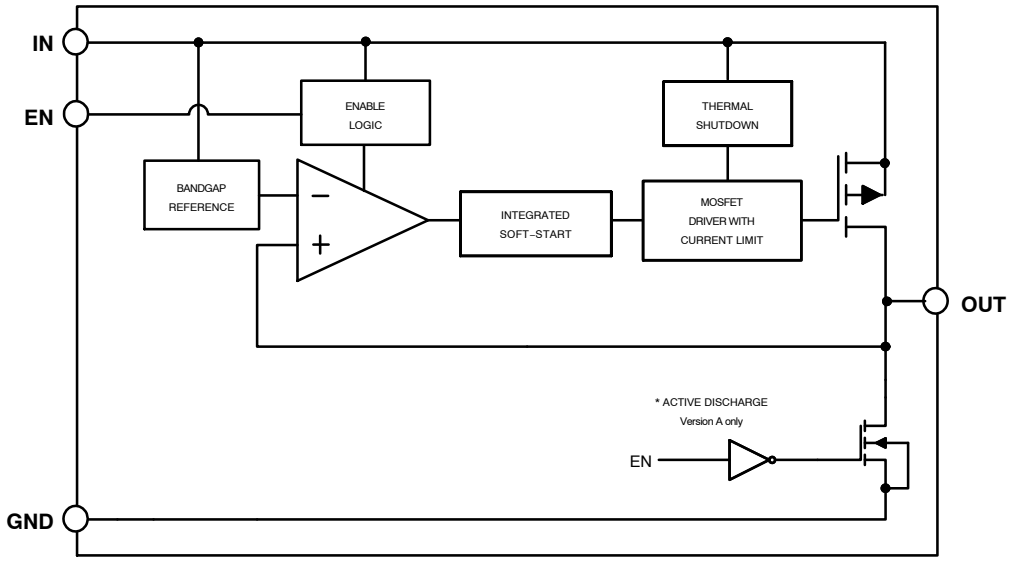


Figure 2. Simplified Schematic Block Diagram

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
A1	IN	Input voltage supply pin
A2	OUT	Regulated output voltage. The output should be bypassed with small 1 μF ceramic capacitor.
B1	EN	Chip enable: Applying V_{EN} < 0.4 V disables the regulator, Pulling V_{EN} > 1.2 V enables the LDO.
B2	GND	Common ground connection
–	EPAD	Expose pad should be tied to ground plane for better power dissipation

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN}	−0.3 to 6	V
Output Voltage	V_{OUT}	−0.3 to V_{IN} + 0.3, max. 6	V
Chip Enable Input	V_{CE}	−0.3 to 6	V
Output Short Circuit Duration	t_{SC}	unlimited	s
Maximum Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	−55 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per EIA/JESD22−A114
   ESD Machine Model tested per EIA/JESD22−A115
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, CSP4 (Note 3) Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	108	°C/W

3. Measured according to JEDEC board specification. Detailed description of the board can be found in JESD51−7

ELECTRICAL CHARACTERISTICS $-40°C \le T_J \le 125°C$; $V_{IN} = V_{OUT(NOM)} + 1$ V; $I_{OUT} = 1$ mA, $C_{IN} = C_{OUT} = 1$ μF, unless otherwise noted. $V_{EN} = 1.2$ V. Typical values are at $T_J = +25°C$ (Note 4).

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Operating Input Voltage			V_{IN}	1.9		5.5	V
Output Voltage Accuracy	$V_{IN} = V_{OUT(NOM)} + 1$ V 0 mA ≤ I_{OUT} ≤ 450 mA		V_{OUT}	−2		+2	%
Line Regulation	$V_{OUT(NOM)} + 1$ V ≤ V_{IN} ≤ 5.5 V		$Line_{Reg}$		0.02		%/V
Load Regulation	I_{OUT} = 1 mA to 450 mA		$Load_{Reg}$		0.001		%/mA
Dropout Voltage (Note 5)	I_{OUT} = 450 mA	$V_{OUT(NOM)}$ = 1.8 V	V_{DO}		300	450	mV
		$V_{OUT(NOM)}$ = 2.5 V			190	315	
		$V_{OUT(NOM)}$ = 2.7 V			180	300	
		$V_{OUT(NOM)}$ = 2.8 V			175	290	
Output Current Limit	V_{OUT} = 90% $V_{OUT(NOM)}$		I_{CL}	450	700		mA
Short Circuit Current	V_{OUT} = 0 V		I_{SC}		690		
Quiescent Current	I_{OUT} = 0 mA		I_Q		55	65	μA
Shutdown Current	$V_{EN} \le 0.4$ V, V_{IN} = 4.8 V		I_{DIS}		0.01	1	μA
EN Pin Threshold Voltage	EN Input Voltage “H”		V_{ENH}	1.2			V
	EN Input Voltage “L”		V_{ENL}			0.4	
EN Pull Down Current	V_{EN} = 4.8 V		I_{EN}		0.2	0.5	μA
Power Supply Rejection Ratio	I_{OUT} = 20 mA	f = 100 Hz f = 1 kHz f = 10 kHz f = 100 kHz	PSRR		91 98 82 48		dB
Output Voltage Noise	f = 10 Hz to 100 kHz	I_{OUT} = 1 mA I_{OUT} = 250 mA	V_N		14 10		μV_{RMS}
Thermal Shutdown Threshold	Temperature rising		T_{SDH}		160		°C
	Temperature falling		T_{SDL}		140		°C
Active output discharge resistance	V_{EN} < 0.4 V, Version A only		R_{DIS}		280		Ω
Line transient (Note 6)	$V_{IN} = (V_{OUT(NOM)} + 1$ V) to ($V_{OUT(NOM)}$ + 1.6 V) in 30 μs, I_{OUT} = 1 mA		$Tran_{LINE}$	−1			mV
	$V_{IN} = (V_{OUT(NOM)} + 1.6$ V) to ($V_{OUT(NOM)}$ + 1 V) in 30 μs, I_{OUT} = 1 mA					+1	
Load transient (Note 6)	I_{OUT} = 1 mA to 450 mA in 10 μs		$Tran_{LOAD}$	−40			mV
	I_{OUT} = 450 mA to 1mA in 10 μs					+40	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at $T_A = 25°C$. Low duty cycle pulse techniques are used during the testing to maintain the junction temperature as close to ambient as possible.
5. Dropout voltage is characterized when V_{OUT} falls 100 mV below $V_{OUT(NOM)}$.
6. Guaranteed by design.

TYPICAL CHARACTERISTICS

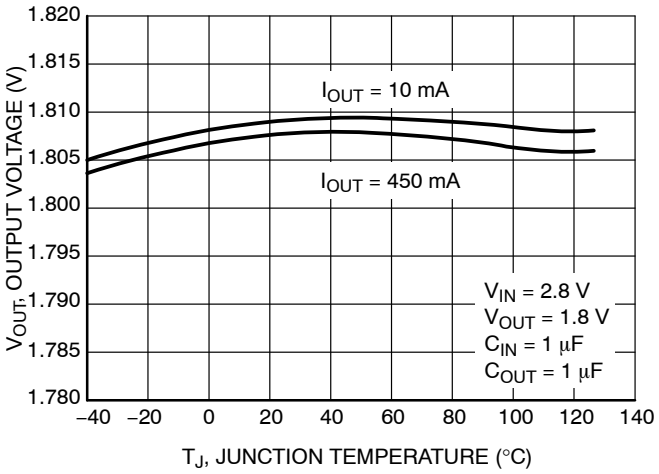


Figure 3. Output Voltage vs. Temperature – V_{OUT} = 1.8 V

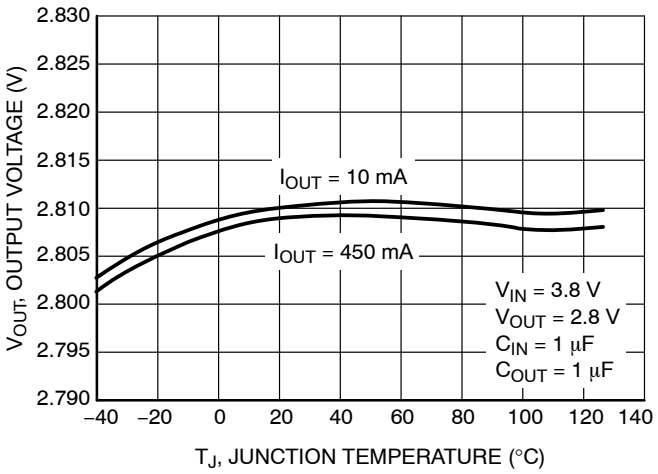


Figure 4. Output Voltage vs. Temperature – V_{OUT} = 2.8 V

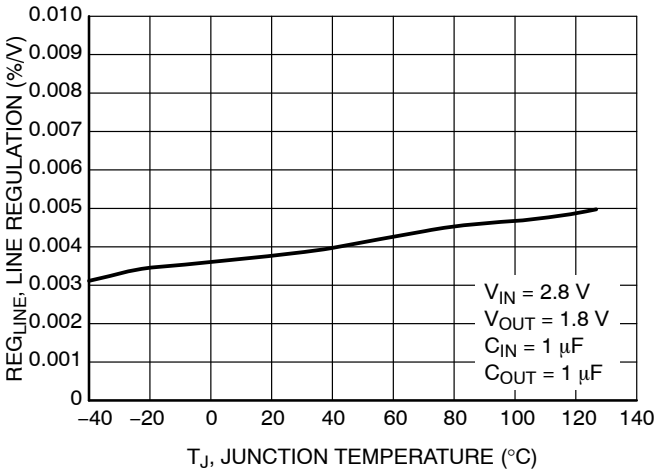


Figure 5. Line Regulation vs. Temperature – V_{OUT} = 1.8 V

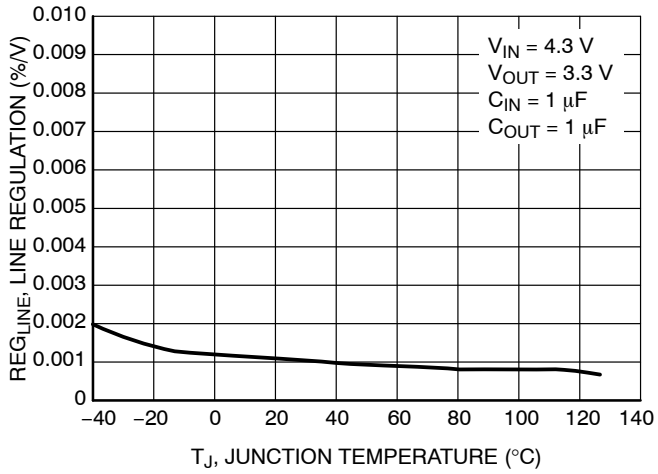


Figure 6. Line Regulation vs. Temperature – V_{OUT} = 2.8 V

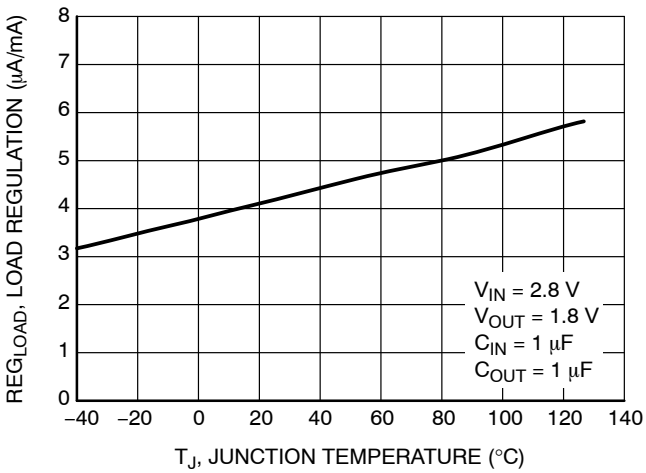


Figure 7. Load Regulation vs. Temperature – V_{OUT} = 1.8 V

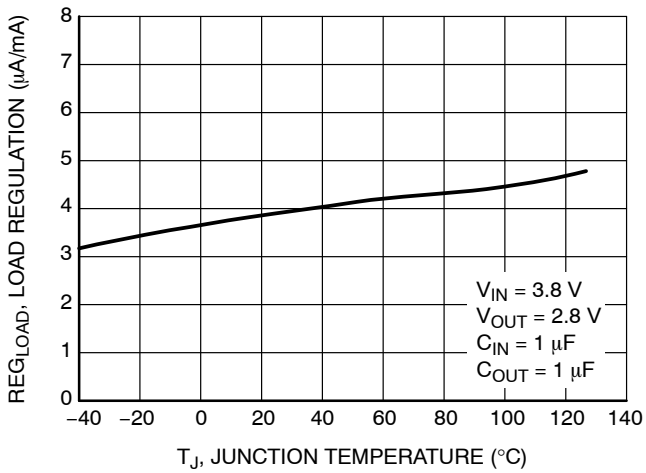


Figure 8. Load Regulation vs. Temperature – V_{OUT} = 2.8 V

TYPICAL CHARACTERISTICS

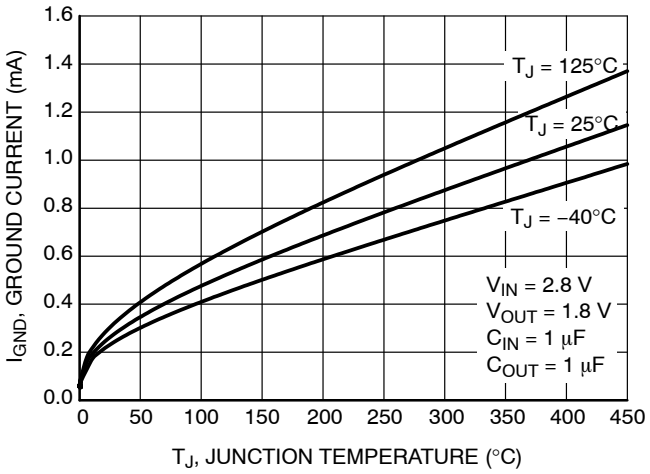


Figure 9. Ground Current vs. Load Current – V_{OUT} = 1.8 V

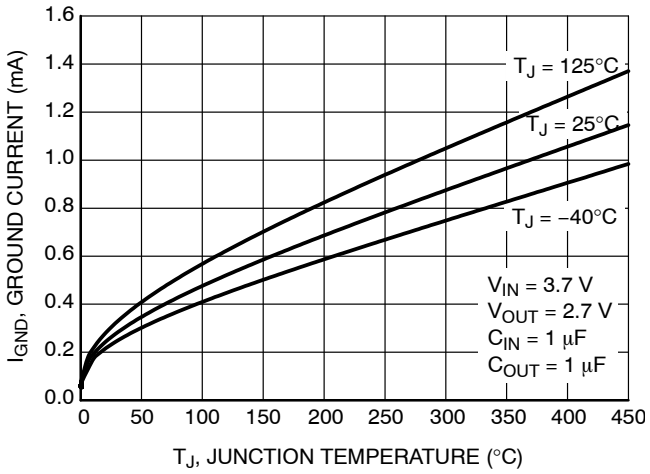


Figure 10. Ground Current vs. Load Current – V_{OUT} = 2.7 V

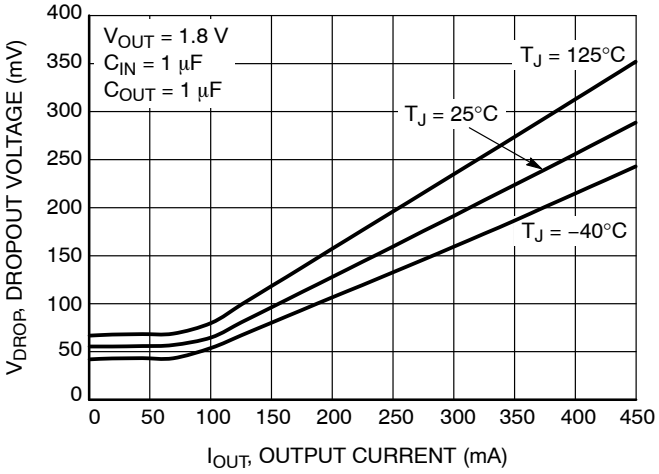


Figure 11. Dropout Voltage vs. Load Current – V_{OUT} = 1.8 V

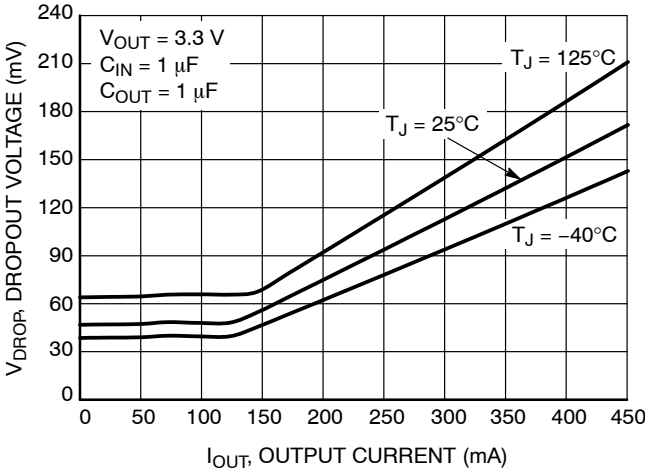


Figure 12. Dropout Voltage vs. Load Current – V_{OUT} = 2.8 V

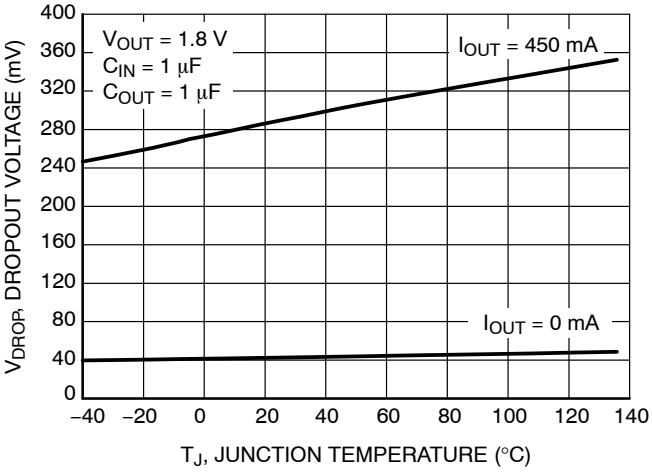


Figure 13. Dropout Voltage vs. Temperature – V_{OUT} = 1.8 V

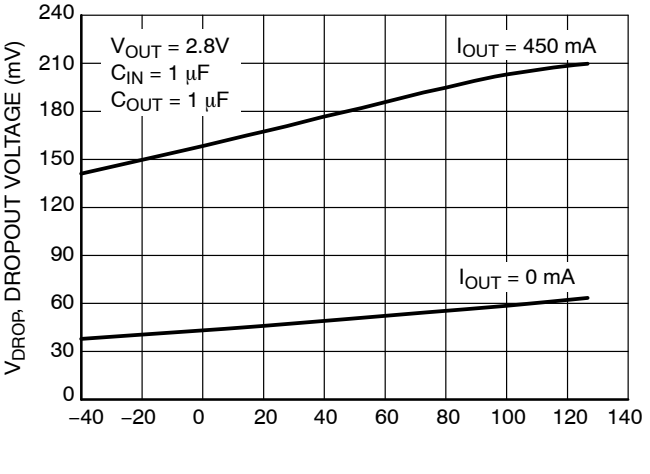


Figure 14. Dropout Voltage vs. Temperature – V_{OUT} = 2.8 V

TYPICAL CHARACTERISTICS

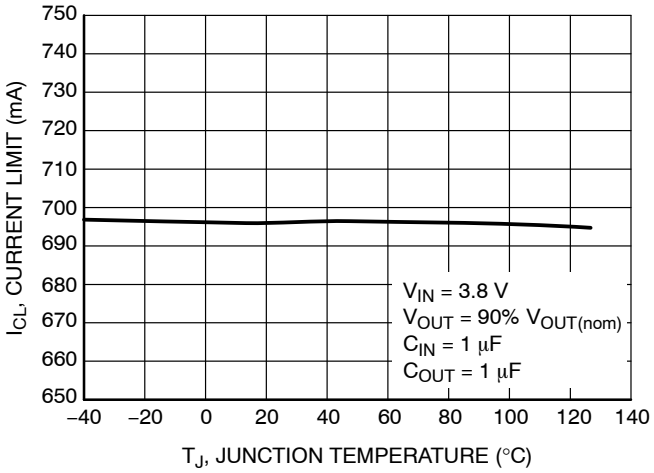


Figure 15. Current Limit vs. Temperature

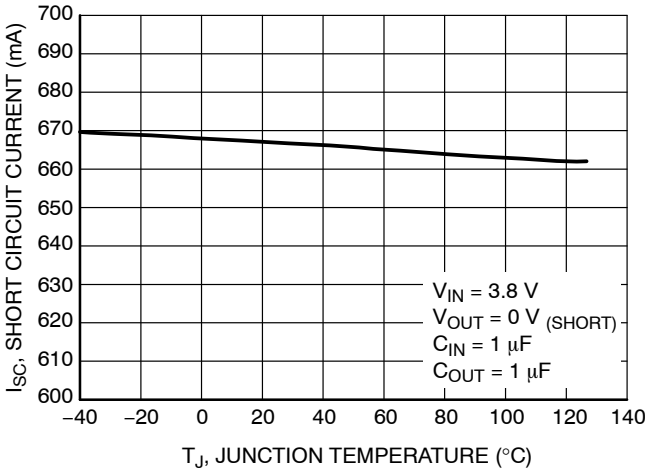


Figure 16. Short Circuit Current vs. Temperature

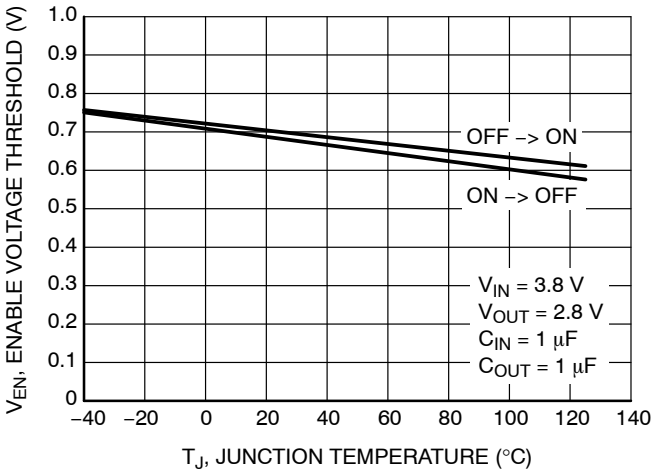


Figure 17. Enable Threshold Voltage vs. Temperature

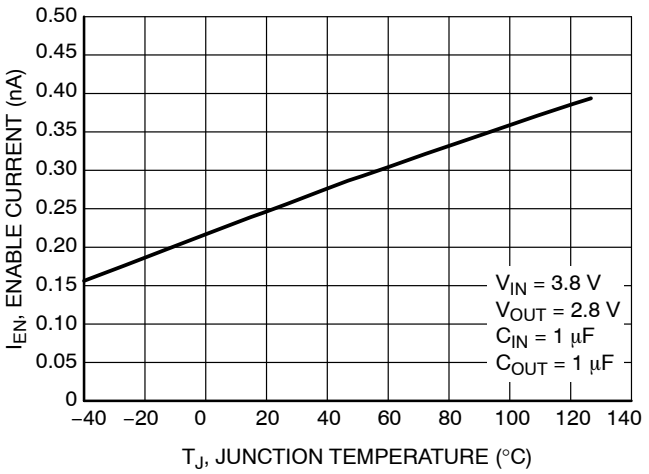


Figure 18. Enable Current vs. Temperature

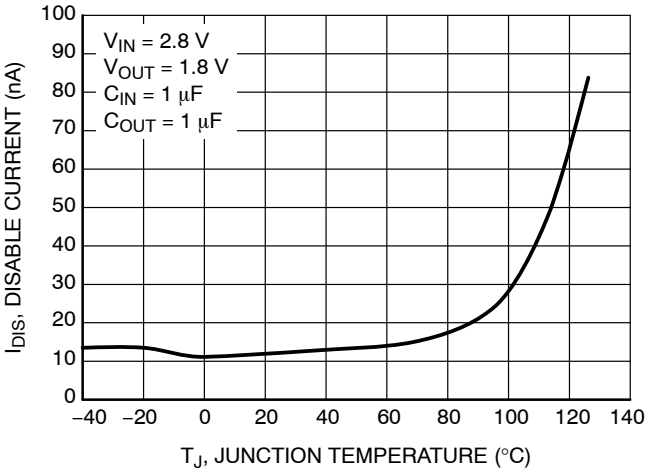


Figure 19. Disable Current vs. Temperature

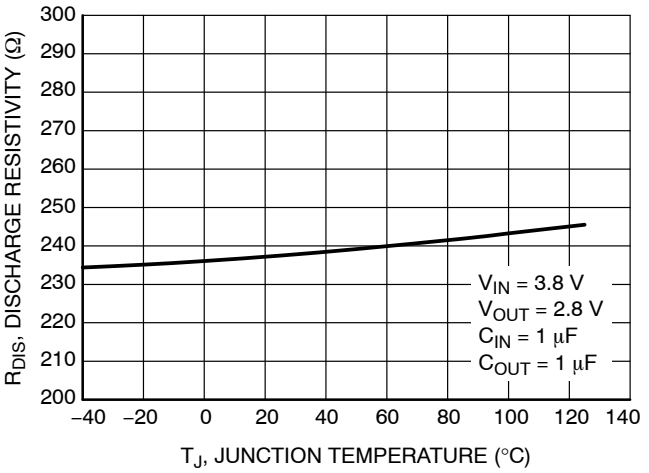
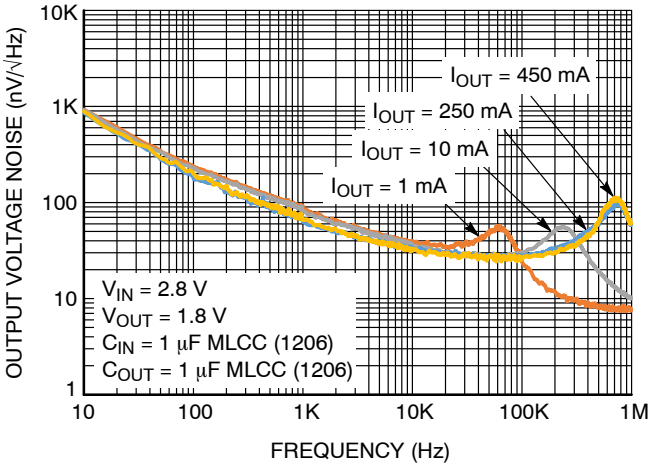


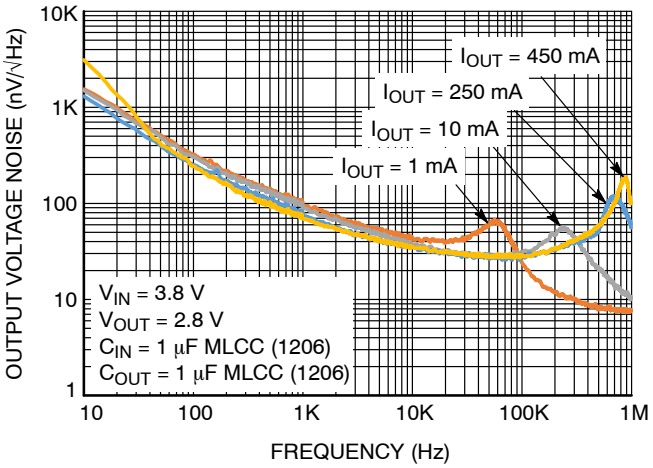
Figure 20. Discharge Resistivity vs. Temperature

TYPICAL CHARACTERISTICS



I_{OUT}	RMS Output Noise (μV)	
	10 Hz – 100 kHz	100 Hz – 100 kHz
1 mA	14.62	14.10
10 mA	11.12	10.48
250 mA	10.37	9.82
450 mA	10.22	9.62

Figure 21. Output Voltage Noise Spectral Density – V_{OUT} = 1.8 V



I_{OUT}	RMS Output Noise (μV)	
	10 Hz – 100 kHz	100 Hz – 100 kHz
1 mA	16.90	15.79
10 mA	12.64	11.13
250 mA	11.96	10.64
450 mA	11.50	10.40

Figure 22. Output Voltage Noise Spectral Density – V_{OUT} = 2.8 V

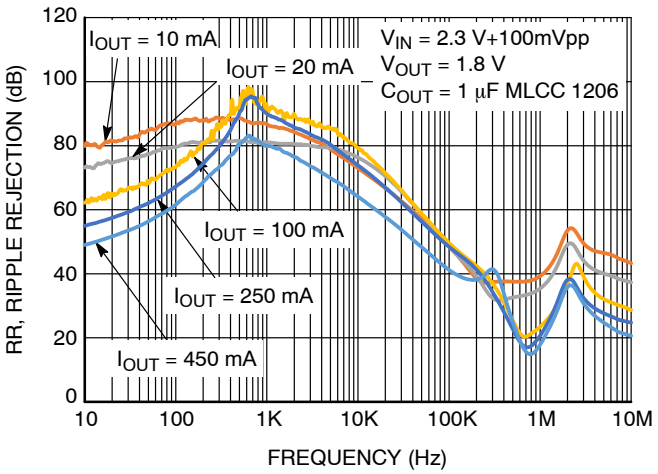


Figure 23. PSRR for Various Output Currents, V_{OUT} = 1.8 V

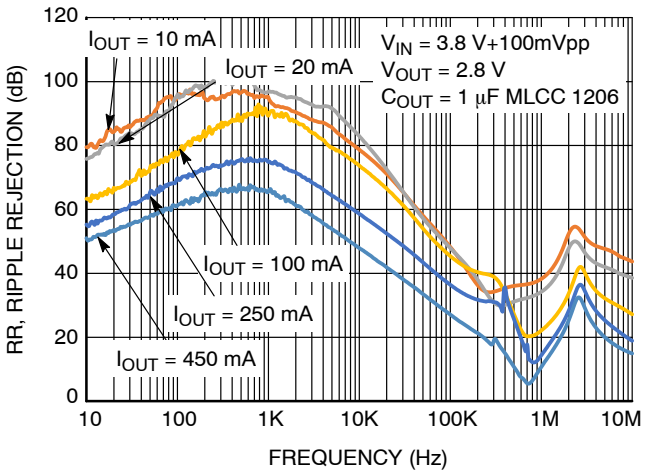


Figure 24. PSRR for Various Output Currents, V_{OUT} = 2.8 V

TYPICAL CHARACTERISTICS

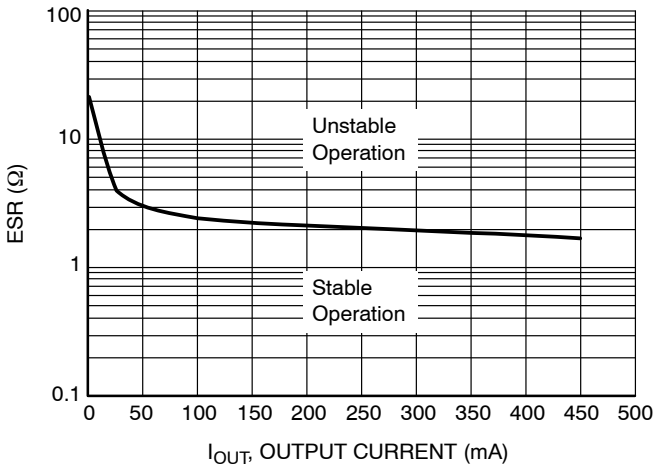


Figure 25. Stability vs. ESR

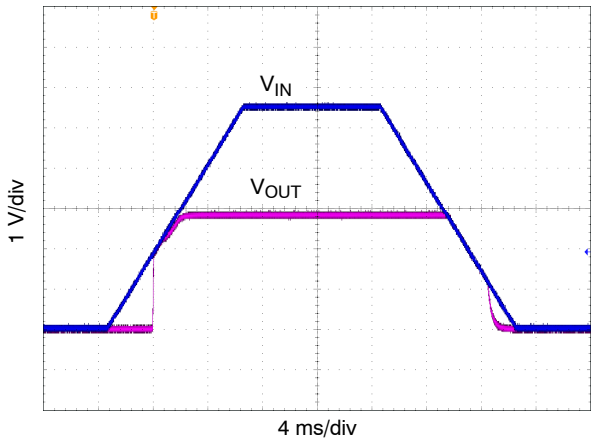


Figure 26. Turn−on/off − slow rising V_{IN}

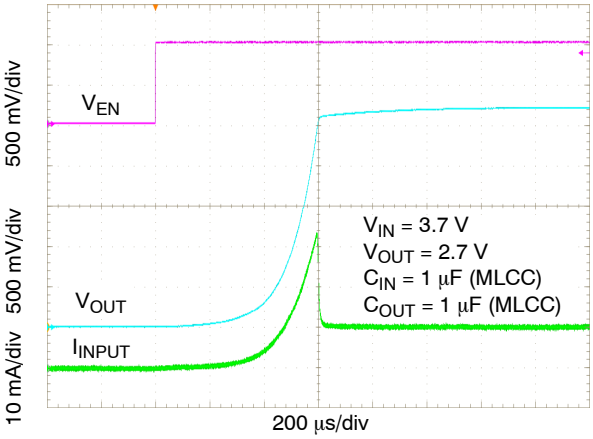


Figure 27. Enable Turn−on Response − C_{OUT} = 1 μF, I_{OUT} = 10 mA

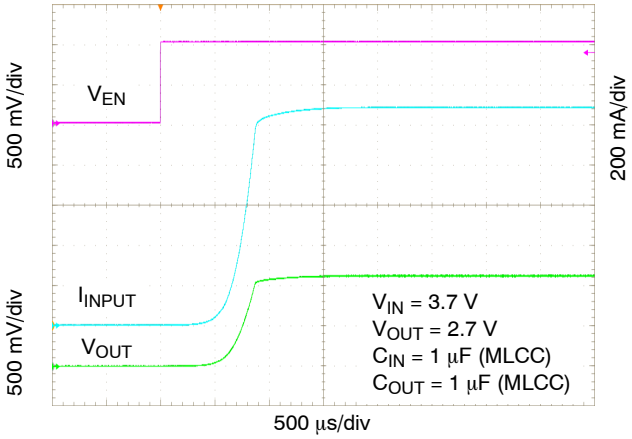


Figure 28. Enable Turn−on Response − C_{OUT} = 1 μF, I_{OUT} = 450 mA

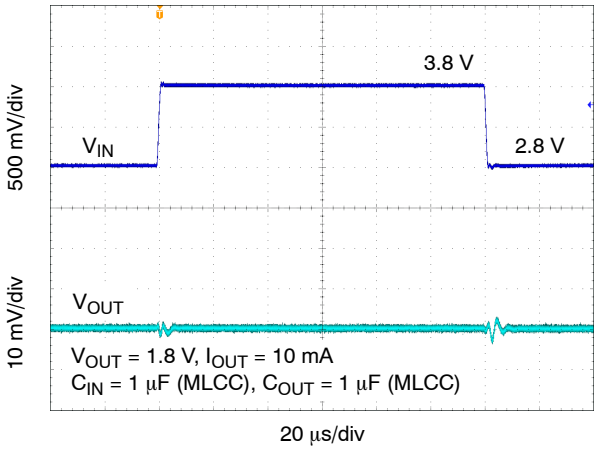


Figure 29. Line Transient Response − V_{OUT} = 1.8 V

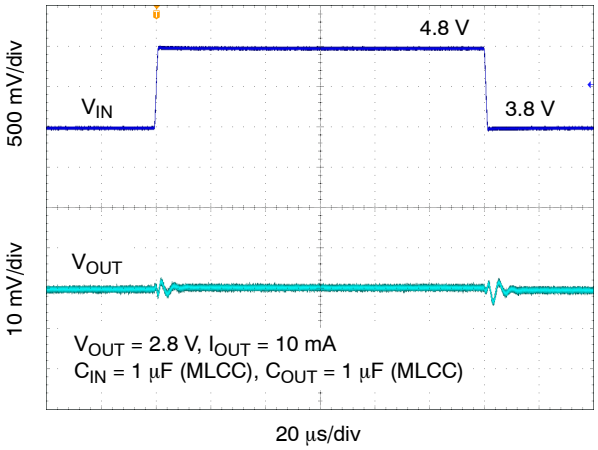


Figure 30. Line Transient Response − V_{OUT} = 2.8 V

TYPICAL CHARACTERISTICS

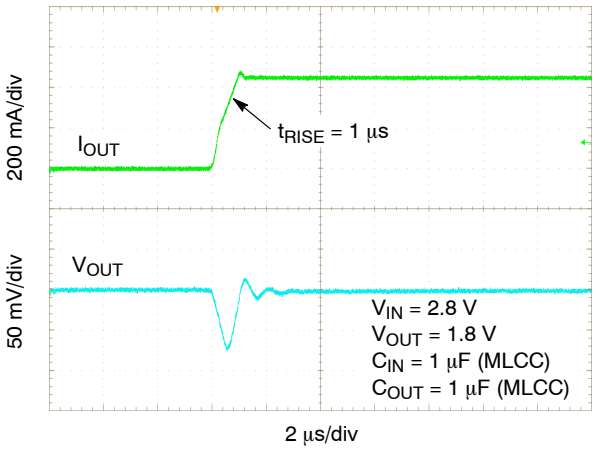


Figure 31. Load Transient Response – 1 mA to 450 mA – V_{OUT} = 1.8 V

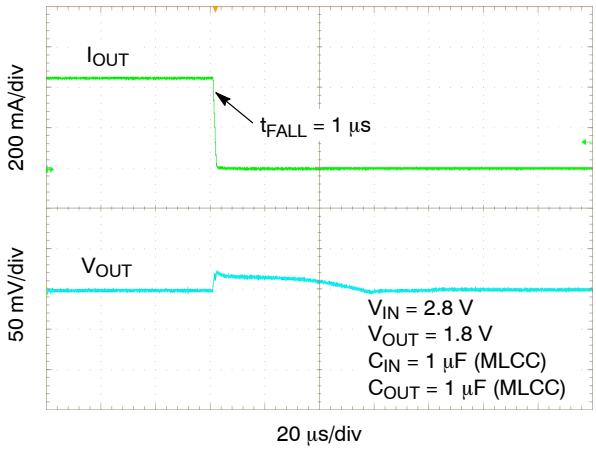


Figure 32. Load Transient Response – 450 mA to 1 mA – V_{OUT} = 1.8 V

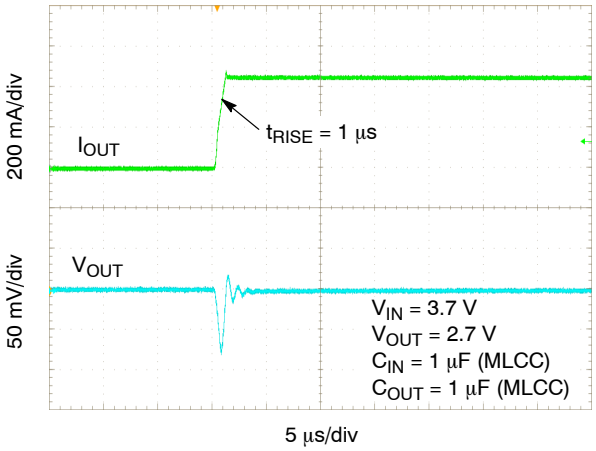


Figure 33. Load Transient Response – 1 mA to 450 mA – V_{OUT} = 2.7 V

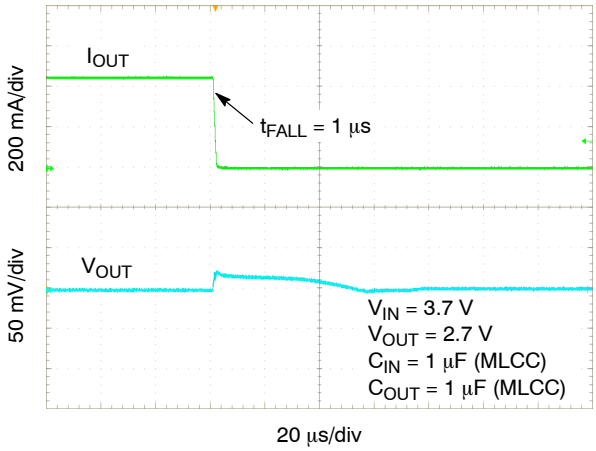


Figure 34. Load Transient Response – 450 mA to 1 mA – V_{OUT} = 2.7 V

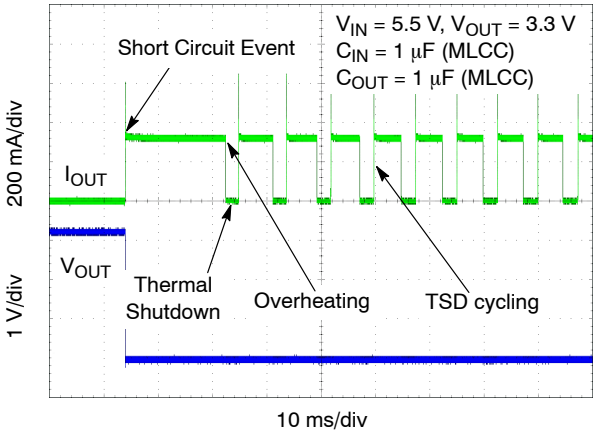


Figure 35. Short Circuit and Thermal Shutdown

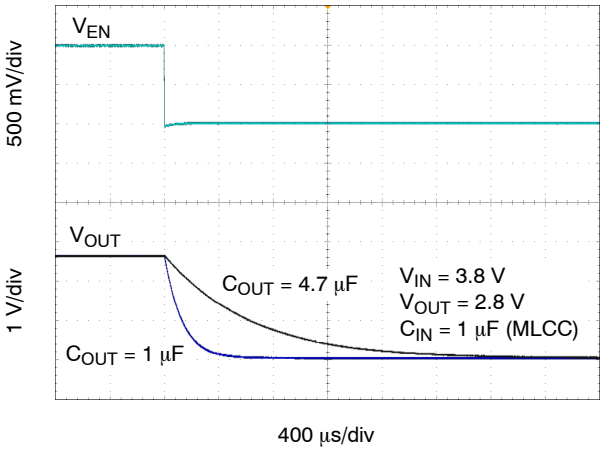


Figure 36. Enable Turn−Off (Active Discharge)

APPLICATIONS INFORMATION

General

The NCP148 is an ultra−low noise 450 mA low dropout regulator designed to meet the requirements of RF applications and high performance analog circuits. The NCP148 device provides very high PSRR and excellent dynamic response. In connection with low quiescent current this device is well suitable for battery powered application such as cell phones, tablets and other. The NCP148 is fully protected in case of current overload, output short circuit and overheating.

Input Capacitor Selection (C_{IN})

Input capacitor connected as close as possible is necessary for ensure device stability. The X7R or X5R capacitor should be used for reliable performance over temperature range. The value of the input capacitor should be 1 μF or greater to ensure the best dynamic performance. This capacitor will provide a low impedance path for unwanted AC signals or noise modulated onto constant input voltage. There is no requirement for the ESR of the input capacitor but it is recommended to use ceramic capacitors for their low ESR and ESL. A good input capacitor will limit the influence of input trace inductance and source resistance during sudden load current changes.

Output Decoupling (C_{OUT})

The NCP148 requires an output capacitor connected as close as possible to the output pin of the regulator. The recommended capacitor value is 1 μF and X7R or X5R dielectric due to its low capacitance variations over the specified temperature range. The NCP148 is designed to remain stable with minimum effective capacitance of 0.7 μF to account for changes with temperature, DC bias and package size. Especially for small package size capacitors such as 0201 the effective capacitance drops rapidly with the applied DC bias. Please refer Figure 37.

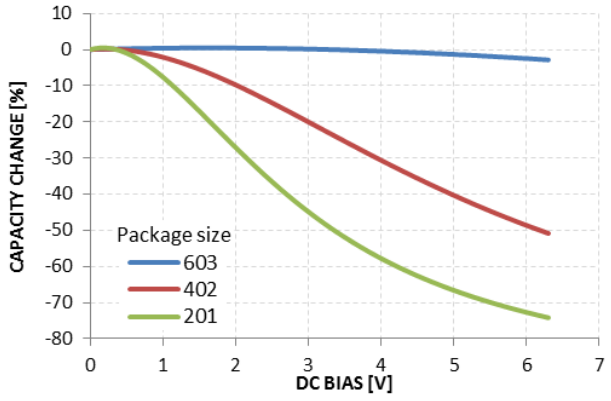


Figure 37. Capacity vs DC Bias Voltage

There is no requirement for the minimum value of Equivalent Series Resistance (ESR) for the C_{OUT} but the maximum value of ESR should be less than 2 Ω. Larger output capacitors and lower ESR could improve the load transient response or high frequency PSRR. It is not recommended to use tantalum capacitors on the output due to their large ESR. The equivalent series resistance of tantalum capacitors is also strongly dependent on the temperature, increasing at low temperature.

Enable Operation

The NCP148 uses the EN pin to enable/disable its device and to deactivate/activate the active discharge function.

If the EN pin voltage is <0.4 V the device is guaranteed to be disabled. The pass transistor is turned−off so that there is virtually no current flow between the IN and OUT. The active discharge transistor is active so that the output voltage V_{OUT} is pulled to GND through a 280 Ω resistor. In the disable state the device consumes as low as typ. 10 nA from the V_{IN}.

If the EN pin voltage >1.2 V the device is guaranteed to be enabled. The NCP148 regulates the output voltage and the active discharge transistor is turned−off.

The EN pin has internal pull−down current source with typ. value of 200 nA which assures that the device is turned−off when the EN pin is not connected. In the case where the EN function isn't required the EN should be tied directly to IN. After device is enabled by EN pin soft start feature ensure that maximal Vout slew rate will be slower than 30 mV/μs. The soft start function also protects powered device before possible damage by large inrush current.

Output Current Limit

Output Current is internally limited within the IC to a typical 700 mA. The NCP148 will source this amount of current measured with a voltage drops on the 90% of the nominal V_{OUT}. If the Output Voltage is directly shorted to ground (V_{OUT} = 0 V), the short circuit protection will limit the output current to 690 mA (typ). The current limit and short circuit protection will work properly over whole temperature range and also input voltage range. There is no limitation for the short circuit duration.

Thermal Shutdown

When the die temperature exceeds the Thermal Shutdown threshold (T_{SD} − 160°C typical), Thermal Shutdown event is detected and the device is disabled. The IC will remain in this state until the die temperature decreases below the Thermal Shutdown Reset threshold (T_{SDU} − 140°C typical). Once the IC temperature falls below the 140°C the LDO is enabled again. The thermal shutdown feature provides the protection from a catastrophic device failure due to accidental overheating. This protection is not intended to be used as a substitute for proper heat sinking.

Power Dissipation

As power dissipated in the NCP148 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad

configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part.

The maximum power dissipation the NCP148 can handle is given by:

$$P_{D(MAX)} = \frac{[125°C - T_A]}{\theta_{JA}} \quad \text{(eq. 1)}$$

The power dissipated by the NCP148 for given application conditions can be calculated from the following equations:

$$P_D \approx V_{IN} \cdot I_{GND} + I_{OUT}(V_{IN} - V_{OUT}) \quad \text{(eq. 2)}$$

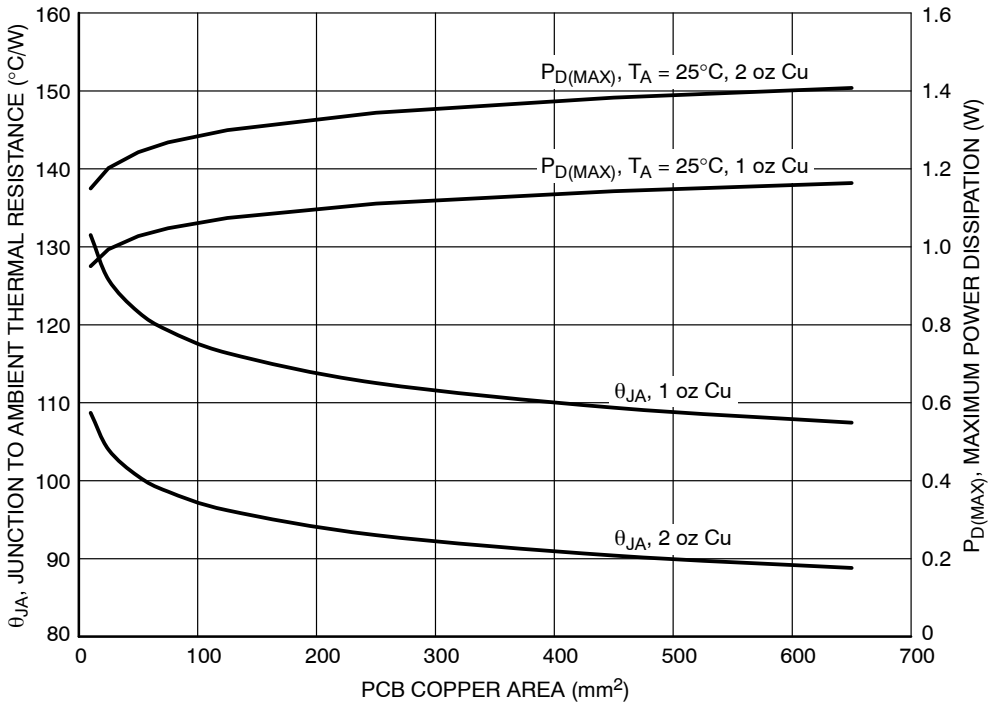


Figure 38. θ_{JA} and $P_{D\ (MAX)}$ vs. Copper Area (CSP4)

Reverse Current

The PMOS pass transistor has an inherent body diode which will be forward biased in the case that $V_{OUT} > V_{IN}$. Due to this fact in cases, where the extended reverse current condition can be anticipated the device may require additional external protection.

Power Supply Rejection Ratio

The NCP148 features very high Power Supply Rejection ratio. If desired the PSRR at higher frequencies in the range 100 kHz – 10 MHz can be tuned by the selection of C_{OUT} capacitor and proper PCB layout.

PCB Layout Recommendations

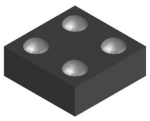
To obtain good transient performance and good regulation characteristics place C_{IN} and C_{OUT} capacitors close to the device pins and make the PCB traces wide. In order to minimize the solution size, use 0402 or 0201 capacitors with appropriate capacity. Larger copper area connected to the pins will also improve the device thermal resistance. The actual power dissipation can be calculated from the equation above (Equation 2). Expose pad can be tied to the GND pin for improvement power dissipation and lower device temperature.

ORDERING INFORMATION

Device	Nominal Output Voltage	Description	Marking	Rotation	Package	Shipping
NCP148AFCT180T2G	1.8 V	450 mA, Active Discharge	T	270°	567JZ	5000 / Tape & Reel
NCP148AFCT250T2G	2.5 V		V	0°		
NCP148AFCT255T2G	2.55 V		4	180°		
NCP148AFCT260T2G	2.6 V		V	90°		
NCP148AFCT270T2G	2.7 V		Y	0°		
NCP148AFCT280T2G	2.8 V		6	0°		
NCP148AFCT285T2G	2.85 V		4	0°		
NCP148AFCT320T2G	3.2 V		$\overline{T}$	0°		

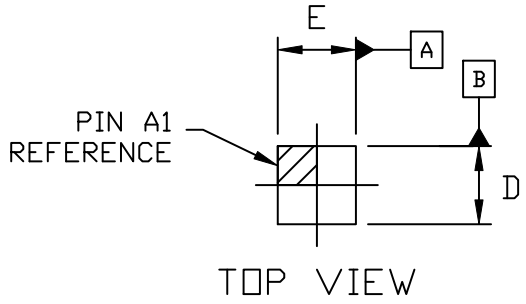
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

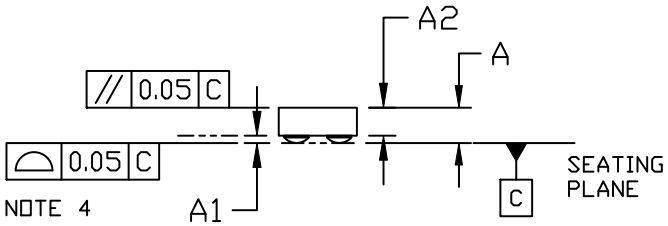


WLCSP4, 0.64x0.64x0.33
CASE 567JZ
ISSUE B

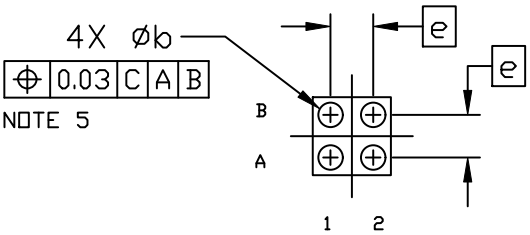
DATE 16 MAY 2022



TOP VIEW



SIDE VIEW

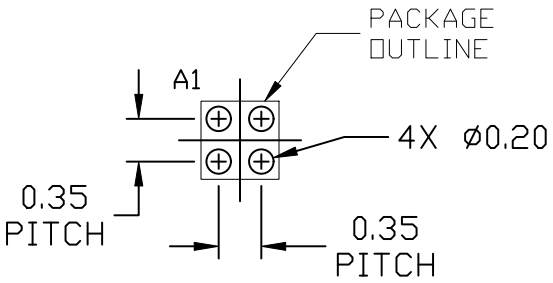


BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPERICAL CROWNS OF THE SOLDER BUMPS.
4. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BUMPS.
5. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM C.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	---	---	0.33
A1	0.04	0.06	0.08
A2	0.23 REF		
b	0.180	0.200	0.220
D	0.610	0.640	0.670
E	0.610	0.640	0.670
e	0.35 BSC		



RECOMMENDED
MOUNTING FOOTPRINT *
(NSMD PAD TYPE)

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*

X = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**WLCSP4, 0.64X0.64x0.33**	**PAGE 1 OF 1**

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