2N6107, 2N6109, 2N6111 (PNP), 2N6288, 2N6292 (NPN)

Complementary Silicon Plastic Power Transistors

These devices are designed for use in general−purpose amplifier and switching applications.

Features

- High DC Current Gain
- High Current Gain − Bandwidth Product
- TO−220 Compact Package
- These Devices are Pb−Free and are RoHS Compliant*

ON Semiconductor®

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7 AMPERE
POWER TRANSISTORS
COMPLEMENTARY SILICON
30 − 50 − 70 VOLTS, 40 WATTS

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Collector−Emitter Voltage 2N6111, 2N6288 2N6109 2N6107, 2N6292	V_{CEO}	 30 50 70	Vdc
Collector−Base Voltage 2N6111, 2N6288 2N6109 2N6107, 2N6292	V_{CB}	 40 60 80	Vdc
Emitter−Base Voltage	V_{EB}	5.0	Vdc
Collector Current − Continuous	I_C	7.0	Adc
Collector Current − Peak	I_{CM}	10	Adc
Base Current	I_B	3.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	 40 0.32	 W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

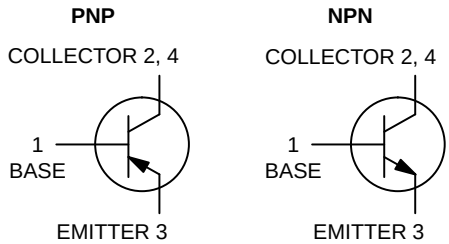
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

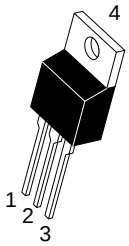
1. Indicates JEDEC Registered Data.

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	3.125	°C/W

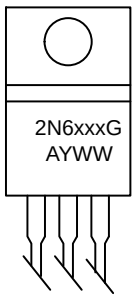
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.





TO−220
CASE 221A
STYLE 1

MARKING DIAGRAM



2N6xxx = Specific Device Code
xxx = See Table on Page 4
G = Pb−Free Package
A = Assembly Location
Y = Year
WW = Work Week

ORDERING INFORMATION

See detailed ordering, marking, and shipping information in the package dimensions section on page 4 of this data sheet.

November, 2014 − Rev. 11
Publication Order Number:
2N6107/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted) (Note 2)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (Note 3)	$V_{CEO(sus)}$			Vdc
(I_C = 100 mAdc, I_B = 0)				
2N6111, 2N6288		30	−	
2N6109		50	−	
2N6107, 2N6292		70	−	
Collector Cutoff Current	I_{CEO}			mAdc
(V_{CE} = 20 Vdc, I_B = 0)				
2N6111, 2N6288		−	1.0	
(V_{CE} = 40 Vdc, I_B = 0)				
2N6109		−	1.0	
(V_{CE} = 60 Vdc, I_B = 0)				
2N6107, 2N6292		−	1.0	
Collector Cutoff Current	I_{CEX}			
(V_{CE} = 40 Vdc, $V_{EB(off)}$ = 1.5 Vdc)				
2N6111, 2N6288		−	100	μAdc
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc)				
2N6109		−	100	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc)				
2N6107, 2N6292		−	100	
(V_{CE} = 30 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)				
2N6111, 2N6288		−	2.0	mAdc
(V_{CE} = 50 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)				
2N6109		−	2.0	
(V_{CE} = 70 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)				
2N6107, 2N6292		−	2.0	
Emitter Cutoff Current	I_{EBO}			mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)		−	1.0	
ON CHARACTERISTICS (Note 3)				
DC Current Gain	h_{FE}			−
(I_C = 2.0 Adc, V_{CE} = 4.0 Vdc)				
2N6107, 2N6292		30	150	
(I_C = 2.5 Adc, V_{CE} = 4.0 Vdc)				
2N6109		30	150	
(I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)				
2N6111, 2N6288		30	150	
(I_C = 7.0 Adc, V_{CE} = 4.0 Vdc)				
All Devices		2.3	−	
Collector−Emitter Saturation Voltage	$V_{CE(sat)}$			Vdc
(I_C = 7.0 Adc, I_B = 3.0 Adc)		−	3.5	
Base−Emitter On Voltage	$V_{BE(on)}$			Vdc
(I_C = 7.0 Adc, V_{CE} = 4.0 Vdc)		−	3.0	
DYNAMIC CHARACTERISTICS				
Current Gain − Bandwidth Product (Note 4)	f_T			MHz
(I_C = 500 mAdc, V_{CE} = 4.0 Vdc, f_{test} = 1.0 MHz)				
2N6288, 2N6292		4.0	−	
2N6107, 2N6109, 2N6111		10	−	
Output Capacitance	C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		−	250	
Small−Signal Current Gain	h_{fe}			−
(I_C = 0.5 Adc, V_{CE} = 4.0 Vdc, f = 50 kHz)		20	−	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Indicates JEDEC Registered Data.
3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
4. $f_T = |h_{fe}| \bullet f_{test}$

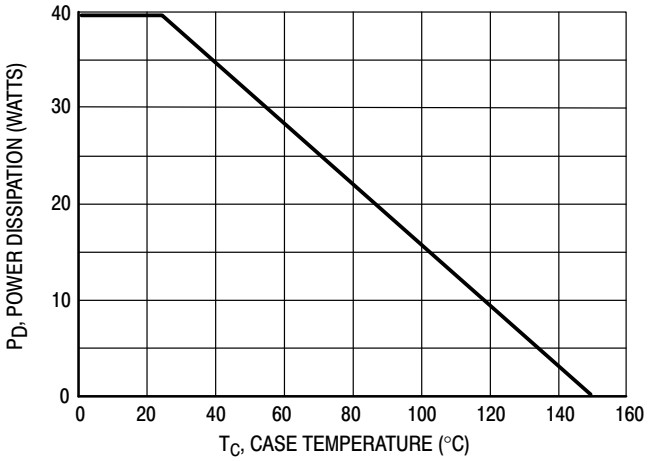


Figure 1. Power Derating

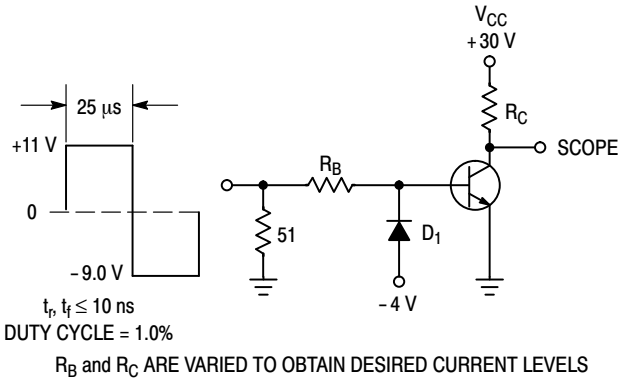


Figure 2. Switching Time Test Circuit

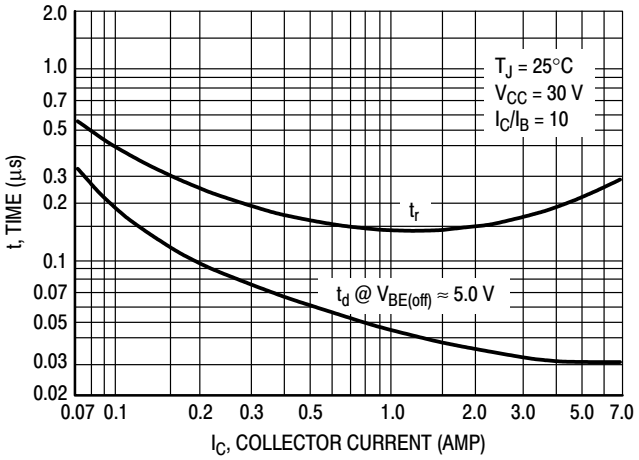


Figure 3. Turn−On Time

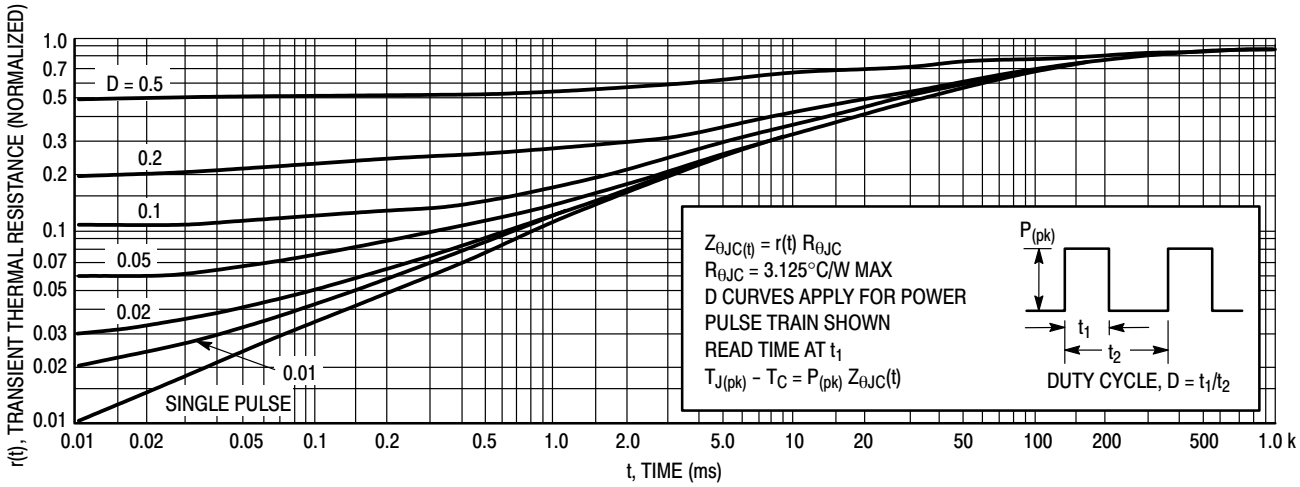


Figure 4. Thermal Response

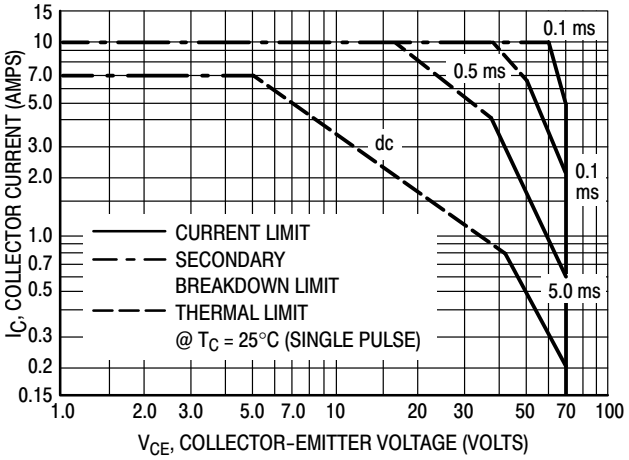


Figure 5. Active−Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

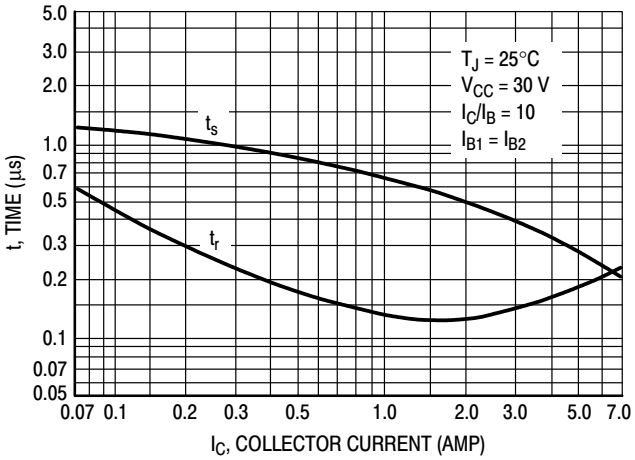


Figure 6. Turn−Off Time

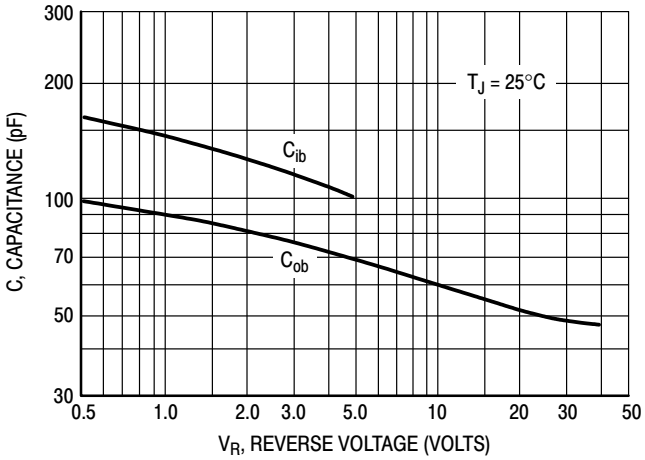
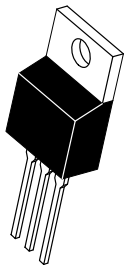


Figure 7. Capacitance

ORDERING INFORMATION

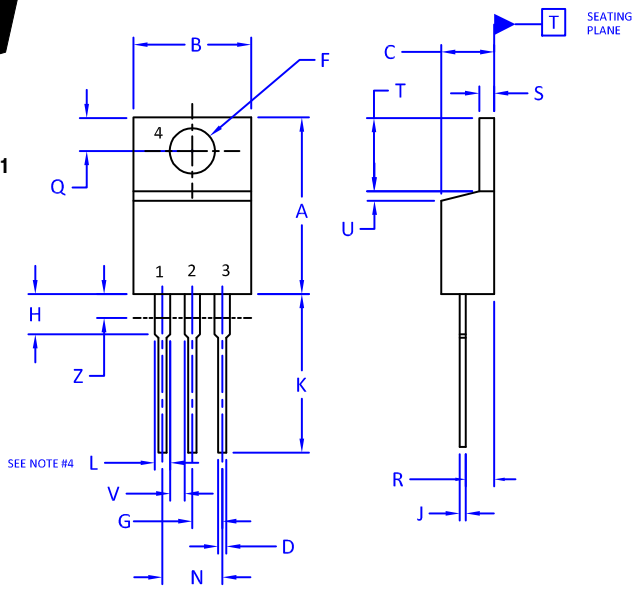
Device	Device Marking	Package	Shipping
2N6107G	2N6107	TO−220 (Pb−Free)	50 Units / Rail
2N6109G	2N6109	TO−220 (Pb−Free)	50 Units / Rail
2N6111G	2N6111	TO−220 (Pb−Free)	50 Units / Rail
2N6288G	2N6288	TO−220 (Pb−Free)	50 Units / Rail
2N6292G	2N6292	TO−220 (Pb−Free)	50 Units / Rail



SCALE 1:1

TO−220
CASE 221A
ISSUE AK

DATE 13 JAN 2022



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. MAX WIDTH FOR F102 DEVICE = 1.35MM

	INCHES		MILLIMETERS	
DIM	MIN.	MAX.	MIN.	MAX.
A	0.570	0.620	14.48	15.75
B	0.380	0.415	9.66	10.53
C	0.160	0.190	4.07	4.83
D	0.025	0.038	0.64	0.96
F	0.142	0.161	3.60	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.024	0.36	0.61
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.41
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	----	1.15	---
Z	----	0.080	---	2.04

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

STYLE 3:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 4:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 6:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

STYLE 8:
PIN 1. CATHODE
2. ANODE
3. EXTERNAL TRIP/DELAY
4. ANODE

STYLE 9:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 10:
PIN 1. GATE
2. SOURCE
3. DRAIN
4. SOURCE

STYLE 11:
PIN 1. DRAIN
2. SOURCE
3. GATE
4. SOURCE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. NOT CONNECTED

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