

PNP - 2N6040, 2N6042, NPN - 2N6043, 2N6045



ON Semiconductor®

www.onsemi.com

Plastic Medium-Power Complementary Silicon Transistors

Plastic medium-power complementary silicon transistors are designed for general-purpose amplifier and low-speed switching applications.

Features

- High DC Current Gain – $h_{FE} = 2500$ (Typ) @ $I_C = 4.0$ Adc
- Collector–Emitter Sustaining Voltage – @ 100 mAdc –
 $V_{CE(sus)} = 60$ Vdc (Min) – 2N6040, 2N6043
 $= 100$ Vdc (Min) – 2N6042, 2N6045
- Low Collector–Emitter Saturation Voltage –
 $V_{CE(sat)} = 2.0$ Vdc (Max) @ $I_C = 4.0$ Adc – 2N6043,44
 $= 2.0$ Vdc (Max) @ $I_C = 3.0$ Adc – 2N6042, 2N6045
- Monolithic Construction with Built–In Base–Emitter Shunt Resistors
- Epoxy Meets UL 94 V–0 @ 0.125 in
- ESD Ratings: Human Body Model, 3B > 8000 V
Machine Model, C > 400 V
- These Devices are Pb–Free and are RoHS Compliant*

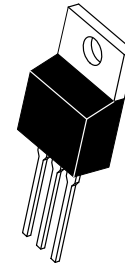
MAXIMUM RATINGS (Note 1)

| Rating | Symbol | Value | Unit |
|---|--------------------------------------|------------------------|--------------------------|
| Collector–Emitter Voltage | 2N6040 2N6043 2N6042 2N6045 | V_{CEO} 60 100 | Vdc |
| Collector–Base Voltage | 2N6040 2N6043 2N6042 2N6045 | V_{CB} 60 100 | Vdc |
| Emitter–Base Voltage | | V_{EB} 5.0 | Vdc |
| Collector Current | Continuous Peak | I_C 8.0 16 | Adc |
| Base Current | | I_B 120 | mAdc |
| Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C | | P_D 75 0.60 | W W/ $^\circ\text{C}$ |
| Operating and Storage Junction Temperature Range | T_J, T_{stg} | –65 to +150 | $^\circ\text{C}$ |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Indicates JEDEC Registered Data.

DARLINGTON, 8 AMPERES COMPLEMENTARY SILICON POWER TRANSISTORS 60 – 100 VOLTS, 75 WATTS



TO-220
CASE 221A
STYLE 1

MARKING DIAGRAM



2N604x = Device Code
x = 0, 2, 3, or 5
A = Assembly Location
Y = Year
WW = Work Week
G = Pb–Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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THERMAL CHARACTERISTICS

| Characteristic | Symbol | Max | Unit |
|---|---------------|------|------|
| Thermal Resistance, Junction-to-Case | θ_{JC} | 1.67 | °C/W |
| Thermal Resistance, Junction-to-Ambient | θ_{JA} | 57 | °C/W |

*ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | Min | Max | Unit |
|---|----------------|-----------------------|-------------------------------|---------------|
| OFF CHARACTERISTICS | | | | |
| Collector-Emitter Sustaining Voltage ($I_C = 100\text{ mAdc}$, $I_B = 0$) | $V_{CEO(sus)}$ | 60 100 | – – | Vdc |
| Collector Cutoff Current ($V_{CE} = 60\text{ Vdc}$, $I_B = 0$) ($V_{CE} = 100\text{ Vdc}$, $I_B = 0$) | I_{CEO} | – – | 20 20 | μA |
| Collector Cutoff Current ($V_{CE} = 60\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CE} = 100\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CE} = 60\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 150^\circ\text{C}$) ($V_{CE} = 80\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 150^\circ\text{C}$) ($V_{CE} = 100\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 150^\circ\text{C}$) | I_{CEX} | – – – – – | 20 20 200 200 200 | μA |
| Collector Cutoff Current ($V_{CB} = 60\text{ Vdc}$, $I_E = 0$) ($V_{CB} = 100\text{ Vdc}$, $I_E = 0$) | I_{CBO} | – – | 20 20 | μA |
| Emitter Cutoff Current ($V_{BE} = 5.0\text{ Vdc}$, $I_C = 0$) | I_{EBO} | – | 2.0 | mAdc |

ON CHARACTERISTICS

| | | | | |
|--|---------------|---------------------|-----------------------|-----|
| DC Current Gain ($I_C = 4.0\text{ Adc}$, $V_{CE} = 4.0\text{ Vdc}$) ($I_C = 3.0\text{ Adc}$, $V_{CE} = 4.0\text{ Vdc}$) ($I_C = 8.0\text{ Adc}$, $V_{CE} = 4.0\text{ Vdc}$) | h_{FE} | 1000 1000 100 | 20,000 20,000 – | – |
| Collector-Emitter Saturation Voltage ($I_C = 4.0\text{ Adc}$, $I_B = 16\text{ mAdc}$) ($I_C = 3.0\text{ Adc}$, $I_B = 12\text{ mAdc}$) ($I_C = 8.0\text{ Adc}$, $I_B = 80\text{ Adc}$) | $V_{CE(sat)}$ | – – – | 2.0 2.0 4.0 | Vdc |
| Base-Emitter Saturation Voltage ($I_C = 8.0\text{ Adc}$, $I_B = 80\text{ mAdc}$) | $V_{BE(sat)}$ | – | 4.5 | Vdc |
| Base-Emitter On Voltage ($I_C = 4.0\text{ Adc}$, $V_{CE} = 4.0\text{ Vdc}$) | $V_{BE(on)}$ | – | 2.8 | Vdc |

DYNAMIC CHARACTERISTICS

| | | | | |
|---|------------|--------|------------|----|
| Small Signal Current Gain ($I_C = 3.0\text{ Adc}$, $V_{CE} = 4.0\text{ Vdc}$, $f = 1.0\text{ MHz}$) | $ h_{fe} $ | 4.0 | – | |
| Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f = 0.1\text{ MHz}$) | C_{ob} | – – | 300 200 | pF |
| Small-Signal Current Gain ($I_C = 3.0\text{ Adc}$, $V_{CE} = 4.0\text{ Vdc}$, $f = 1.0\text{ kHz}$) | h_{fe} | 300 | – | – |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

*Indicates JEDEC Registered Data.

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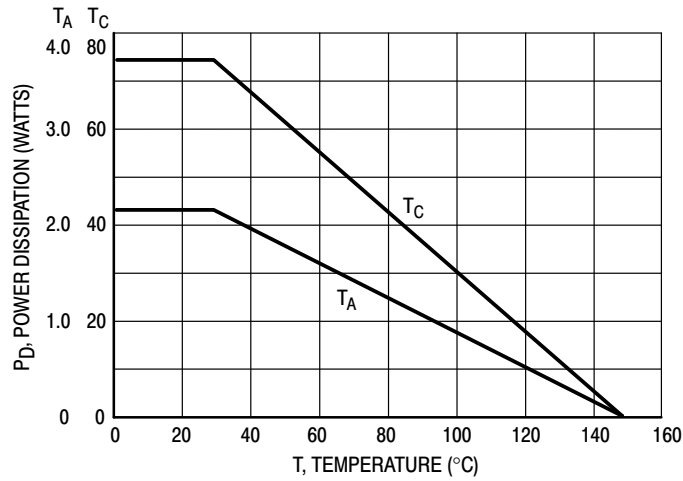


Figure 1. Power Derating

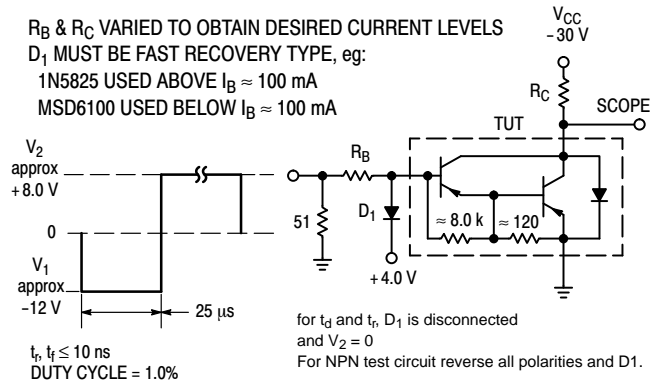


Figure 2. Switching Times Equivalent Circuit

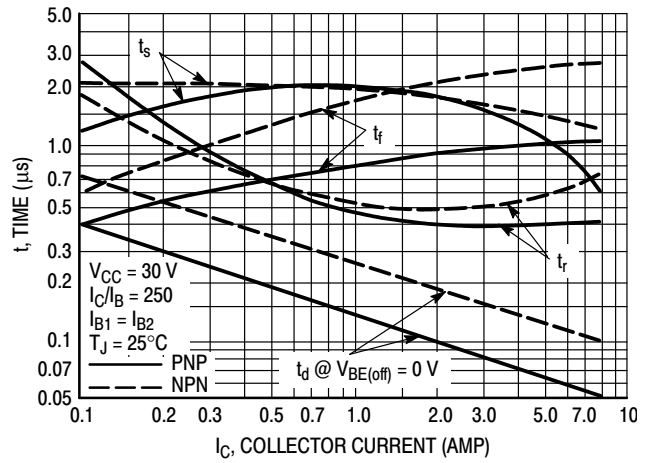


Figure 3. Switching Times

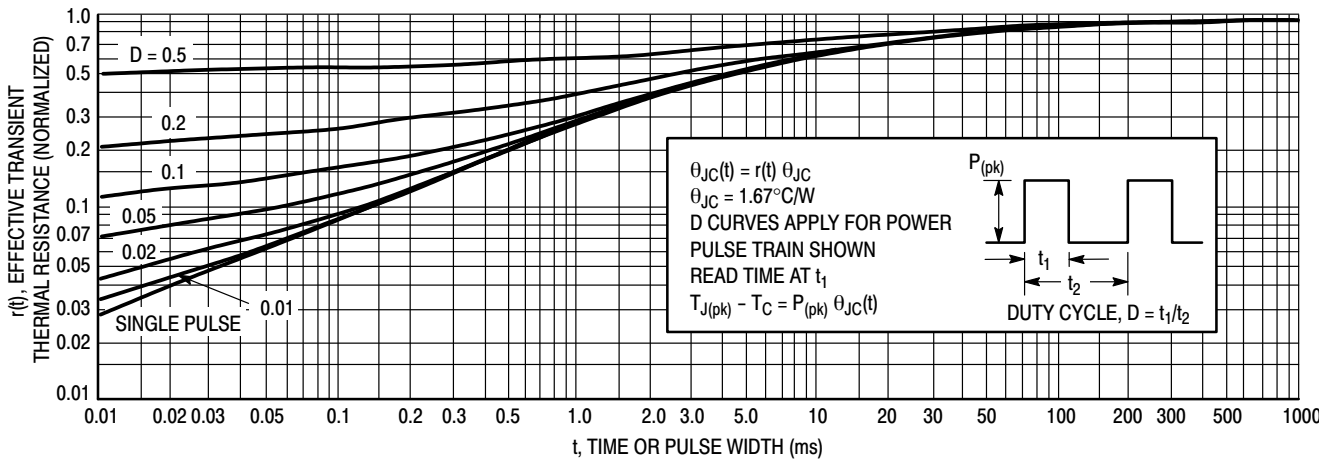


Figure 4. Thermal Response

PNP – 2N6040, 2N6042, NPN – 2N6043, 2N6045

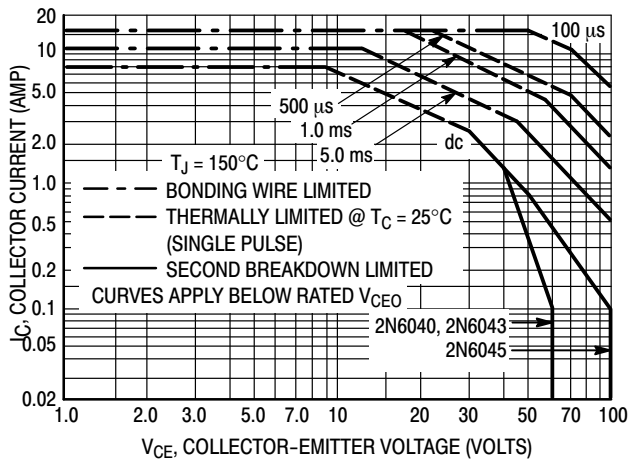


Figure 5. Active-Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

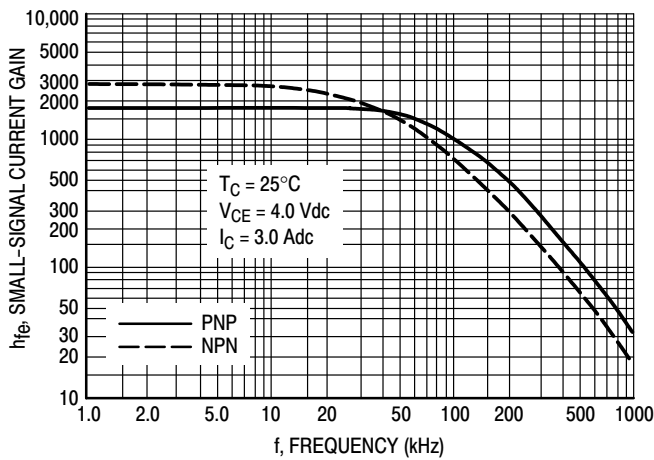


Figure 6. Small-Signal Current Gain

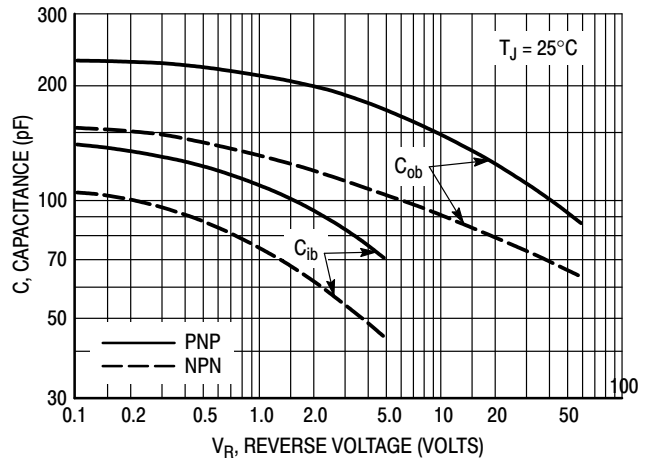


Figure 7. Capacitance

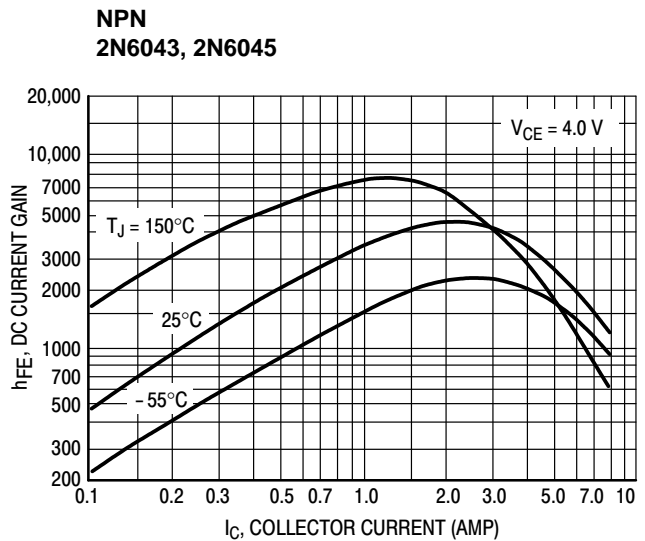
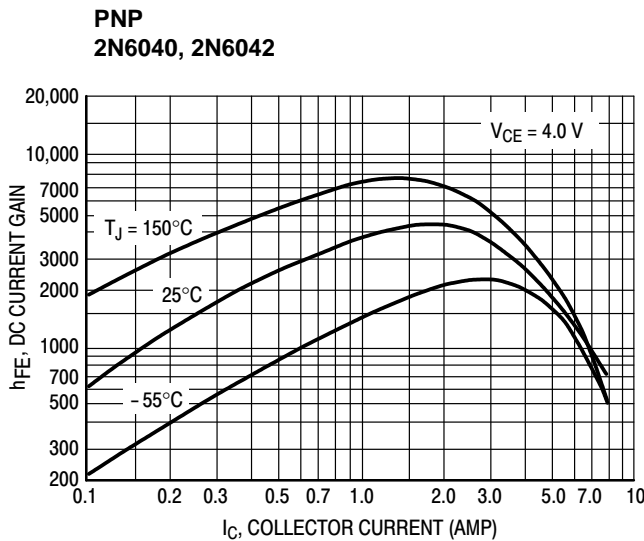


Figure 8. DC Current Gain

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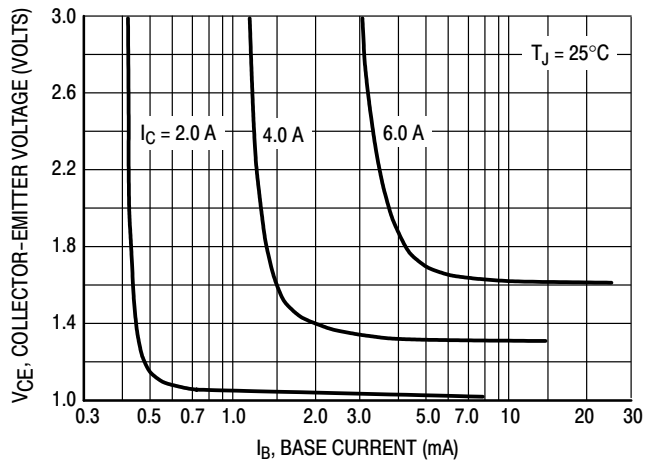
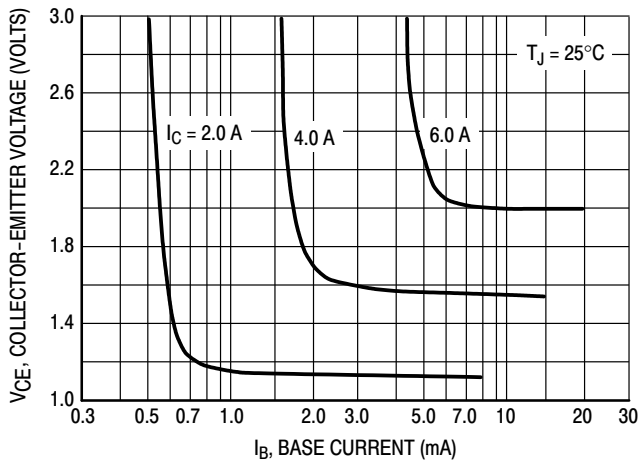


Figure 9. Collector Saturation Region

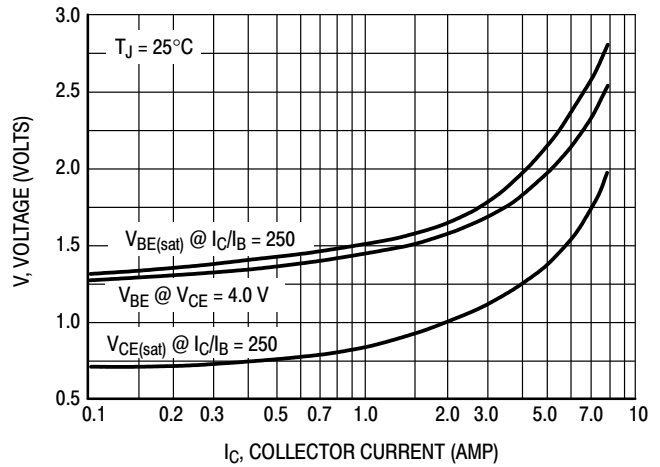
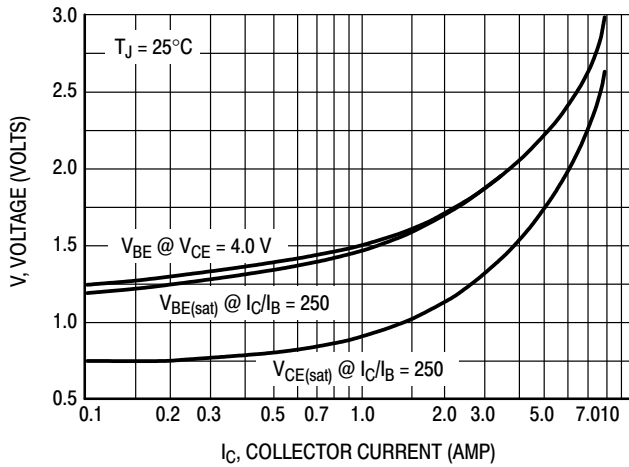


Figure 10. "On" Voltages

ORDERING INFORMATION

| Device | Package | Shipping |
|---------|---------------------|-----------------|
| 2N6040G | TO-220 (Pb-Free) | 50 Units / Rail |
| 2N6042G | TO-220 (Pb-Free) | 50 Units / Rail |
| 2N6043G | TO-220 (Pb-Free) | 50 Units / Rail |
| 2N6045G | TO-220 (Pb-Free) | 50 Units / Rail |

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



TO-220 CASE 221A ISSUE AK

DATE 13 JAN 2022



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. MAX WIDTH FOR F102 DEVICE = 1.35MM

| DIM | INCHES | | MILLIMETERS | |
|-----|--------|-------|-------------|-------|
| | MIN. | MAX. | MIN. | MAX. |
| A | 0.570 | 0.620 | 14.48 | 15.75 |
| B | 0.380 | 0.415 | 9.66 | 10.53 |
| C | 0.160 | 0.190 | 4.07 | 4.83 |
| D | 0.025 | 0.038 | 0.64 | 0.96 |
| F | 0.142 | 0.161 | 3.60 | 4.09 |
| G | 0.095 | 0.105 | 2.42 | 2.66 |
| H | 0.110 | 0.161 | 2.80 | 4.10 |
| J | 0.014 | 0.024 | 0.36 | 0.61 |
| K | 0.500 | 0.562 | 12.70 | 14.27 |
| L | 0.045 | 0.060 | 1.15 | 1.52 |
| N | 0.190 | 0.210 | 4.83 | 5.33 |
| Q | 0.100 | 0.120 | 2.54 | 3.04 |
| R | 0.080 | 0.110 | 2.04 | 2.79 |
| S | 0.045 | 0.055 | 1.15 | 1.41 |
| T | 0.235 | 0.255 | 5.97 | 6.47 |
| U | 0.000 | 0.050 | 0.00 | 1.27 |
| V | 0.045 | --- | 1.15 | --- |
| Z | --- | 0.080 | --- | 2.04 |

STYLE 1:

- PIN 1. BASE
- 2. COLLECTOR
- 3. EMITTER
- 4. COLLECTOR

STYLE 2:

- PIN 1. BASE
- 2. EMITTER
- 3. COLLECTOR
- 4. EMITTER

STYLE 3:

- PIN 1. CATHODE
- 2. ANODE
- 3. GATE
- 4. ANODE

STYLE 4:

- PIN 1. MAIN TERMINAL 1
- 2. MAIN TERMINAL 2
- 3. GATE
- 4. MAIN TERMINAL 2

STYLE 5:

- PIN 1. GATE
- 2. DRAIN
- 3. SOURCE
- 4. DRAIN

STYLE 6:

- PIN 1. ANODE
- 2. CATHODE
- 3. ANODE
- 4. CATHODE

STYLE 7:

- PIN 1. CATHODE
- 2. ANODE
- 3. CATHODE
- 4. ANODE

STYLE 8:

- PIN 1. CATHODE
- 2. ANODE
- 3. EXTERNAL TRIP/DELAY
- 4. ANODE

STYLE 9:

- PIN 1. GATE
- 2. COLLECTOR
- 3. EMITTER
- 4. COLLECTOR

STYLE 10:

- PIN 1. GATE
- 2. SOURCE
- 3. DRAIN
- 4. SOURCE

STYLE 11:

- PIN 1. DRAIN
- 2. SOURCE
- 3. GATE
- 4. SOURCE

STYLE 12:

- PIN 1. MAIN TERMINAL 1
- 2. MAIN TERMINAL 2
- 3. GATE
- 4. NOT CONNECTED

| | | |
|------------------|-------------|--|
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| DESCRIPTION: | TO-220 | PAGE 1 OF 1 |

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